Journal of ELECTRONIC MATERIALS, Vol. 43, No. 2, 2014
DOI: 10.1007/s11664-013-2891-6

Electrodeposition of Indium Bumps for Ultrafine Pitch Interconnection

YINGTAO TIAN,[1,2,4] CHANGQING LIU,[1] DAVID HUTT,[1] and BOB STEVENS[3]

1.—Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, Loughborough, Leicestershire LE11 3TU, UK. 2.—School of Electronic, Electrical and Computer Engineering, University of Birmingham, Edgbaston, Birmingham B15 2TT, UK. 3.—iSMART, School of Science and Technology, Nottingham Trent University, Clifton Campus, Nottingham NG11 8NS, UK. 5.—e-mail: y.tian@bham.ac.uk

Electroplating is a promising method to produce ultrafine pitch indium bumps for assembly of pixel detectors in imaging applications. In this work, the process of indium bumping through electrodeposition was demonstrated and the influences of various current waveforms on the bump morphology, microstructure and height uniformity were investigated. Electron microscopy was used to study the microstructure of electroplated indium bumps and a Zygo white light interferometer was utilised to evaluate the height uniformity. The results indicated that the bump uniformities on wafer, pattern and feature scales were improved by using unipolar pulse and bipolar pulse reverse current waveforms.

Key words: Electroplating, indium bumps, ultrafine pitch interconnection

INTRODUCTION

The assembly of pixel detectors used for imaging applications, e.g. infrared focal plane array or particle detectors in high energy physics studies, requires direct interconnections between the readout chip and sensor chip.[1] The pixel detector systems usually have their active elements, i.e. pixels, in an array with distances less than 100 μm between them and the latest application is moving to less than 50 μm pitch. Such high density of connections (i.e. inputs/outputs, I/Os) necessitates very high yield flip chip assembly. Moreover, because most of the sensor chips are sensitive to excessive heat flow, a low temperature fabrication process is preferred in order to diminish thermal impact on the device. Therefore, the packaging of a pixel detector application needs to fulfil requirements including ultrafine pitch, high density of I/Os (may exceed 40,000/cm^2), high yield and low temperature processes.[2] Furthermore, in order to minimise the damage to the sensor induced by the radiation, the resulting device must frequently be capable of operating at cryogenic temperatures.[1]

Indium bump bonding has been developed to fulfil the requirements of pixel detector fabrication. Indium is a soft metal and has very good ductility in cryogenic environments such as in liquid nitrogen. The melting point of pure indium is only 156.6 °C and it is easy to form a good mechanical and electrical interconnection at room temperature, which makes indium bump bonding advantageous for these applications.

The current state-of-the-art indium bump bonding process was developed by the Paul Scherrer Institute (PSI), and consists of two lift-off steps on the sensor chip and one on the readout chip.[3] The PSI process uses a three-layer under bump metallisation (UBM) of Ti/Ni/Au, which is sputtered onto both the sensor and readout wafers. Indium is then deposited by evaporation, with indium bumps formed on the sensor part of the pixel module, while only a very thin indium layer is deposited onto the readout chip for better adhesion in the following bonding step. Before assembly, the evaporated indium bumps on the sensor wafer are reflowed to

(Received May 31, 2013; accepted October 26, 2013; published online November 21, 2013)

form truncated indium spheres. Finally, the readout chip is bonded to the sensor chip by applying appropriate pressure. The PSI process has been successfully employed in fabricating the PILATUS detector at 100 μm bonding footprint. However, when it comes to ultrafine pitch, i.e. less than 50 μm, the evaporation of indium bumps becomes difficult and time consuming and the process is not cost-effective due to the waste of material on the lift-off mask.

Electrodeposition has been a promising method to enable low-cost, ultrafine pitch and high yield wafer bumping. The process normally involves depositing a thin seed layer across the entire wafer followed by high resolution photoresist patterning. Then, appropriate solder material can be electroplated into the resist apertures and, following resist removal, the exposed seed layer is etched away.[4] It does not necessitate the time-consuming vacuum evaporation step, can minimise the waste of materials deposited on the undesired areas and is able to achieve ultrafine pitch through high resolution lithography. Challenges of the electroplating process exist in the uniformity and consistency of plated bumps at the wafer scale with ultra-fine pitch and high yield.

Electroplating of Sn-Pb and lead-free solder bumps have been widely employed in electronics manufacturing.[4–7] To date, electroplating indium bumping has been demonstrated by several researchers through various electrolyte solutions; however, the information on the uniformity and consistency of electroplated indium bumps on large areas is still limited in the current literature.[8–10] In earlier studies, the feasibility of electroplating indium using an indium sulphamate solution was investigated for wafer bumping.[11,12] The current paper presents results dedicated to systematically investigating the influences of the various current waveforms on the morphology, microstructure and uniformity of electroplated ultrafine pitch indium bumps.

EXPERIMENTAL DETAILS

Electroplating Bumping Process

The electroplating indium bumping process flow is illustrated in Fig. 1. Plain 100-mm-diameter silicon wafers were used as the substrates in this work. These wafers were metallised using e-beam evaporation with a thin seed layer consisting of 100 nm Ti, which acted as an adhesion promoter for a

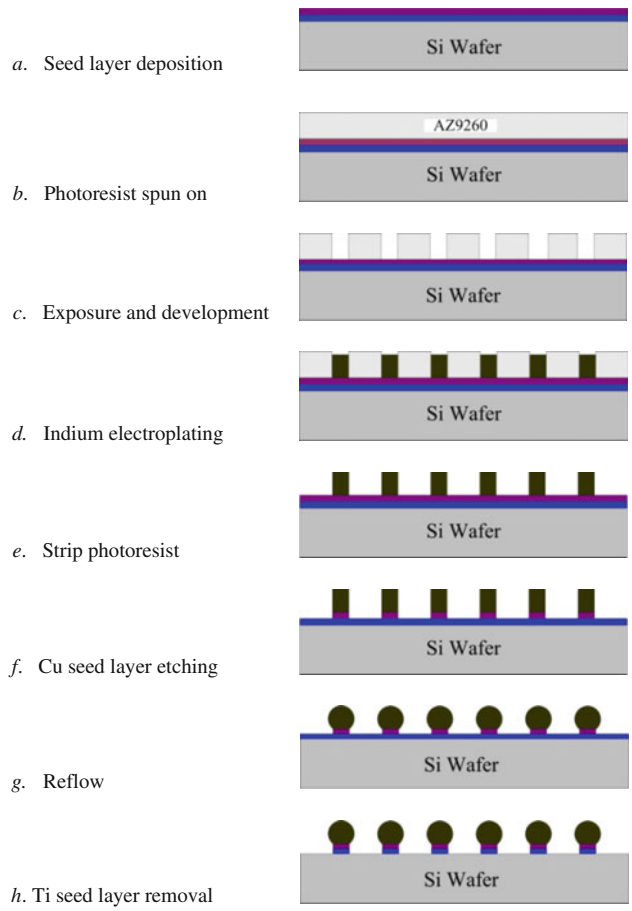

Fig. 1. Schematic of the electroplating bumping process.

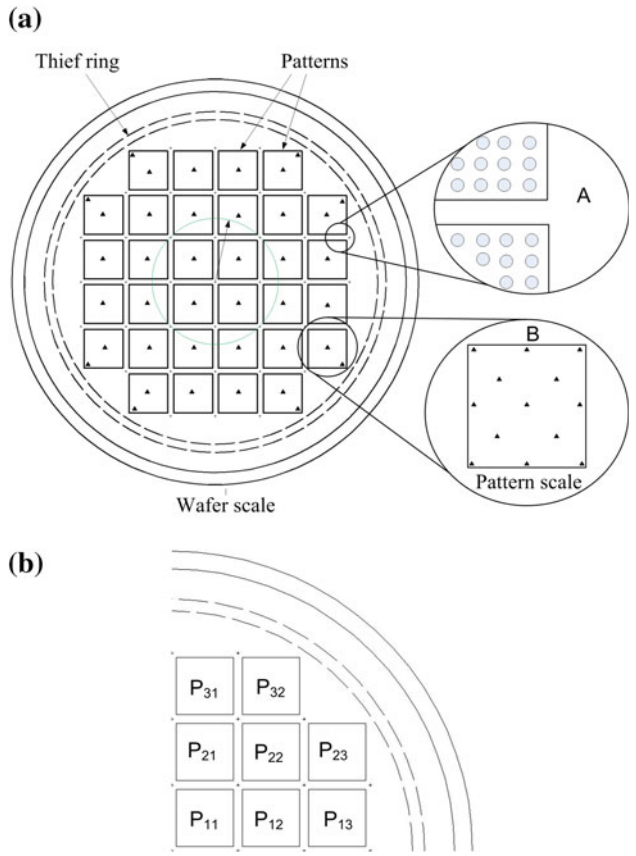

Fig. 2. **a** The layout of the wafer patterns and locations for uniformity measurement, and **b** the numbering of patterns in a quarter of the wafer.

further 100 nm of Cu. Once the seed layer was deposited, an approximately 20-μm-thick photoresist layer was spin-coated, exposed and developed to form the required pattern. In this step, a positive photoresist AZ9260 was preferred as it was easier to remove after electroplating. The photoresist pattern (Fig. 2) consisted of 32 die-sized areas distributed across the wafer, within which circular openings of 25 μm diameter arranged in a square array at 50 μm pitch were included, as shown in the zoomed-in view 'A' of the diagram. To achieve more uniform current distribution across the wafer, a circular current "thief ring" (1 mm in width) was also designed surrounding the patterns—this was not used in the earlier study.[11]

Indium bumps were electroplated onto the seed layer through the apertures defined by the photoresist, after which the photoresist was removed using acetone. The exposed Cu seed layer was then etched away using a nitric acid-based chemical bath. This left behind the titanium layer which was used to prevent indium from wetting the silicon substrate during the following reflow. The electroplated indium bumps were then reflowed to form truncated spheres. For production, the bottom Ti seed layer would also need to be removed afterwards. However, as this study focused on the electroplating process, the majority of the microstructure characterisation and bump height uniformity measurements were conducted on the as-plated bumps before reflow. Steps 'f' and 'g' were only carried out for feasibility demonstration.

Materials

An indium sulphamate solution, supplied by Indium (Milton Keynes, UK) was used for electroplating. The solution comprises of $In(NH_2SO_3)_3$ 105.36 g/L, $NaNH_2SO_3$ 150 g/L, HNH_2SO_3 26.4 g/L, NaCl 45.84 g/L, dextrose and triethanolamine.[13] A 99.9 % pure indium plate (8×8 cm^2) was utilised as the anode, having 100 % anode efficiency.

Cathodic Polarisation

Before the electroplating of indium bumps was carried out, it was necessary to determine the electrochemical characteristics of the indium sulphamate solution. A cathodic potentiodynamic polarisation was firstly conducted in the above electrochemical system by scanning the potential from an open circuit to -2.0 V (relative to a standard calomel electrode, SCE) at 0.5 mV/s to characterise the performance of the electrolyte. For this part of the study, a small piece of unpatterned wafer with blanket Cu seed layer was used as the cathode. A computer-controlled electroplating power system (PARSTAT® 2273, Potentiostat/Galvanostat; Princeton Applied Research, AMETEK) was utilised for the cathodic polarisation and the subsequent electroplating. On the basis of the cathodic polarisation curve, the parameters for the subsequent electroplating bumping were defined.

Electroplating Parameters

Electroplating of indium bumps was carried out through direct current (DC), unipolar pulse and bipolar pulse reverse current waveforms. Figure 3 illustrates the features of the unipolar pulse and bipolar pulse reverse current waveforms. The duty cycle is defined as $\{[t_{on}/(t_{on} + t_{off})] \times 100\ \%\}$ for unipolar pulse electroplating and $\{[t_{on(c)}/(t_{on(c)} + t_{on(a)} + t_{off})] \times 100\ \%\}$ for the bipolar pulse reverse plating. The average current densities of unipolar pulse and bipolar pulse reverse current were kept the same as the DC condition at 10 mA/cm^2 to enable direct comparison. In this case, the electrodeposition rate was calculated to be around 0.3 μm/min according to Faraday's law and all electroplating was conducted for 60 min at room temperature, thereby aiming to achieve 18-μm-thick indium bumps. Table I details the parameters of the various current waveforms for electrodeposition of indium bumps.

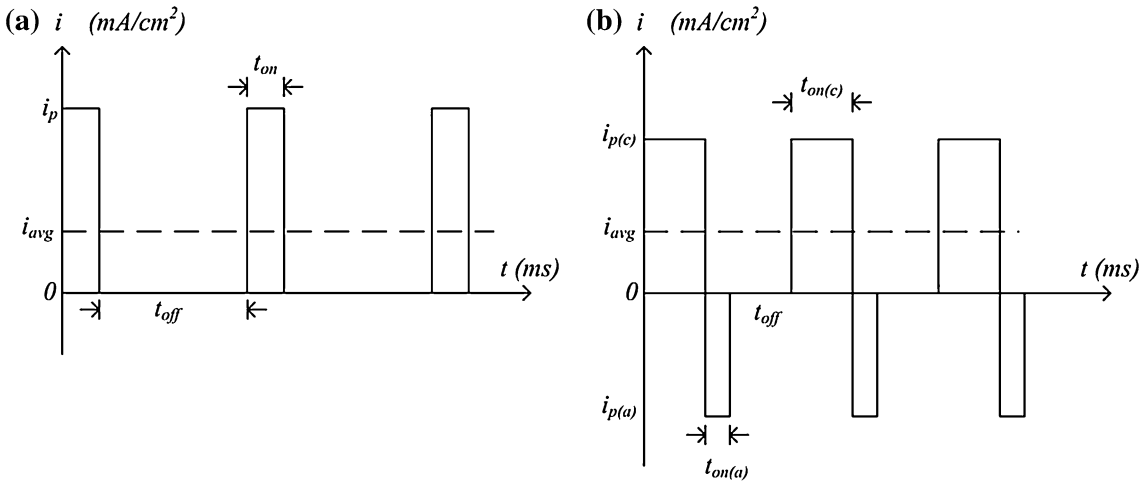

Fig. 3. Features of unipolar pulse (**a**) and bipolar pulse reverse (**b**) current waveforms.

Table I. Parameters of DC, pulse and pulse reverse electroplating for indium bumping using sulphamate solution

	Type I: DC electroplating					
No.	i_{avg} (mA/cm^2)					
1	10					
	Type II: Unipolar pulse electroplating					
No.	t_{on} (ms)	i_p (mA/cm^2)	t_{off} (ms)	Frequency (Hz)	Duty cycle (%)	i_{avg} (mA/cm^2)
2	1	50	4	200	20	10
3	2	50	8	100	20	10
4	1	100	9	100	10	10
	Type III: Bipolar pulse reverse electroplating					
No.	$i_{p(c)}$ (mA/cm^2)	$t_{on(c)}$ (ms)	$i_{p(a)}$ (mA/cm^2)	$t_{on(a)}$ (ms)	t_{off} (ms)	Frequency (Hz)	i_{avg} (mA/cm^2)
5	50	1.5	50	0.5	3	200	10
6	100	1.5	100	0.5	8	100	10

Characterisation

The bump morphology and microstructures were observed using scanning electron microscopy (SEM) assisted by focused ion beam (FIB; FEI Nova 600 Nanolab Dual Beam System) and energy-dispersive x-ray spectroscopy (EDX). Because indium is a soft material, the traditional mechanical polishing approach will result in the grinding particles becoming embedded in the indium. The as-plated indium bumps were therefore examined on the wafer directly, utilising the flexibility of the dual beam system. In addition, the bump height was measured by using a Zygo NewView 5000 system and the uniformity was assessed on different scales, i.e. wafer scale, pattern scale and feature scale, by measuring bumps selected from a number of areas, indicated by the triangles shown in Fig. 2a. Here, the bump uniformity was
calculated as:

$$\text{Uniformity} = \frac{\text{Max. Bump Height} - \text{Min. Bump Height}}{2 \times \text{Average Bump Height}} \times 100\,\%. \quad (1)$$

RESULTS AND DISCUSSION

Cathodic Polarisation

The electrochemical reduction of reactive species in the sulphamate solution and the cathodic behavior of the bath were examined, as illustrated in Fig. 4. When the external potential was applied, indium deposition on the cathode surface did not start immediately. The initial part of the curve in Fig. 4 shows a negligible current density (less than 0.01 mA/cm^2) up to a potential of about −0.65 V. A so-called activation overpotential needs to be built up to begin the reduction of metal ions. The electrodeposition of indium began sharply when the cathodic potential was approximately −0.65 V until it reached a final limiting current density of around 30 mA/cm^2. Then, the current density dropped although the potential kept rising due to the inhibitive effect of additives.[14] The further increase in the current density from the potential of −1.15 V onward can be attributed to hydrogen evolution.

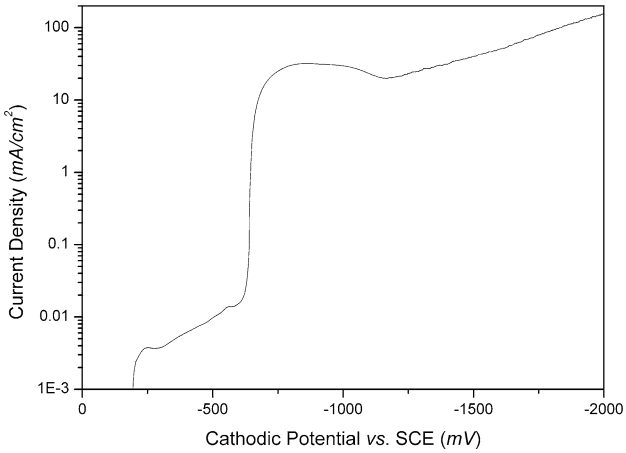

Fig. 4. Cathodic polarisation curve for In deposition onto Cu coupons in indium sulphamate solution. Potential scanning rate is 0.5 mV/s.

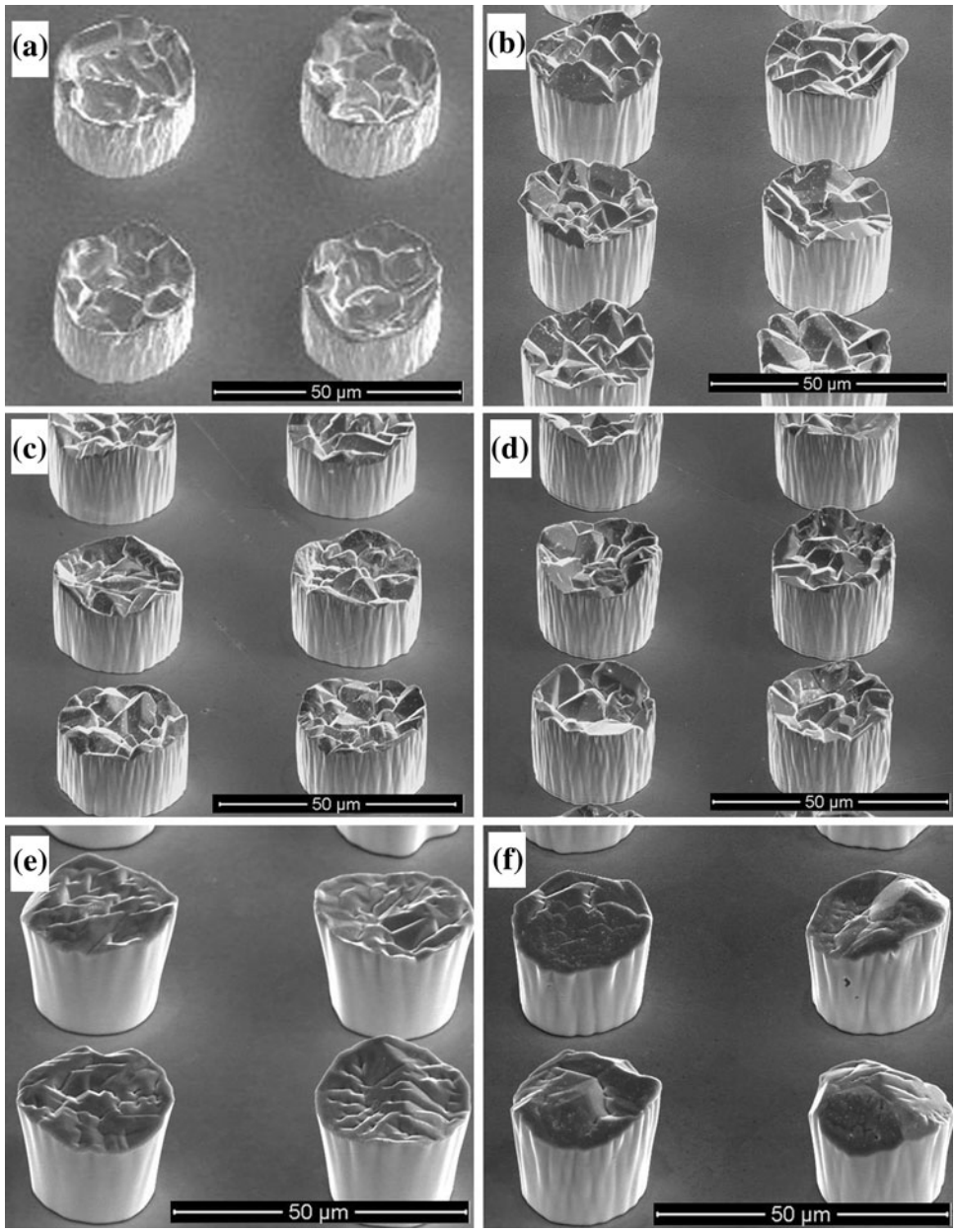

Fig. 5. Morphology of electroplated indium bumps deposited with different current waveforms as shown in Table I: **a** waveform 1, **b** waveform 2, **c** waveform 3, **d** waveform 4, **e** waveform 5 and **f** waveform 6.

Morphology of Electroplated Indium Bumps

Figure 5 shows the morphology of electroplated indium bumps deposited with the various current waveforms listed in Table I. These images were obtained after the removal of the photoresist, but before etching of the copper seed layer. In general, the electroplating method produced a very high yield, in which, in this case, the yield is defined by the presence of an indium bump. It can be seen that the DC electroplated indium bumps have very coarse grain size and typically a hollow in the centre, which was caused by the current crowding effect near the opening of the photoresist feature. Current crowding occurs when the cathode is smaller than the anode so that the current line preferably accumulates near the edge of the cathode resulting in a relatively higher current density. A sacrificial auxiliary cathode is often used by surrounding the periphery of the cathode to absorb the excessive current density and leave a uniform current distribution across the cathode.

High frequency pulse plating has been shown to give significant changes in the electroplating

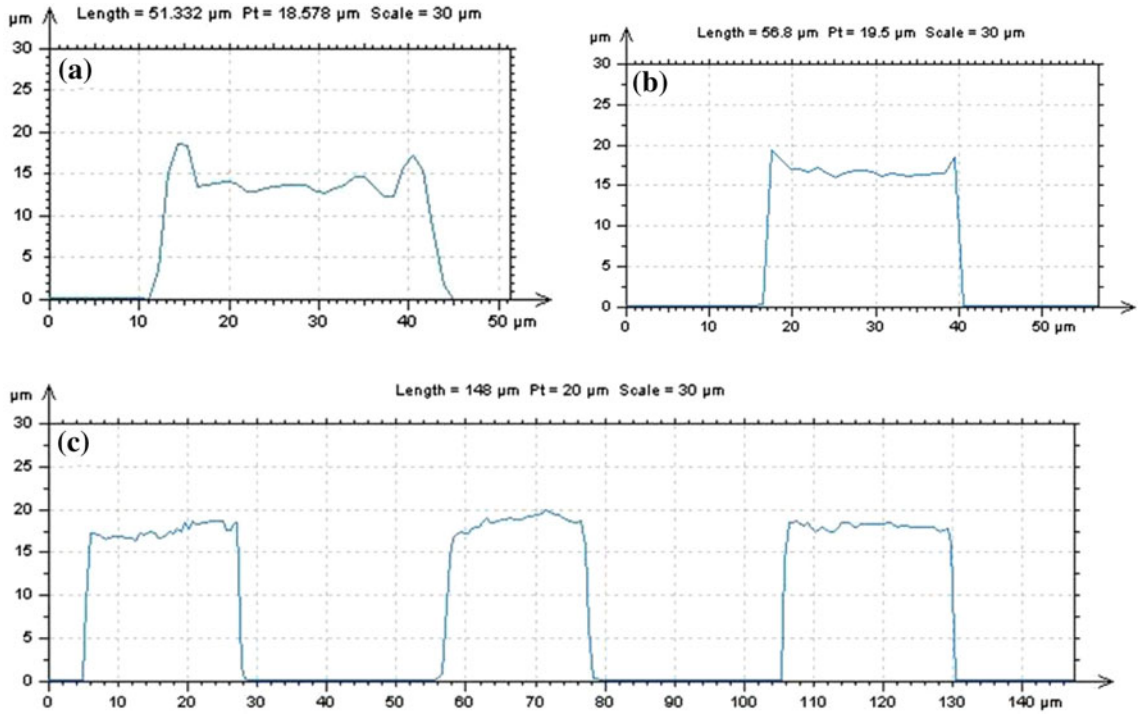

Fig. 6. Indium bump profiles measured using the Zygo white light interferometer: **a** DC, **b** pulse and **c** pulse reverse electroplating.

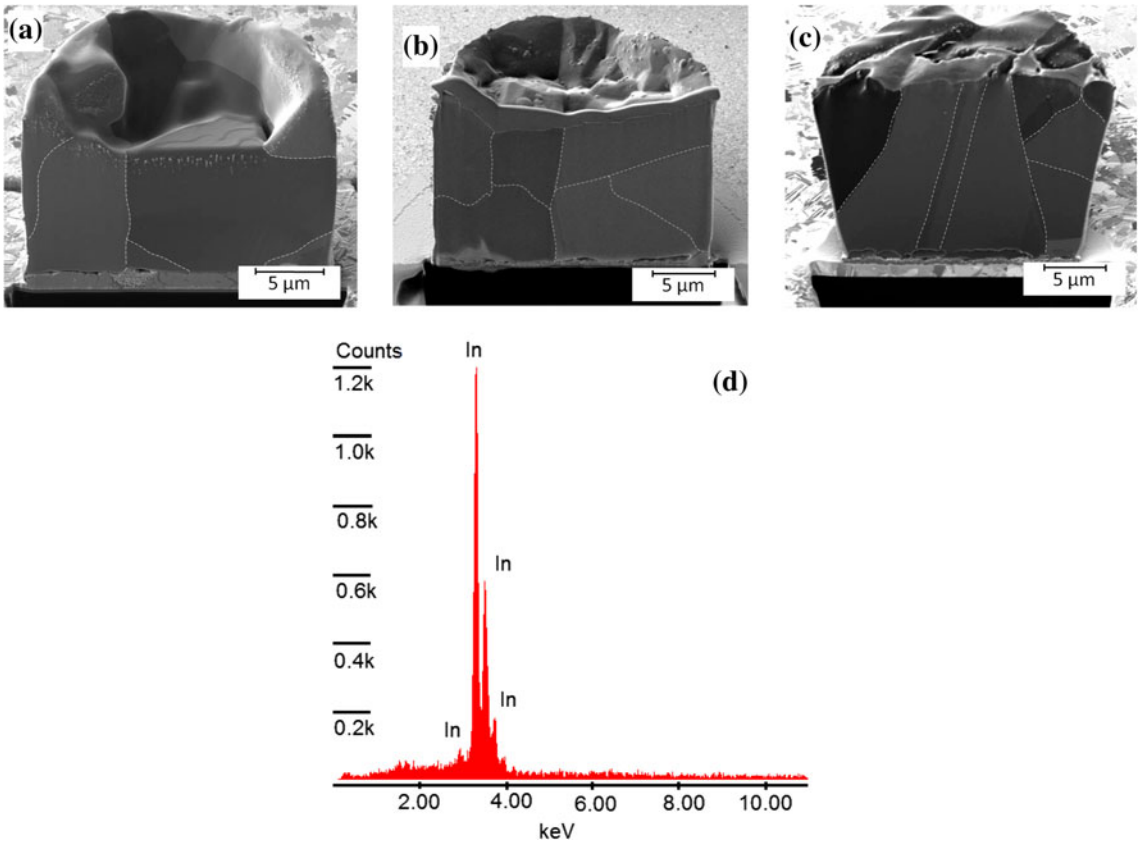

Fig. 7. Cross-section analysis of indium bumps obtained through different current waveforms: **a** DC, **b** unipolar pulse, **c** bipolar pulse reverse and **d** EDX analysis of the electroplated indium.

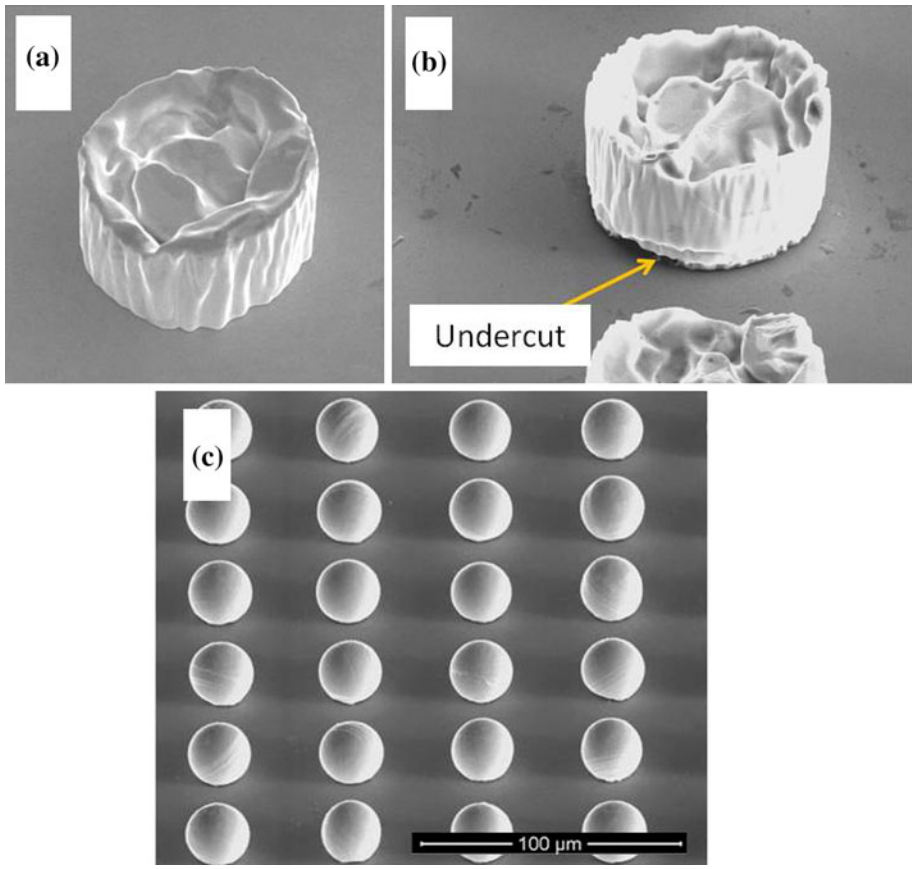

Fig. 8. Seed layer etching and indium bump reflow: **a** before etching, **b** after etching and **c** after reflow. The bumps were obtained by DC electroplating.

bumping process, such as improved surface flatness, suppression of abnormal growth and reduced grain size.[15] The use of a short current pulse allows a much higher peak current during the pulse-on period, and, during the pulse-off period, the solution is able to recover the reactants. The uneven top surface of the bumps deposited here appears to be levelled to some extent in the case of pulse electroplating which also gives a finer grain size. However, very little difference can be found between the deposits for waveforms 2–4. In other words, in the range of parameters investigated here, no obvious influence of pulse current on bump morphology was observed.

For the pulse reverse electroplating (waveforms 5 and 6), the surface flatness of the bumps is apparently improved because of the additional anodic cycle. In pulse reverse electroplating, the anodic cycle can dissolve part of the deposit on the cathode surface, especially on protruding points, and result in a levelling effect.[16] Figure 6 shows profiles of the bumps obtained using the Zygo white light interferometer and illustrates the changes to the bump top surface caused by different current waveforms, especially the improvement of surface flatness induced by using pulse and pulse reverse current waveforms.

Microstructure Analysis

Cross-section analysis of electroplated indium bumps was conducted using FIB, as shown in Fig. 7. The DC electroplated bump contains only a few large-sized grains which could reach more than 10 μm in size. In comparison, indium bumps obtained through pulse and pulse reverse electroplating present grain refinement to some extent. However, little difference can be found between pulse and pulse reverse electroplating conditions. In all electroplating conditions, no defects or impurities were found in the electroplated indium bumps and EDX analysis confirmed that the bumps contained pure indium.

Seed Layer Etching and Reflow

After In electroplating, the top Cu seed layer was removed using a nitric acid-based etchant. As mentioned above, the Ti layer remained after this

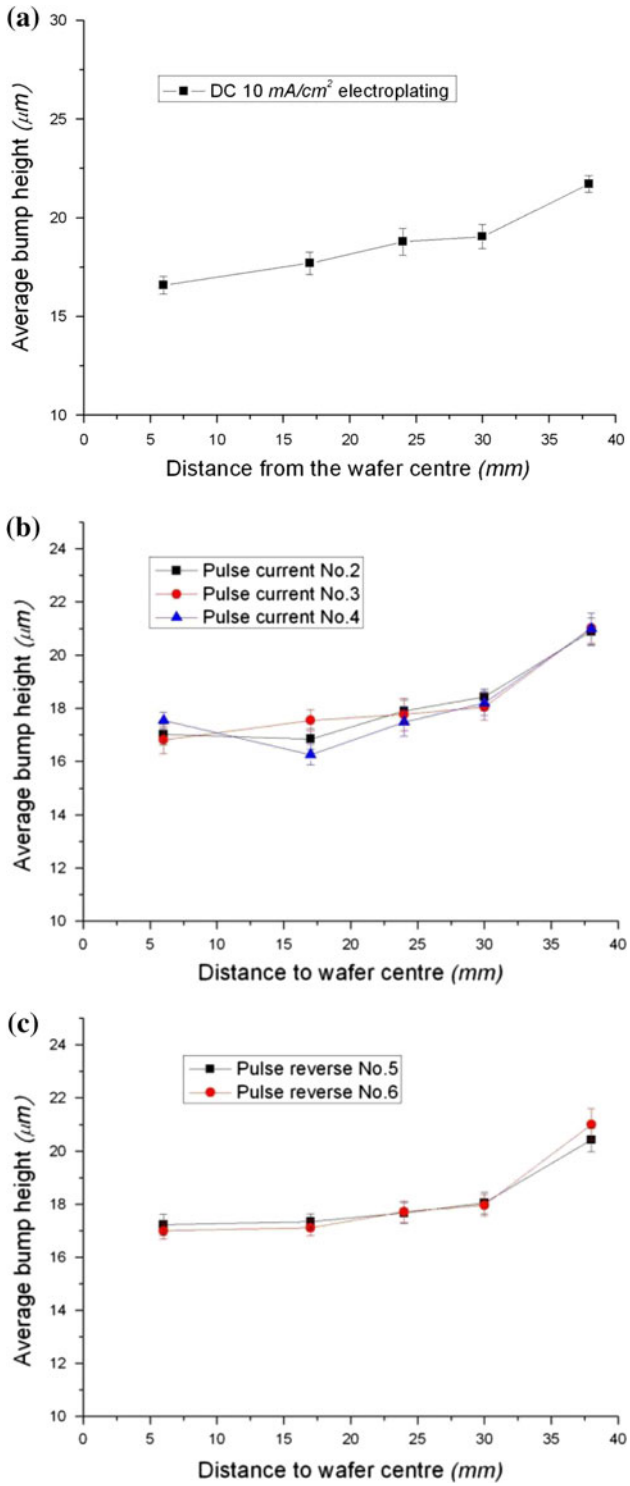

Fig. 9. Wafer scale uniformity measurement: **a** DC, **b** pulse and **c** pulse reverse electroplating.

treatment and was used as a non-wettable material during reflow to prevent the spread of the indium across the surface. Indium bumps were also attacked by the etchant resulting in a noticeable undercut near the base, but most of the bump material stayed on the wafer (Fig. 8b). Ideally, the indium bumps should be reflowed in an oven with a reducing atmosphere.[10,17] However, for demonstration purposes, a liquid flux was applied and the bumps were reflowed in a conventional reflow oven with a peak temperature of 200 °C. Figure 8c shows the reflowed indium bumps with the truncated sphere shape.

Influences of Current Waveforms on Uniformity

Height uniformity of the as-plated indium bumps was evaluated by measuring bumps located on the wafer and within the individual patterns as indicated by the triangles in Fig. 2a, and calculated using Eq. 1. Because the patterns were symmetrically distributed on the wafer, the bump height was averaged to a quarter of the wafer area within the patterns P_{11}, P_{21}, etc., in Fig. 2b. Figure 9 plots the average pattern bump height as a function of distance from the centre of the wafer for different electroplating conditions. In this case, the distance is from the centre of the wafer to the centre of the pattern. In some cases, more than one pattern was at the same distance from the centre of the wafer (e.g. P_{12} and P_{21}) and these bump heights were therefore averaged for the purposes of the graphs. The bump height was determined in the Zygo software by normalising the bump profile, i.e. the software identified the average height across the bump allowing for the maxima and minima in the profile. It can be seen that, in all electroplating conditions, the bump height was noticeably larger near the periphery area of the wafer which was induced by the typical 'terminal effect'.[18] This is due to the resistance of the very thin seed layer which is no longer negligible and causes a potential drop from the edge to the centre as the electrical contact is normally made near the wafer boundary. The higher potential near the wafer boundary can draw a larger current and result in an increased bump height.

It was calculated that the bump height uniformity was 19.65 % for DC electroplating (Fig. 9a). The uniformity for pulse current waveforms 2, 3 and 4 (as listed in Table I) were reduced to 14.3, 15.2 and 14.96 %, respectively (Fig. 9b). In the case of pulse reverse electroplating, the wafer scale uniformity for waveforms 5 and 6 were further reduced to about 13.6 and 14.07 %, respectively (Fig. 9c). Although little difference was found between the unipolar pulse and bipolar pulse reverse electroplating in terms of the wafer scale bump uniformity, indium bumps obtained through pulse reverse electroplating were the most uniform. Bumps near the wafer boundary can act as protruding points during the anodic cycle and can also be dissolved more into the solution resulting in a better uniformity. Furthermore, the wafer boundary can also draw higher potential during the reverse cycle which can dissolve more material into the solution and contribute to the uniformity improvement.

The pattern (chip) scale uniformity was also evaluated using the format shown in Fig. 2 and calculated by Eq. 1. Again, the bump height was averaged to a quarter of the wafer. Within an individual pattern, the bump height distribution was found to show a similar trend to the wafer scale, i.e. bumps near the boundary of a pattern were taller than others in the centre. This is attributed to the current crowding effect on the pattern scale.[19] Figure 10 shows the pattern scale uniformity on a quarter of the wafer. The data are plotted based on the distance from the pattern centre to the wafer centre. It can be seen that the pattern scale uniformity is worst for DC plating, and for all depositions the uniformity generally deteriorates when the pattern is nearer to the wafer boundary which, again, is thought to be a reflection of the terminal effect. Again, as seen earlier in Fig. 6 at the feature scale, the use of pulse and pulse reverse electroplating has also demonstrated a significant improvement on the pattern scale uniformity. Particularly, in pulse reverse plating, the protruded bump edge caused by the current crowding was dissolved during the anodic cycle resulting in a more even bump top profile.

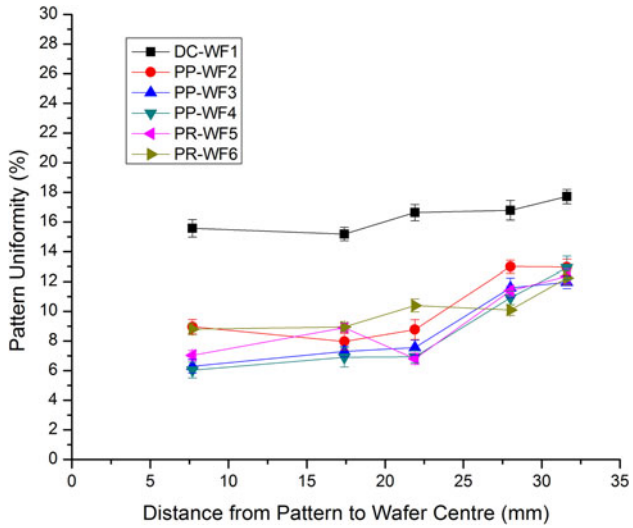

Fig. 10. Pattern scale uniformity of indium bumps obtained through different waveforms: *DC* direct current, *PP* unipolar pulse plating, *PR* bipolar pulse reverse plating. Waveform (*WF*) parameters refer to Table I.

CONCLUSIONS

The influence of different current waveforms on the electroplating of ultrafine pitch indium bumps in a sulphamate bath was investigated. In addition, the process of indium bumping for high density interconnection was also demonstrated. Electroplating is capable of producing high quality, ultrafine pitch and high yield indium bumps to replace the current evaporation process. The current waveform has significant influence on the morphology, microstructure and height uniformity of the indium bumps. The terminal effect in all electroplating conditions affects the wafer-scale uniformity resulting in higher bumps near the boundary area. By using pulse and pulse reverse current, the bump uniformity on the wafer, pattern and feature scale can be improved.

ACKNOWLEDGEMENTS

The authors would like to acknowledge DTA funding from the UK Engineering and Physical Sciences Research Council (EPSRC) through the Innovative Electronics Manufacturing Research Centre (IeMRC) and the support of the Science and Technology Facilities Council for access to processing facilities.

REFERENCES

1. N. Wermes, *Nucl. Instrum. Methods A* 512, 277 (2003).
2. L. Rossi, P. Fischer, and T. Rohe, *Pixel Detectors: From Fundamentals to Applications* (Berlin: Springer, 2006).
3. T. Rohe, C. Broennimann, F. Glaus, J. Gobrecht, S. Heising, M. Horisberger, R. Horisberger, H.C. Kastli, J. Lehmann, and S. Streuli, *Nucl. Instrum. Methods A* 565, 303 (2006).
4. M. Datta and D. Landolt, *Electrochim. Acta* 45, 2535 (2000).
5. L.T. Romankiw, *Electrochim. Acta* 42, 2985 (1997).
6. Y. Qin, G.D. Wilcox, and C. Liu, *J. Electrochem. Soc.* 156, D424 (2009).
7. M. Datta, R.V. Shenoy, C. Jahnes, P.C. Andricacos, J. Horkans, J.O. Dukovic, L.T. Romankiw, J. Roeder, H. Deligianni, H. Nye, B. Agarwala, H.M. Tong, and P. Totta, *J. Electrochem. Soc.* 142, 3779 (1995).
8. P. Merken, J. John, L. Zimmermann, and C. Van Hoof, *IEEE Trans. Adv. Packag.* 26, 60 (2003).
9. Q. Huang, G. Xu, and L. Luo, *2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)*, Beijing, China.
10. J. Jiang, S. Tsao, T. O'Sullivan, M. Razeghi, and G.J. Brown, *Infrared Phys. Technol.* 45, 143 (2004).
11. Y. Tian, C. Liu, D.A. Hutt, and R. Stevens, *Proceedings of the 58th Electronic Components & Technology Conference*, 2096 (2008).
12. Y. Tian, D.A. Hutt, and C. Liu, *2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)*, 456, Beijing, China.
13. *Operation Instruction of Indium Sulphamate Bath*, Indium Corporation, Released in 2008.
14. T.C. Franklin, *Surf. Coat. Technol.* 30, 415 (1987).
15. B. Kim and T. Ritzdorf, *J. Electrochem. Soc.* 151, C342 (2004).
16. M.S. Chandrasekar and M. Pushpavanam, *Electrochim. Acta* 53, 3313 (2008).
17. T. Fritzsch, R. Jordan, M. Töpper, J. Röder, I. Kuna, M. Lutz, F. Defo Kamga, J. Wolf, O. Ehrmann, H. Oppermann, and H. Reichl, *Nucl. Instrum. Methods A* 565, 309 (2006).
18. M. Matlosz, P.H. Vallotton, A.C. West, and D. Landolt, *J. Electrochem. Soc.* 139, 752 (1992).
19. B. DeBecker and A.C. West, *J. Electrochem. Soc.* 143, 486 (1996).