Stress Analysis and Output Power Measurement of an n-Mg₂Si Thermoelectric Power Generator with an Unconventional **Structure**

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We examine the mechanical stability of an unconventional Mg_2Si thermoelectric generator (TEG) structure. In this structure, the angle θ between the thermoelectric (TE) chips and the heat sink is less than 90° . We examined the tolerance to an external force of various Mg2Si TEG structures using a finiteelement method (FEM) with the ANSYS code. The output power of the TEGs was also measured. First, for the FEM analysis, the mechanical properties of sintered Mg_2Si TE chips, such as the bending strength and Young's modulus, were measured. Then, two-dimensional (2D) TEG models with various values of θ (90°, 75°, 60°, 45°, 30°, 15°, and 0°) were constructed in ANSYS. The x and y axes were defined as being in the horizontal and vertical directions of the substrate, respectively. In the analysis, the maximum tensile stress in the chip when a constant load was applied to the TEG model in the x direction was determined. Based on the analytical results, an appropriate structure was selected and a module fabricated. For the TEG fabrication, eight TE chips, each with dimensions of 3 mm \times 3 mm \times 10 mm and consisting of Sb-doped n -Mg₂Si prepared by a plasma-activated sintering process, were assembled such that two chips were connected in parallel, and four pairs of these were connected in series on a footprint of 46 mm \times 12 mm. The measured power generation characteristics and temperature distribution with temperature differences between 873 K and 373 K are discussed.

Key words: Mg2Si, thermoelectric generator, stress analysis, output power evaluation

INTRODUCTION

 n -Type magnesium silicide (Mg₂Si) is one of the candidate thermoelectric (TE) materials for operation in the temperature range from 600 K to 900 K. Because of its good TE properties $(ZT \approx 1),^{1-7}$ nontoxicity, naturally abundant constituent elements Si and Mg, and low density (\sim 2 g/cm³), Mg₂Si is in demand for practical thermoelectric generator

 (TEG) applications.^{[8,9](#page-9-0)} One of the main applications is in utilizing automotive waste heat, in which, because of the brittleness of Mg_2Si , there is a risk of failure of the TEG due to vibration from the engine. To prevent the TEG from being damaged or destroyed by external forces originating from vibrations and/or external stress, one needs: (i) a modified TEG structure, and/or (ii) improvement of the bending strength of Mg_2Si . In this work, we examine the mechanical stability of an unconventional Mg2Si TEG structure. Generally, TEGs Received June 30, 2013; accepted September 20, 2013;
have a plate-like shape and the TE chips are held (Received online October 19, 2013)

published online October 19, 2013)

vertically in compression between a heat source and a heat sink.¹⁰ However, there is the possibility of shear failure under horizontal loads caused by vibration, thermal stress, unintentional stress, etc. Thus, in this work, we vary the angle θ between the TE chips and the heat sink. We propose an unconventional TEG structure which has a smaller θ than typical TEGs. The external force tolerance of various Mg2Si TEG structures was analyzed by a finiteelement method (FEM) using the ANSYS code. The structure most robust to horizontal stress was found by the FEM stress analysis, and a TEG was assembled based on this. The power generation properties of this TEG were evaluated.

MG2Si TE CHIP EVALUATION

To prepare for the evaluation of the TEGs, the mechanical and TE properties of the Mg_2Si TE chips were measured. First, 0.5 at.% Sb-doped Mg2Si TE chips with and without Ni electrodes were fabricated, and the mechanical and TE properties were evaluated.

TE Chip Fabrication

For the starting material, polycrystalline Mg_2Si was fabricated by an all-molten synthesis process by Yasunaga Co. Ltd. using Mg (Nippon Thermochemical, 3 N, 1.4 mm \times 0.5 mm), Si (Memc Electronic Materials, 6 N+, under 4 mm), and Sb (Electronics and Materials, 6 N, under 5 mm). The obtained polycrystalline Mg₂Si was pulverized to 25 μ m to $75 \mu m$ powder using an alumina mortar in air ambient. The obtained Mg_2Si powder and Ni powder (Kojundo Chemical Laboratory, 3 N, 2 μ m to 3 μ m) were placed in a graphite die as shown in Fig. 1a, and sintered simultaneously at 1123 K for 10 min at pressure of 30 MPa in Ar (0.06 MPa) ambient. The sintered samples were cut using a wire saw, and 3 mm \times 3 mm \times 10 mm TE chips were obtained as shown in Fig. 1b. The thickness of both the top and bottom Ni electrodes was 200 μ m.

The variation in resistance of the TE chips was evaluated at room temperature. The resistance of each chip, R_{chip} , was measured using a Battery HiTester 3561 (Hioki) with a four-terminal probe 9772 (Hioki). The average and standard deviation of R_{chip} for 66 samples were 4.65 m Ω and 0.21 m Ω , respectively.

Characterization of the Mechanical Properties and FEM Analysis

The Young's modulus of the sintered 0.5 at.% Sb-doped Mg2Si was measured by a nanoindentation method using a nanohardness tester (CSM Instruments). The applied load, Poisson's ratio, and the number of measurement points were 10 mN, 0.3, and 8, respectively. The average and standard deviation of the Young's modulus were measured as 117.6 GPa and 1.5 GPa, respectively.

Fig. 1. (a) Sintering conditions. (b) Resulting 3 mm \times 3 mm \times 10 mm TE chip with Ni electrodes.

Table I. Conditions for the three-point bending test: (a) JIS R1601, (b) this work

To predict the durability of the TEG under external stress, tensile strength measurements of the sintered Mg_2Si are needed. Generally, the tensile strength of brittle materials such as Mg_2Si is smaller than the compressive strength, and the stress–strain diagram is linear. Thus, to understand the bending failure of the Mg_2Si TE chip, only the maximum tensile stress is considered. Thus, a three-point bending test was carried out using a Legacy 4442 electromechanical materials testing machine (Instron). Japanese Industrial Standard (JIS) R1601 defines the test conditions for the threepoint bending test as presented in Table Ia .^{[11](#page-9-0)} This standard is harmonized with ISO $14704:2008.¹²$ $14704:2008.¹²$ $14704:2008.¹²$ If the sample size is different from that specified in JIS R1601, the ratio of the length to thickness of the sample and the amount of chamfer should be greater than or equal to 5 and less than or equal to 1/10th of the sample thickness, respectively. In this work, these criteria were satisfied, as shown in Table [I](#page-1-0)b. The average and standard deviation of the bending strength obtained on six samples were 78.9 MPa and 25.0 MPa, respectively, thus the tensile strength is considered to be 78.9 MPa.

Estimation and Measurement of the Output Power of the Mg2Si TE Chip

The TE properties and output power of the Mg_2Si TE chip were evaluated to ascertain the loss in output power after assembling the TEG.

First, the Seebeck coefficient (α) and electrical conductivity (σ) over the temperature range from 327 K to 841 K were measured using a ZEM-II (Ulvac), as shown in Fig. 2. Approximate curves were also fitted to the measured values. These can be used to evaluate the contact resistance between the electrode and Mg_2Si , make comparisons between the estimated and measured output power, etc.

The estimated α and σ are given below:

$$
\alpha_{\rm Mg_2Si}~(\mu V/K) = 9.26 \times 10^{-5} T^2 - 0.284 T - 7.86,~(1)
$$

$$
\sigma_{Mg_2Si}~(S/m) = 0.431T^2 - 830T + 4.90 \times 10^5.~~(2)
$$

The resistance of the TE chip, which is not included in the contact resistance between the electrode and the Mg_2Si , was estimated from the following equation:

$$
R_{\rm chip_est.} = \frac{1}{\sigma_{\rm Mg_2Si}} \frac{L_{\rm Mg_2Si}}{S_{\rm Mg_2Si}},\tag{3}
$$

where σ_{Mg_2Si} is the electrical conductivity at 300 K estimated using Eq. 2, L_{Mg_2Si} is the length of the TE chip without the Ni, and S_{Mg_2Si} is the cross-sectional area of the chip, taking the values 2.80×10^5 S/m, 9.6 mm, and 9 mm^2 , respectively. The electrical

Fig. 2. Measured and estimated Seebeck coefficient and electrical conductivity.

resistance $R_{\text{chip_est.}}$ calculated using Eq. 3 is $3.82 \text{ m}\Omega$. As mentioned above, the measured average resistance $R_{\text{chip_meas.}}$ is 4.65 m Ω , thus the difference between $R_{\text{chip_meas.}}$ and $R_{\text{chip_est.}}$ is 0.83 mΩ. This discrepancy is due to the contact resistance at the interface between the electrodes and the $Mg_2Si.$ ¹

The output power curve of the Mg_2Si TE chip was measured as shown in Fig. [3](#page-3-0). The measurements were done with temperature differences (ΔT) ranging from 100 K to 500 K (hot-side temperature T_h of 473 K to 873 K in steps of 100 K; cool-side temperature T_c of 373 K) and a pressure of 0.5 MPa on 15 mm \times 15 mm Ni plates. For these measurements, the dimensions of the Mg_2Si TE chip were $3 \text{ mm} \times 3 \text{ mm} \times 10 \text{ mm}$, the length of the Mg₂Si part was 9.6 mm, and the thicknesses of the top and bottom Ni electrodes were 0.2 mm, respectively. For thermal and electrical insulation, internally and around it, the TE chip was surrounded by a ceramic fiber material (1260 blanket, Isolite Insulating Products, $\kappa = 0.07$ W/m-K to 0.12 W/m-K at 673 K to 873 K).^{[14](#page-9-0)} The values obtained for the open-circuit voltage $V_{oc_est.}$, the resistance of the TE chip $R_{\rm chip_est.}$, and the maximum output power $P_{\rm max_est.}$ were compared with the estimated values. $V_{oc_est.}$ was calculated by integrating Eq. 1 over T from T_c to each T_h value. The Seebeck effect of Cu was ignored because it is much smaller $(1.94 \mu\text{V/K}$ to $5.23 \mu\text{V/K}$ at 300 K to 900 K)^{[15](#page-9-0)} than that of Mg₂Si. The calculation of $R_{\text{chip_est.}}$ was carried out using the following equation with the assumption that the temperature gradient from the top (T_h) to the bottom (T_c) was constant along the length:

$$
R_{\text{chip_est.}} = \frac{1}{\frac{\int_{T_c}^{T_h} \sigma_{\text{Mg}_2\text{Si}} dT}{T_h - T_c}} \frac{L_{\text{Mg}_2\text{Si}}}{S_{\text{Mg}_2\text{Si}}},\tag{4}
$$

Fig. 3. Schematic side view illustrating the output power measurement for the Mg₂Si TE chip.

	$\boldsymbol{V_{oc}}$			$R_{\rm chip}$				P_{\max}		
$\varDelta T$ (K) Contract Contract Contract	Meas. (mV)	Est. (mV)	Meas./ Est.	Meas. $(m\Omega)$	Est. $(m\Omega)$	$Meas. - Est.$ $(m\Omega)$	Meas./ Est.	Meas. (mW)	Est. (mW)	Meas./ Est.
0 at RT			—	4.30	3.82	0.48	1.13			
100	9.64	11.2	0.864	5.35	4.94	0.41	1.08	4.35	6.29	0.691
200	21.5	24.3	0.886	6.06	5.47	0.59	1.11	19.0	26.9	0.706
300	35.6	39.2	0.909	6.73	6.04	0.69	1.11	49.5	63.5	0.779
400	51.4	55.7	0.923	7.43	6.61	0.82	1.12	88.9	117	0.759
500	68.7	73.6	0.934	8.25	7.17	1.08	1.15	143	189	0.757

Table II. Measured and estimated V_{oc} , R_{chip} , and P_{max} values

where σ_{Mg_2Si} was obtained from Eq. [2.](#page-2-0) The length, $L_{\text{Mg}_2\text{Si}}$, and cross-sectional area, $S_{\text{Mg}_2\text{Si}}$, of the chip were 9.6 mm and 9 mm^2 , respectively. Values of $P_{\text{max}_\text{est.}}$ for each ΔT were obtained from $V_{\text{oc}_\text{est.}}/2$ and $I_{\rm sc_est.}/2 = V_{\rm oc_est.}/2R_{\rm chip_est.}$, where $P_{\rm max_est.}$ was ${\rm calculated\,\, from\,\,}P_{\rm max_est.}^{-} = \bar{V}_{\rm oc_est.}^{2}/4R_{\rm chip_est.}$

Table II presents the results of the measured and estimated V_{oc} , R_{chip} , and P_{max} values. For V_{oc} , the measured values are less than the estimated ones for all ΔT . It seems that the actual ΔT is smaller than the preset ΔT because of some temperature loss between the heat source/heat sink and the Ni plates caused by the thermal contact resistance. At larger ΔT , the difference between the estimated and

measured values becomes smaller. This seems to be due to a reduction in the thermal contact resistance, because as the temperature of the interface increases, the thermal conductivity of the air increases.^{[16](#page-9-0)} Regarding R_{chip} , the difference between the values (measured $-$ estimated) increases with increasing ΔT , indicating that the contact resistance between the Ni electrode and the Mg₂Si increases with ΔT . However, it is interesting to note that the ratio of the values (measured/estimated) is similar for all the ΔT values. This suggests that the contact resistance increases with temperature difference in the same way as the resistivity of the Mg_2Si . For P_{max} , the difference between the measured and

Fig. 4. The models for the stress analysis. The Cu blocks of the TEG are considered to be (a) rigid bodies, and (b) deformable bodies.

Table III. Dimensions of the elements and mechanical properties of the materials

Material	Height (mm)	Width (mm)	Young's Modulus (GPa)	Poisson's Ratio		
the contract of the contract of the Cu		(Model dependent)	117^{17}	0.33^{17}		
Mg_2Si	9.6	$3.0\,$	118	0.30		
Ni	$0.2\,$	$3.0\,$	200^{18}	0.31^{18}		

estimated values reduces with increasing ΔT due to the reducing difference between the measured and estimated V_{oc} values.

EXAMINATION OF MG₂Si TEG

TEG Design and Stress Analysis

Generally, a TEG has a plate-like structure and the TE chips stand vertically on the substrate. If the chips are Mg_2Si , which is a typical brittle material, being tough against compressive and weak against tensile stress, horizontal forces on the substrate are problematic. When TEGs are utilized for automotive waste heat applications, they are stabilized by mechanically pressing the TEG between the heat source and the heat sink. Even so, vibration and/or thermal expansion of the substrate can be severe for the TE chips.

Thus, an unconventional structure is proposed to reduce the tensile stresses on the Mg_2Si TE chips. As shown in Fig. 4, the angle θ between the TE chips and the bottom Cu block is different from the typical right angle, so that the horizontally directed force becomes a compressive force on the TE chips. In addition, this TEG is composed only of $n\text{-Mg}_2\text{Si}$ TE chips in order to reduce the risk of device failure due to the difference in thermal expansion between p - and n -type TE chips. In this paper, we consider the two-dimensional (2D) case as a preliminary study.

Attention was focused on the θ dependence of the external horizontal load resistance of the proposed TEG. Analysis of the TEG using the FEM in the ANSYS code was carried out. Structural analysis of the TEG model under a single horizontal load led to the optimal geometry for avoiding brittle fracture of the chips. This may be considered as a first step in a general mechanical analysis, which would also include thermal stress and vibration.

Figure 4a shows the two kinds of geometry considered for the TEG. The Cu blocks of the TEG are considered to be (a) rigid bodies, and (b) deformable bodies. The former is to understand the effect of the angle dependence, and the latter considers not only the angle dependence but also the strain in the Cu blocks. The dimensions of the elements and the mechanical properties of the materials are presented in Table III. Poisson's ratio of Mg_2Si is assumed to be 0.3, since Mg_2Si is considered to be isotropic. The mesh size is 0.2 mm^2 square, and the mesh is built from eight-node quadratic elements. A detailed description of the mesh size and the observation points for the principal stress on the TE chips is reported in the Appendix. The external load F is 65 N.

Figure [5](#page-5-0) shows the results of the analysis of the principal stress distribution when the Cu blocks of the TEG are considered to be (a) rigid bodies, and (b) deformable bodies. Where the principal stress is regarded as being tensile, smaller stress is better for the TEG. Figure [6](#page-5-0) shows the maximum principal stress on the Mg_2Si when the Cu blocks of the TEG are considered to be (a) rigid bodies, and (b) deformable bodies.

When the Cu blocks are regarded as being rigid, the maximum principal stress becomes smaller as the angle becomes lower as shown in Figs. [5a](#page-5-0) and

Fig. 5. Principal stress distribution when the Cu blocks of the TEG are considered to be (a) rigid bodies, and (b) deformable bodies.

6a. However, elastic deformation of the Cu blocks should be considered for a practical situation. Figures 5b and 6b show the results when there is elastic deformation of the Cu blocks. These results do not show the same tendencies as Figs. 5a and 6a. The analytical results show that, in the Cu blocks, bending stresses appear for θ less than 45°. Regarding the 75° , 60° , 30° , and 15° angles, other models in which the width of the bottom Cu block was increased in the x direction were also analyzed to see how this affected the principal stress on the TE chips. When the width of the Cu block was increased by 10 mm in the x direction, the principal stresses for the 30° and 15° angle chips were less than 11 MPa and 15 MPa, respectively. It seems that the Cu block was less deformed by the load due to the increased width. These stress values are near to the value of 12.1 MPa for the 45° angle chip. However, this solution is inconvenient because, the greater the width, the smaller the output power density. Regarding the 60° and 75° angled chips, no reduction in the principal stress was observed when the width was increased. Thus, the 45° geometry seems to be the most appropriate TEG structure.

Fig. 6. Maximum principal stress on the Mg₂Si when the Cu blocks of the TEG are considered to be (a) rigid bodies, and (b) deformable bodies.

TEG Assembly

A TEG device with $\theta = 45^{\circ}$, the value indicated by the FEM analysis to be the most resistant against horizontal stress, was assembled. Figure [7a](#page-6-0) shows a photograph of a unit of the TEG component. Two Mg2Si TE chips in parallel support a small and a large Cu block, which are for the heat-source side and the heat-sink side, respectively. The chips and the metals are joined by a silver braze (Ag:Cu:Zn: Sn = 56:22:17:5). A Cu wire $(0.5 \text{ mm} \times 4 \text{ mm})$ is connected to the hot side of the Cu block by a silver braze. This wire is connected to the next unit in a series connection. All the metal parts were Ni plated to protect them from oxidation. Figure [7](#page-6-0)b shows the assembled TEG composed of four units in series. As shown in this figure, four soldered wires $(I+, V+, I-,$ V -) are connected for output power measurements. T_{mh} and T_{mc} show the positions at which temperature measurements on the heat-source and heat-sink sides were made. The unit heights of these were matched by #800 grinding. It is possible to put 16 TEG ($\theta = 45^{\circ}$) units on the 5 cm \times 5 cm heat sink.

Output Power Measurements

The output power and heat flow of the assembled TEG were measured as shown in Fig. [8.](#page-6-0) The heat source/TEG and TEG/heat sink thermal interfaces were filled with thermal interface material to improve the thermal conduction and electrical insulation. The heat source/TEG interface was filled with boron nitride (BN) paste, and the TEG/heat sink interface was filled with 60 μ m polyurethane sheet (TSU-700H, Toyo-Chem, $\kappa = 3$ W/m-K at RT).^{[19](#page-9-0)} Then, for heat insulation, a ceramic fiber material (1260 blanket) was used internally and around the TEG. The temperatures of the heat source, $T_{\rm h}$, heat sink, $T_{\rm c-1}$, the TEG hot side, $T_{\rm mh}$, and the TEG cool side, T_{mc} , were measured using type K sheath thermocouples ($\phi = 1$ mm), where T_{mh}

Fig. 8. Schematic illustration of the output power measurement setup for the TEG.

and $T_{\rm mc}$ are given by the averages of $T_{\rm mh\text{-}1}$ and $T_{\rm mh\text{-}2}$ and $T_{\text{mc-1}}$ and $T_{\text{mc-2}}$, respectively. The detailed conditions of the TEG evaluation are described in Table [IV.](#page-7-0) The TEG output power was measured using a 6242 (ADCMT). The heat flux, $Q(W)$, from the TEG to the heat sink was calculated using Fourier's law of thermal conduction as follows: 20 20 20

$$
Q(W) = \frac{\kappa_{Cu}(T_{c-2} - T_{c-3})S}{L},
$$
 (5)

where κ_{Cu} is the average thermal conductivity of pure Cu under a temperature gradient between T_{c-2}

and $T_{\rm c\text{-}3}$.^{[21](#page-9-0)} S and L are the cross-sectional area of the heat sink at T_{c-2} , and the distance between T_{c-2} and T_{c-3} , respectively. The TE efficiency at the maximum output power $\eta_{P_{\text{max}}}$ (%) was calculated from $\eta = P_{\rm max}/(P_{\rm max}+Q)\times 100.$

Regarding the estimation, the estimated TEG output power at the measured T_{mb} and T_{mc} , and at the ideal ΔT (=873 – 373 K) was calculated as follows: $V_{oc_est.}$ was calculated by integrating Eq.[1](#page-2-0) over T from T_{mc} to T_{mh} , and the TEG resistance, $R_{\text{TEG-est.}}$, was calculated from the equation below:

$$
R_{\text{TEG_est.}} = U \times (R_{\text{Mg}_2\text{Si}} + R_{\text{CuHot}} + R_{\text{CuCool}} + R_{\text{CuWire1}}) + R_{\text{Wire2}}
$$
\n
$$
= U \times \left(\frac{1}{\int_{T_c}^{T_b} \frac{L_{\text{Mg}_2\text{Si}}}{\sigma_{\text{Mg}_2\text{Si}}} + \rho_{\text{Cu}}^{T = T_{\text{mh}}} \frac{L_{\text{CuHot}}}{S_{\text{CuHot}}} + \rho_{\text{Cu}}^{T = T_{\text{me}}} \frac{L_{\text{CuCool}}}{S_{\text{CuCool}}} + \rho_{\text{Cu}}^{T = T_{\text{mh}} - T_{\text{me}}} \frac{L_{\text{CuWire1}}}{S_{\text{CuWire1}}} \right) + R_{\text{Wire2}}, \tag{6}
$$

Fig. 9. Output power curves: (a) measured, (b) estimated using the measured ΔT (=T_{mh} - T_{mc}), and (c) estimated using the ideal ΔT .

where U is the number of units. In this study, a four-unit TEG was assembled, i.e., $U = 4$. The electrical conductivity of Mg₂Si, σ_{Mg_2Si} , is given by Eq. [2](#page-2-0). $L_{\rm Mg_2Si}$ and $S_{\rm Mg_2Si}$ are the length and crosssectional area of the Mg₂Si chip, respectively. ρ_{Cu} is the temperature-dependent electrical resistivity of pure Cu.^{[21](#page-9-0)} L_{Cu} and S_{Cu} are the length and cross-sectional area of the Cu in the direction of the current, respectively. The subscripts ''Hot,'' "Cool," and "Wire1" refer to parts of the TEG, and R_{Wire2} is a wire resistance which is independent of the number of units. The maximum output power, $P_{\rm max_est.},~~{\rm was}~~{\rm calculated}~~{\rm from}~~P_{\rm max_est.}=\bar{V}_{\rm oc_est.}^2/2$ $4R_{\text{TEG}_\text{est.}}$. The thermal contact resistances $R_{\text{tc-h}}$ (between the heat source and the hot side of the TEG) and $R_{tc,c}$ (between the cool side of the TEG and the heat sink) were calculated from the following equations:

$$
R_{tc_h} = (T_h - T_{mh})/Q,
$$

\n
$$
R_{tc_c} = (T_{mc} - T_{c-1})/Q.
$$
\n(7)

Figure 9 and Table [V](#page-8-0) show the TEG output power curve and the various measurement results, respectively. (a), (b), and (c) are the measured values, the values estimated using the measured ΔT $(=T_{mh} - T_{mc})$, and the values estimated using the ideal ΔT (= 873 – 373 K), respectively.

The measured P_{max} , power density, heat flux (Q) , and TE efficiency (η) at P_{max} were 696 mW, 1.26 kW/m², 96.7 W, and 0.71%, respectively. Since it is possible to put 16 TEG units on the heat sink, a potential maximum output power of 2.78 W can be obtained.

The measured value of P_{max} (a) is 23% smaller than the value estimated from the measured ΔT (b). This seems to be due to the additional 15.2% in the measured resistance compared with the estimated resistance calculated from $(R_{\text{TEG}}_{\text{meas.}} - R_{\text{TEG-est.}})/$ $R_{\text{TEG}_{\text{est}}},$ which is greater than the 5.5% reduction in the measured value of V_{oc} compared with the $\text{estimated} \quad \text{value} \quad \text{calculated} \quad \text{from} \quad (V_{\text{oc_meas.}} V_{\text{oc_est.}}/V_{\text{oc_est.}}$ Here, the ratio between the measured and estimated resistances, $R_{\text{meas}}/R_{\text{est.}} = 1.15$, is the same as that of a single TE chip given in Table [II](#page-3-0), which is considered to be due to the contact resistance between the Mg2Si and the Ni electrodes. This indicates that the difference between the estimated and measured resistances is due to this contact resistance, and did not arise as a result of assembling the TEG.

Next, we consider the thermal contact resistances to the TEG. The thermal contact resistances on the hot $(R_{\text{tc hot}})$ and cool sides $(R_{\text{tc cool}})$ of the TEG are 0.71 K/W and 0.16 K/W, respectively. Thus, R_{tc_hot} is 4.4 times greater than $R_{\text{tc cool}}$. Here, the area at the interface between the TEG and the heat sink is 420 mm^2 , which is three times larger than the area of the interface between the TEG and the heat source, which is 140 mm² . Thus, increasing the area on the hot side of the TEG would reduce R_{tc_hot} . If ideal values, i.e., negligibly small values, for $R_{\rm tc_hot}$, $R_{\rm tc_cool}$, and the contact resistance between the Mg_2Si and the Ni can be achieved, then a P_{max} of 1323 mW for the TEG could be obtained, as shown in Fig. 9 and Table [Vc](#page-8-0).

Table V. TEG evaluation results

Fig. 10. (a) Conditions for the analysis of a single Mg2Si TE chip. (b) Comparison between the theoretical solution and the mesh-size-dependent FEM solution.

CONCLUSIONS

An n -Mg₂Si TEG with an unconventional structure, designed to mitigate the stress in the TEG due to external forces, is proposed in this work. First, the TE and mechanical properties of the TEG components were evaluated. Then, the unconventional TEG structure, comprising inclined TE chips, was designed with the aid of ANSYS FEM analysis code, using the measured mechanical properties of Mg_2Si . Several inclinations of the TE chips were considered to find the geometry that best mitigated the stress in the chips. The angle between the Cu heat sink and the TE chips was varied from 0° to 90° , and a horizontal external load of 65 N was applied to analyze the stress. When elastic deformation of the Cu parts of the TEG was taken into consideration, the geometrical configuration that was most

resistant to the applied force was that with chips at an angle of 45° to the Cu heat sink. A $\rm{Mg_2Si}$ TEG with 45° angled chips was assembled, and the measured P_{max} , power density, heat flux, and TE efficiency at P_{max} were 696 mW, 1.26 kW/m², 96.7 W, and 0.71%, respectively. The estimates made for this TEG indicate that improving the thermal contact between the TEG and the heat source and reducing the electrical contact resistance between the Ni electrode and the Mg_2Si would increase the TE output power.

ACKNOWLEDGEMENTS

This work was partly supported by a Grant-in-Aid for Scientific Research (A) from the Japanese Ministry of Education, Science, Sports, and Culture, and a Grant-in-Aid for JSPS Fellows awarded by the Japan Society for the Promotion of Science. The authors thank Mr. Alvise Miozzo for his helpful discussions and constructive advice.

APPENDIX

FEM Analysis Optimization

To determine the appropriate mesh size and observation points for the maximum principal stress on the meshed domain of the Mg2Si TE chip, FEM results calculated using various mesh sizes were compared with the results from bending theory. $22,23$

First, a 2D analytical FEM model was defined for the Mg_2Si TE chip. As shown in Fig. [10](#page-8-0)a, the width and length of the model were 3 mm and 10 mm, respectively, including the top and bottom 0.2-mmthick Ni layers. The model was meshed with eightnode quadratic elements. Since Mg_2Si is a brittle material, attention was focused on the tensile stress. Thus, only the upper half of the TE chip was considered; the behavior of the lower part is symmetric. The inputted load P was chosen to be 65 N, because the tensile stress at $y = 0.2$ mm (which is a reliable observation point as described below) was larger than the bending strength of 78.9 MPa when P was above 65 N, as shown in Fig. [10b](#page-8-0).

On the other hand, the theoretical stress distribution at $x = 0$ as a function of the parameter y in the TE chip was described by the following equation:

$$
\sigma = \frac{6P(1-y)}{w^3},\tag{8}
$$

where σ (MPa) is the bending stress at position x from the fixed end, $P(N)$ is the load in the x direction at the other end, w (mm) is the width and depth of the chip, and l (mm) is half the length, L , of the chip.

Figure [10b](#page-8-0) shows comparisons between the theoretical solution and the FEM numerical solutions for different values of mesh size. The tensile stress values for each mesh are not observed at the fixed edge; the results for $y > 0.2$ mm are independent of the mesh size, so there is no mesh size dependence beyond the interface between the Mg_2Si and the Ni electrode. Thus, it was decided that the observation

point would be $y = 0.2$ mm. Regarding the mesh size, it was decided to use 0.2 mm^2 in order to decrease the computational load.

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