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Analysis of the Temperature Dependence of the Capacitance–Voltage and Conductance–Voltage Characteristics of Au/TiO_2(rutile)/*n*-Si Structures

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The capacitance–voltage–temperature (C–V–T) and the conductance/angular frequency–voltage–temperature (G/ω–V–T) characteristics of Au/TiO_2(rutile)/*n*-Si Schottky barrier diodes (SBDs) were investigated over the temperature range from 200 K to 380 K by considering the series resistance effect. Titanium dioxide (TiO_2) was deposited on *n*-type silicon (Si) substrate using a direct-current (DC) magnetron sputtering system at 200°C. To improve the crystal quality, the deposited film was annealed at 900°C to promote a phase transition from the amorphous to rutile phase. The C^{-2} versus V plots gave a straight line in the reverse-bias region. The main electrical parameters, such as the doping concentration (N_D), Fermi energy level (E_F), depletion layer width (W_D), barrier height (ϕ_{CV}), and series resistance (R_S), of Au/TiO_2(rutile)/*n*-Si SBDs were calculated from the C–V–T and the G/ω–V–T characteristics. The obtained results show that ϕ_{CV}, R_S, and W_D values decrease, while E_F and N_D values increase, with increasing temperature.

Key words: TiO_2(rutile), DC magnetron sputtering, capacitance–voltage–temperature characteristic, conductance–voltage–temperature characteristic

INTRODUCTION

TiO_2 thin film has been used in many optical and electrical device applications, such as solar cells, optical filters, high-speed memory devices, and antireflection coatings, due to its high refractive index, large bandgap, and high dielectric constant.[1–19] TiO_2 thin films can be prepared by various techniques, such as the sol–gel method,[20–22] chemical vapor deposition,[23] electron-beam evaporation,[24] and DC reactive magnetron sputtering.[25,26] Among these techniques, the DC reactive magnetron sputtering method is widely utilized due to its ability to obtain uniform, dense, and precise stoichiometric TiO_2 thin films. Bulk TiO_2 is a potential candidate because it has different phases, such as anatase, rutile, and brookite, the most common of which are the anatase and rutile phases.[4,6]

Metal–insulator–semiconductor (MIS) structures play an important role in modern device technology. The performance and reliability of these devices depend on various parameters, such as the surface preparation process, the formation of the barrier height and interface states (N_{SS}) at the M–S interface, substrate temperature, applied bias voltage, and R_S.[27–33] Among these, R_S is only effective in the downward curvature region (accumulation region) of the C–V characteristic. Several researchers have studied the electrical characteristics of MS structures with a TiO_2 interfacial insulator layer.[5–8] Altuntas et al.[5] examined the temperature-dependent forward- and reverse-bias I–V characteristics of Au/TiO_2/*n*-Si Shcottky barrier diodes (SBDs). They showed that the obtained ideality factor values decrease, while the values of zero-bias barrier height increase, with increasing temperature. Bengi et al.[6]

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investigated the electrical characteristics of Au/TiO_2/n-Si for both anatase- and rutile-phase TiO_2 at room temperature. It was reported that thermal annealing strongly affects the main electrical parameters. In addition, the leakage current was found to be very sensitive to the annealing temperature, and also the magnitude of the leakage current for the rutile phase is 15 times lower than that obtained for the anatase phase. These results show that the performance of Au/TiO_2/n-Si SBDs can be improved by thermal annealing. Pakma et al.[7] investigated the electrical characteristics of an Al/TiO_2/p-Si structure and reported that the measured C and G/ω were strongly dependent on the bias voltage and frequency and that the effect of R_S on C and G/ω was noticeable at high frequencies. In our previous study,[8] we investigated the temperature-dependent forward- and reverse-bias I–V characteristics of Au/TiO_2(rutile)/n-Si SBDs. The barrier formation at the M–S interface decreases with decreasing temperature, which may be responsible for the intersection of ln(I)–V curves.

It is well known that analysis of the electrical characteristics of MS or MIS devices at room temperature only cannot provide detailed information about conduction mechanisms and barrier formation at the M–S interface. However, the temperature-dependent electrical characteristics of these devices allow us to understand the temperature dependence behavior of the main electrical parameters and the conduction mechanisms. Therefore, in the present study, the first aim is to investigate the temperature dependence of N_D, E_F, W_D, ϕ_{CV}, and R_S obtained from C–V and G/ω–V measurements at 1 MHz. The second aim is to compare with the R_S values obtained from the C–V and the I–V (previous study) measurements.

EXPERIMENTAL PROCEDURES

Au/TiO_2(rutile)/n-Si SBDs were fabricated on (100)-oriented phosphorus-doped n-type polycrystalline Si substrate (diameter 2 inches, thickness 350 μm, resistivity 0.01 Ω-cm). Prior to deposition process, the substrate was cleaned using $CHClCCl_2$, CH_3COCH_3, CH_3OH organic solvents, respectively. After the cleaning step, the substrate was etched in a sequence of H_2SO_4 and H_2O_2, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF and finally rinsed in de-ionized water. (resistivity 18 MΩ-cm).

After the cleaning and etching steps, the substrate was loaded into a DC magnetron sputtering system. When the vacuum reached 10^{-8} mbar, the substrate was heated up to 400°C and sputter-cleaned in pure argon ambient to ensure removal of any residual organics. After the substrate preparation, the substrate was transferred into the deposition chamber to deposit TiO_2 thin film with 1500 Å thickness from a high-purity (99.999%) Ti target, under a specific Ar + O_2 reactive gas mixture (Ar/O_2 = 90/10) controlled by mass flow controllers. During the TiO_2 thin-film deposition, the substrate temperature and the pressure were set to 200°C and 4.2×10^{-3} mbar, respectively, and kept constant. After completion of the deposition, the structure was annealed in a conventional thermal annealing (CTA) system at 900°C to promote a phase transition from the amorphous to the rutile phase.

For electrical characterization, firstly an ohmic back contact was formed by deposition of high-purity (99.999%) Au. Then, the structure was annealed at 400°C to achieve good ohmic contact behavior. Finally, dot-shaped rectifier front contacts (2 mm diameter, 1000 Å thickness) were formed by deposition of high-purity (99.999%) Au at 70°C.

Temperature-dependent C–V and G/ω–V measurements were carried out at 1 MHz by using a HP 4192 A LF impedance analyzer. The temperature was adjusted using a Janis vpf-475 cryostat. The temperature of the structure was always monitored by using a copper–constantan thermocouple close to the structure and measured with a Keithley model 199 dmm/scanner and Lake Shore model 321 autotuning temperature controllers with sensitivity better than ±0.1 K. All measurements were carried out by using a microcomputer through an IEEE-488 AC/DC converter card.

RESULTS AND DISCUSSION

The temperature-dependent reverse- and forward-bias C–V and G/ω–V characteristics of the Au/TiO_2(rutile)/n-Si SBDs at 1 MHz are shown in Figs. 1 and 2, respectively. As seen in Figs. 1 and 2, both the C–V and G/ω–V plots increase with the increasing temperature, especially in the depletion region. The temperature-dependent semilogarithmic forward- and reverse-bias I–V diode plot, which is also shown in the inset of Fig. 1, gives an intersection point at high forward bias voltages (~1.4 V). In addition, it can be seen in Fig. 1 that the C–V plots show a concave curvature behavior in the accumulation region as a result of the effect of R_S and the interfacial insulator layer. At sufficiently high frequencies ($f \geq 1$ MHz), N_{SS} cannot follow the AC signal. In this case, R_S seems to be the most important parameter which causes the electrical characteristics of the structure to be nonideal. To extract the R_S value of the structure, several methods have been suggested in the literature.[33–37] In our calculation, we exploited the method used by Nicollian and Brews.[33] The real R_S of MIS devices can be calculated from the measured capacitance (C_m) and conductance (G_m) in the strong accumulation region at high frequencies (~1 MHz) using the equation

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2}, \tag{1}$$

where C_m and G_m represent the measured capacitance and conductance for any bias voltage.

The values of R_s are calculated by using Eq. 1 and shown in Fig. 3 for various temperatures. The

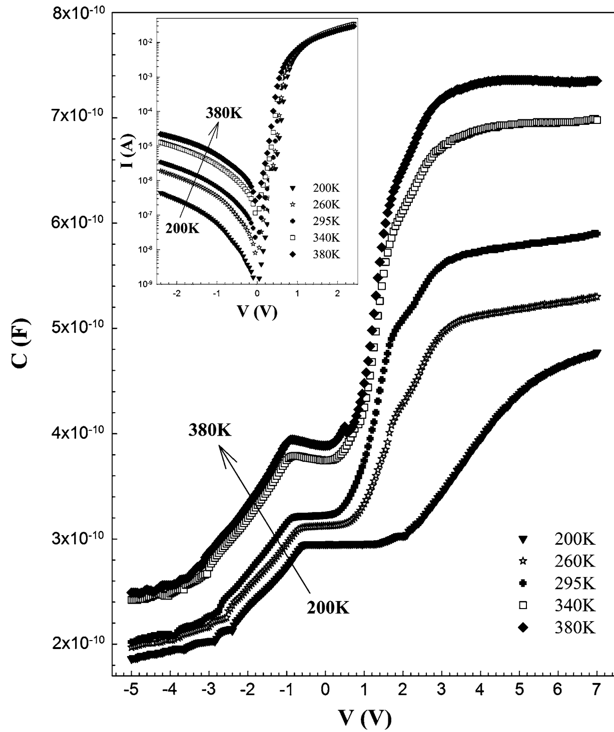

Fig. 1. Temperature-dependent C–V characteristics for Au/TiO_2 (rutile)/n-Si SBDs at 1 MHz, with semilogarithmic plot of the I–V characteristic of the diode for various temperatures in the inset.

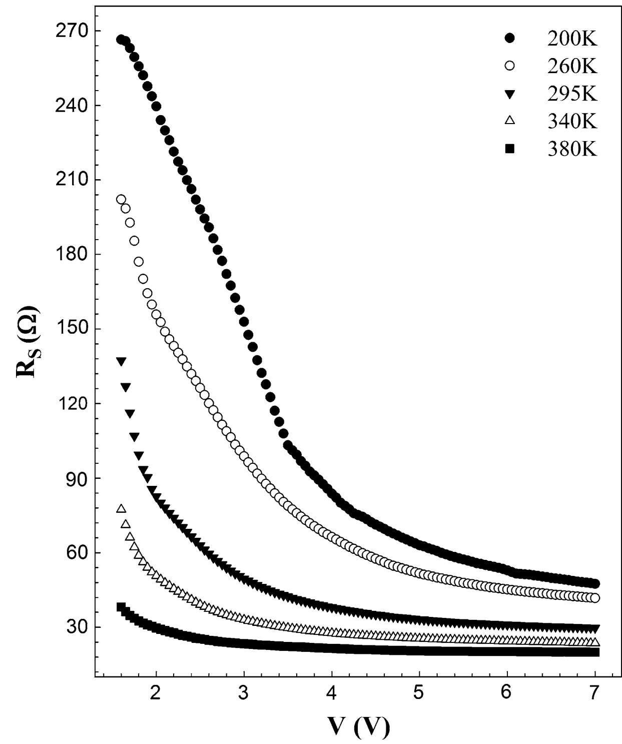

Fig. 3. R_S versus V for Au/TiO_2(rutile)/n-Si SBDs for various temperatures at 1 MHz.

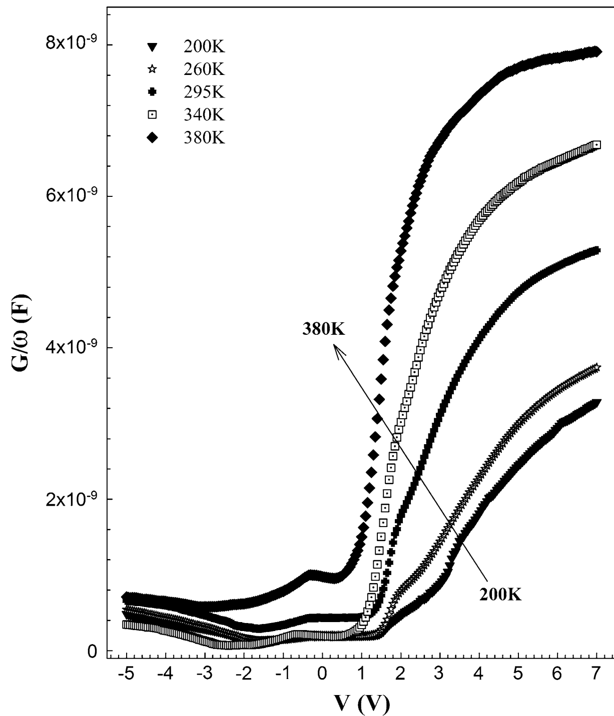

Fig. 2. Temperature-dependent G/ω–V characteristics for Au/TiO_2(rutile)/n-Si SBDs at 1 MHz.

obtained values of R_S are presented in Table I. It can be seen from the table and Fig. 3 that the values of R_S decrease with increasing temperature, indicating that the trap charges have sufficient energy to escape from traps at high temperature. In addition, the series resistance–temperature (R_S-T) plot for various temperatures at the particular voltage range (2.6 V to 3.2 V in steps of 0.1 V) is given in Fig. 4. It can be observed that the voltage dependence of R_S decreases with increasing temperature, since the carriers are frozen out at low temperatures but they move at high temperatures and thus the diode begins conducting at lower voltages. Therefore, the R_S value is nearly independent of voltage at high temperatures. Similar results have been reported in the literature.[31,38–40]

Figures 5, 6, and 7 show the voltage-dependent C, G/ω, and R_S values obtained from the capacitance–temperature (C–T), conductance–temperature (G/ω–T), and R_S–T plots for various applied forward-bias voltages (2 V to 7 V in steps of 1 V) at 1 MHz. It is clearly seen that the values of C and G/ω increase, while the value of R_S decreases, with increasing temperatures for each bias voltage value. The changes in the C, G/ω, and R_S values can be attributed to restructuring of the interface charge at the M–S interface.

The temperature dependence of the C^{-2} versus V characteristics is presented in Fig. 8. As can be seen from Fig. 8, the C^{-2} versus V plot gives a straight line in the reverse-bias region. The depletion-layer capacitance of the diode can be expressed as[29]

Table I. Values of various parameters for the Au/TiO_2(rutile)/n-Si structure as determined from C–V–T and G/ω–V–T characteristics

T (K)	N_D (cm^{-3})	E_F (meV)	ϕ_{CV} (eV)	W_D (cm)	R_S (at 7 V) (Ω)
200	8.98×10^{16}	9.54	0.87	1.60×10^{-5}	47.47
260	7.32×10^{16}	12.62	0.86	1.44×10^{-5}	41.74
295	5.94×10^{16}	14.89	0.80	1.17×10^{-5}	29.75
340	4.79×10^{16}	15.84	0.65	1.11×10^{-5}	23.58
380	4.20×10^{16}	19.39	0.53	0.80×10^{-5}	19.96

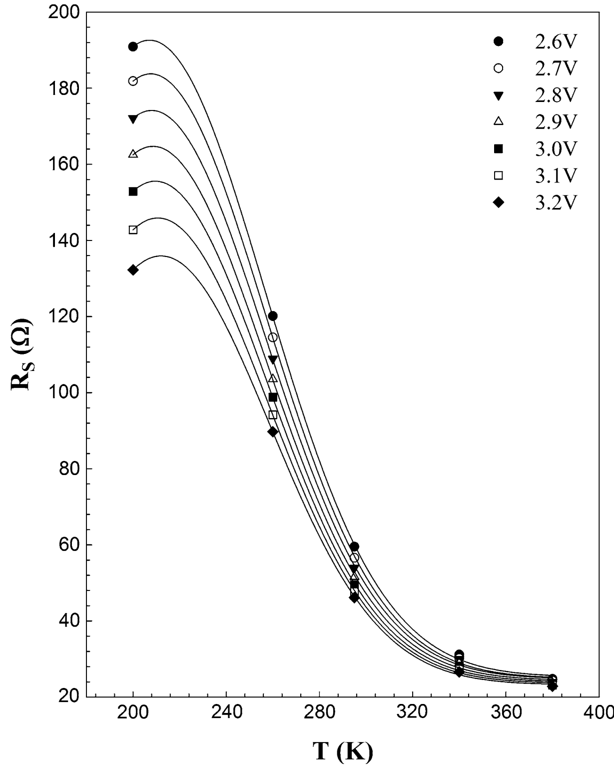

Fig. 4. The temperature dependence of the R_S values of Au/TiO_2(rutile)/n-Si SBDs for particular forward-bias voltage ranges at 1 MHz.

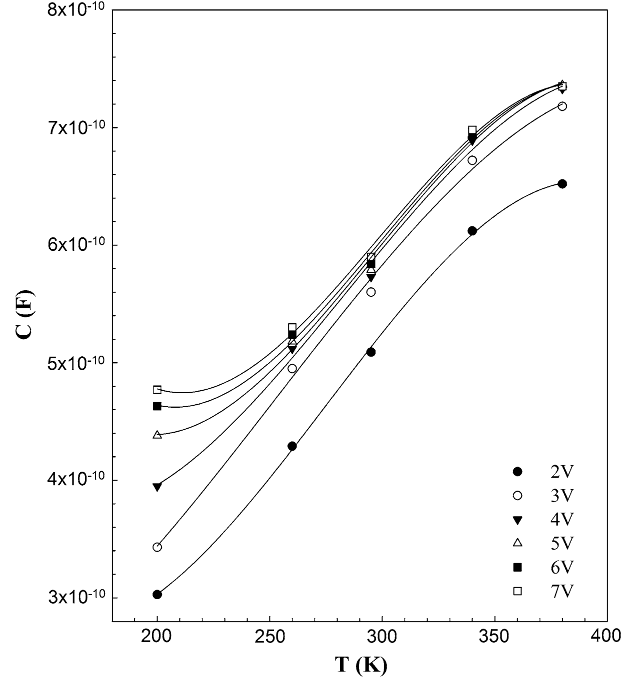

Fig. 5. Temperature-dependent C values of Au/TiO_2(rutile)/n-Si SBDs for various bias voltages at 1 MHz.

$$C^{-2} = \frac{2(V_R + V_0)}{q\varepsilon_s N_D A^2}, \quad (2)$$

where V_R is the reverse-bias voltage and V_O is the built-in voltage at zero bias, which can be determined from the extrapolation of the C^{-2} versus V plot to the bias axis. The main electrical parameters can be calculated at various temperatures from Fig. 8 by using the following equations:

$$V_0 = V_D - \frac{kT}{q}, \quad (3)$$

$$E_F = \frac{kT}{q}\mathrm{Ln}\left(\frac{N_C}{N_D}\right), \quad (4)$$

$$\phi_{CV} = V_0 + \frac{kT}{q} + E_F - \Delta\phi_B, \quad (5)$$

and

$$\Delta\phi_B = \left(\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right)^{0.5}, \quad (6)$$

where V_D is the diffusion potential at zero bias (Eq. 3), N_C is the effective density of states in the semiconductor conduction band (Eq. 4), $\Delta\phi_B$ is the image force barrier lowering (Eq. 5), and E_m is the maximum electric field (Eq. 6). The obtained values of N_D, E_F, W_D, and ϕ_{CV} at different temperatures are presented in Table I. As shown in Table I, the obtained ϕ_{CV} and W_D values decrease, while the values of N_D and E_F increase, with increasing temperature. Similar results have been reported in the literature.[31,38–44]

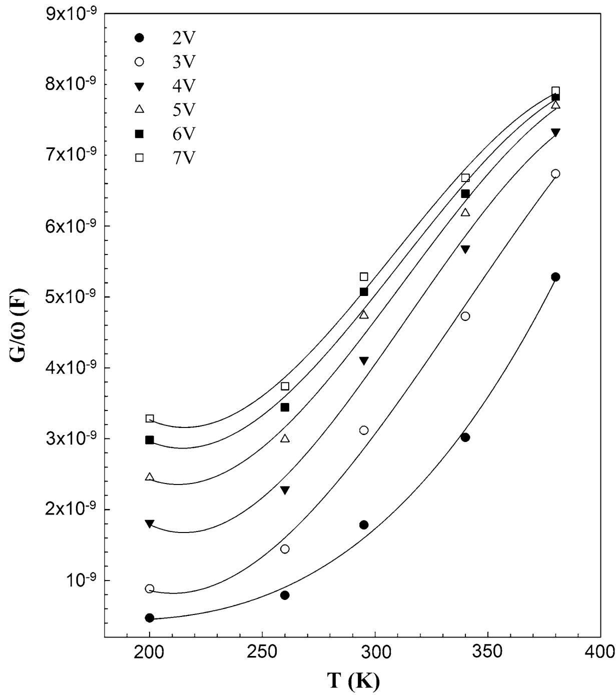

Fig. 6. Temperature-dependent G/ω values of Au/TiO_2(rutile)/n-Si SBDs for various bias voltages at 1 MHz.

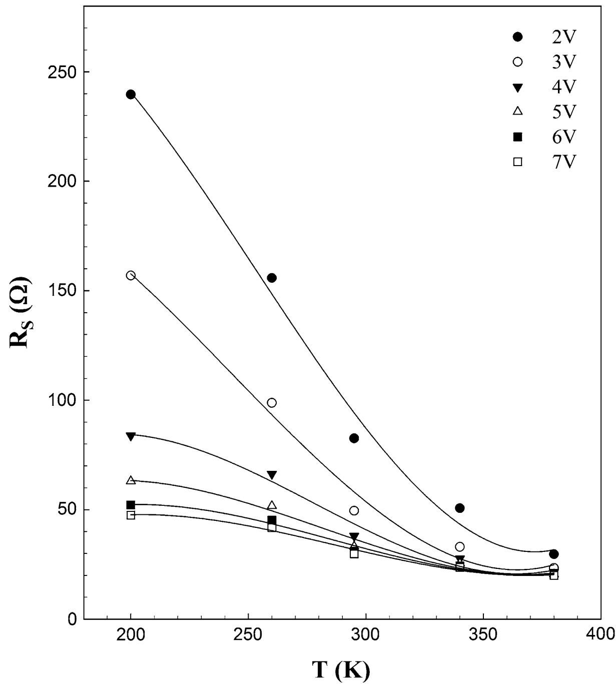

Fig. 7. Temperature-dependent R_S values of Au/TiO_2(rutile)/n-Si SBDs for various bias voltages at 1 MHz.

In summary, in the present study, the temperature-dependent C–V and G/ω–V characteristics of Au/n-Si SBDs with a TiO_2(rutile) interfacial insulator layer were analyzed at 1 MHz. The experimental results show that R_S exhibits the usual behavior of decreasing with increasing temperature,

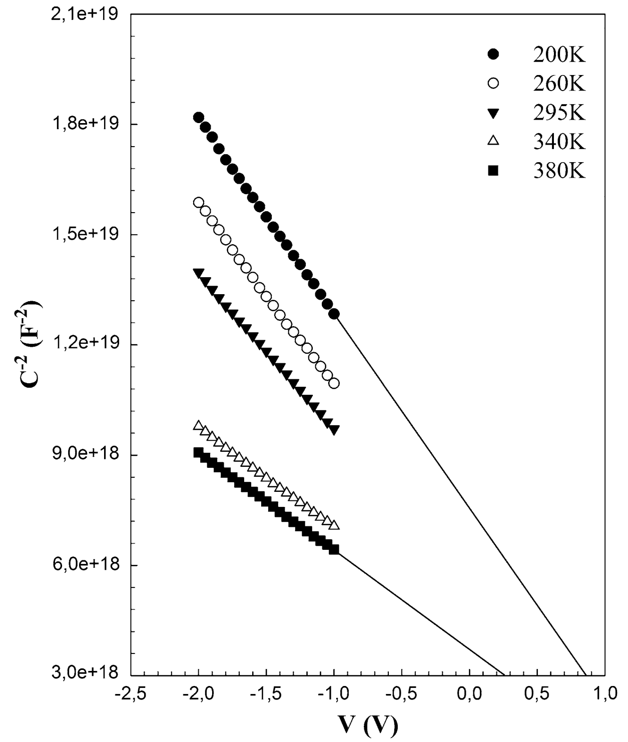

Fig. 8. C^{-2} versus V for Au/TiO_2(rutile)/n-Si SBDs for various temperatures at 1 MHz.

and is nearly independent of voltage at high temperatures. In addition, according to the obtained results, we can deduce that the R_S effect is strong in the accumulation region. On the other hand, in our previous study, experimental results showed that the intersection of I–V curves may be a result of a double Gaussian distribution of barrier inhomogeneities. Since SBDs have different barrier heights for different temperature regions, the current flow through the SBDs will be different, which at first glance is incompatible with the fact that we expect higher current flow for high temperatures. For voltages higher than the crossing point, the current flow for the diode is higher at low temperatures. Thus, R_S shows an unusual behavior of increasing with increasing temperature. As a result, it is clearly seen that R_S is one of the most important parameters for the electrical characteristics of semiconductor devices. Moreover, for both the C–V and I–V characteristics, rutile-phase TiO_2 was found to exhibit suitable device performance due to its lower series resistance.

CONCLUSIONS

The reverse- and forward-bias C–V–T and G/ω–V–T characteristics of Au/TiO_2(rutile)/n-Si SBDs were studied at 1 MHz. The experimental results showed that both the C–V and G/ω–V plots increase with increasing temperature, especially in the depletion region. In addition, we obtained the voltage-dependent

C, G/ω, and R_S values for various applied forward-bias voltages. It is clear that the values of R_S decrease, while the values of C and G/ω increase, with increasing temperatures for each bias voltage value. On the other hand, the obtained values of R_S, ϕ_{CV}, and W_D decrease, while the values of N_D and E_F increase, with increasing temperature. According to the experimental results obtained from the Au/n-Si structure with a rutile-phase TiO_2 interfacial insulator layer, we conclude that it would be possible to use this structure for device applications.

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