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Trapping Time Characteristics of Carriers in a-InGaZnO Thin-Film Transistors Fabricated at Low Temperatures for Next-Generation Displays

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The effect of low-temperature annealing treatment for various durations on the stability of amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors was investigated. By this treatment, IGZO TFTs showed enhanced electrical characteristics and better stability under positive gate bias stress with increasing annealing time up to 18,000 s. For all V_G stresses at different annealing times, the experimentally measured threshold voltage shift (ΔV_{th}) as a function of stress time was precisely modeled with a stretched-exponential function. ΔV_{th} was generated by carrier trapping, not by defect creation. It was verified that the decrease of interface trap state density (N_{it}) and free carriers resulted in the decrease of ΔV_{th} with increasing annealing time. However, the characteristic trapping time of the carriers increased up to 5.3×10^3 s with increasing annealing time to 7,200 s and then decreased, implying that the interface quality between active layer/insulator was deteriorated with further annealing. In this study, successful fabrication of IGZO TFTs by post treatment with optimized duration is demonstrated for flexible display applications.

Key words: Low-temperature thermal treatment, IGZO thin-film transistor, double insulators, trapping time characteristics of carriers

INTRODUCTION

Currently, flexible and transparent electronic devices show the most promise in futuristic technological applications, such as flexible displays, solar cells, touch panels, and wearable devices. According to Nomura et al.,[1] amorphous oxide semiconductors are expected to play a key role in advanced electronics due to their superior electrical performance compared with conventional amorphous silicon and polycrystalline silicon thin-film transistors (TFTs). These a-IGZO TFTs have shown excellent performance in the development of future displays, especially those demanding high mobility (>10 cm^2 V^{-1} s^{-1}), flexibility, and transparency in the visible range.[2]

However, investigations on amorphous oxide TFTs have shown that low-temperature-deposited IGZO TFTs suffer from significant stability problems.[3] To overcome these problems, furnace annealing has been applied at temperatures greater than 300°C.[4] It was reported that the annealing process reduces the tail state defects, rearranges the amorphous structure, and improves the oxygen compensation in nonstoichiometric film.[3] However, annealing temperatures above 300°C make this process unsuitable for flexible substrates. Therefore, a low-temperature annealing process is essential for the development of stable IGZO TFTs

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on flexible substrates. In this study, the influences of annealing time on the performance and stability of IGZO TFTs at the low annealing temperature of 200°C are investigated. This successful manufacture of IGZO TFTs at relative low post treatment temperatures promises simplicity in the fabrication of high-performance devices for flexible displays.

EXPERIMENTAL PROCEDURES

A schematic cross-section view of an IGZO TFT is shown in Fig. 1. It was fabricated using a *p*-type silicon wafer with very low resistivity ($\rho \approx 0.001\ \Omega$ cm) as the gate electrode. A double-layer SiO_2/SiN_x gate insulator with total thickness of 300 nm was fabricated by the inductively coupled plasma (ICP) chemical vapor deposition (CVD) process. Details of the fabrication process can be found elsewhere.[4] As the active layer, an a-IGZO thin film of 100 nm was deposited by direct-current (DC) magnetron sputtering at room temperature. The initial vacuum level was lower than 5×10^{-5} Torr, and the working pressure and DC power density were maintained at 5×10^{-3} Torr and 1.78 W cm^{-2}, respectively, during the sputtering.

For use in flexible displays, the IGZO TFT was post annealed at low temperature of 200°C in air atmosphere using rapid thermal annealing equipment. The annealing time was varied from 600 s to 18,000 s to investigate the influences of thermal energy on the properties of the IGZO and interface. Then, 150-nm silver (Ag) layers were deposited as the source/drain (S/D) electrodes by thermal evaporation at base pressure of 5×10^{-5} Torr in the conventional mask process. The TFT channel width-to-length ratio (*W*/*L*) was fixed at 40. The nonpassivated TFT bottom gate structure with a very thick IGZO active layer (100 nm) was used to investigate the effect of thermal annealing conditions on bias stability. A very thick active layer was used in this study to minimize the influences of field-induced adsorption/desorption of some kinds of molecules (such as oxygen or/and water molecules) on the back channel surface.[5–8] The electrical performance of the TFT devices was characterized using an EL 420C semiconductor parameter analyzer. All *I*–*V* measurements in this study were carried out at room temperature with the gate voltage sweeping rate fixed at 0.21 V/s. The chemical bonding structures of the films were studied by Fourier-transform infrared (FTIR) spectroscopy in the 400 cm^{-1} to 4000 cm^{-1} wavenumber range at 8 cm^{-1} resolution using a Sopra GES5 spectroscopic ellipsometer. Films of 100 nm thickness were used for the analysis.

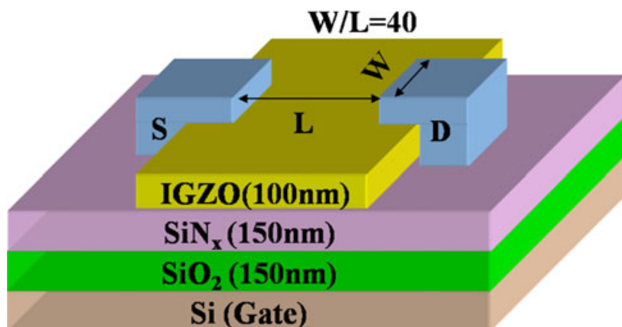

Fig. 1. Schematic cross-section of the a-IGZO-based TFT bottom gate structure with SiO_2/SiN_x gate dielectric on silicon substrate.

RESULTS AND DISCUSSION

TFT bottom gate devices were fabricated using various annealing times with two insulator layers of SiN_x and SiO_2. These two insulator layers were used because the SiN_x layer offers stability[9] while the SiO_2 layer offers high breakdown voltage.[10] Figure 2 shows the transfer characteristics of the TFTs at different annealing times. The drain current (I_D) was measured in a dark box as the gate voltage (V_G) was swept from −5 V to 25 V, with the drain voltage (V_D) fixed at 1 V. The electrical characteristics of the TFTs improved with increasing annealing time, and the best electrical performance was obtained from the device annealed for 18,000 s with the smallest off-current and high on-current as well as the best subthreshold swing (SS).

Detailed electrical properties of IGZO TFTs were obtained for different annealing times, as presented in Fig. 3. V_{th} in the linear region (V_D = 1 V) was calculated by fitting a straight line to the plot of I_D versus V_G according to the following expression for a field-effect transistor:[11]

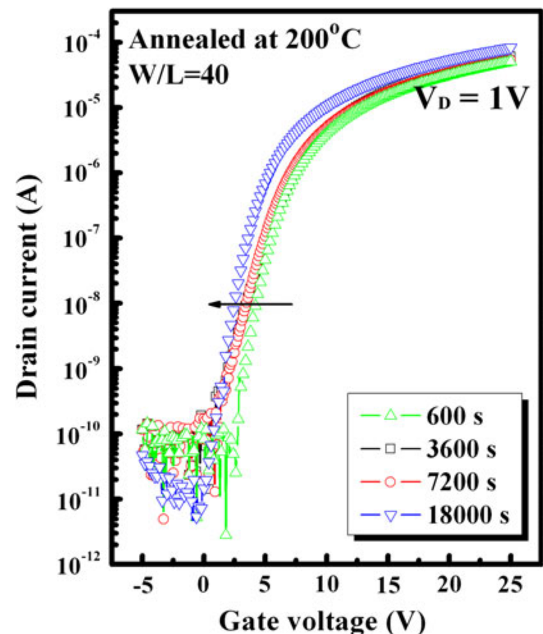

Fig. 2. Transfer characteristics of IGZO TFTs for different annealing times.

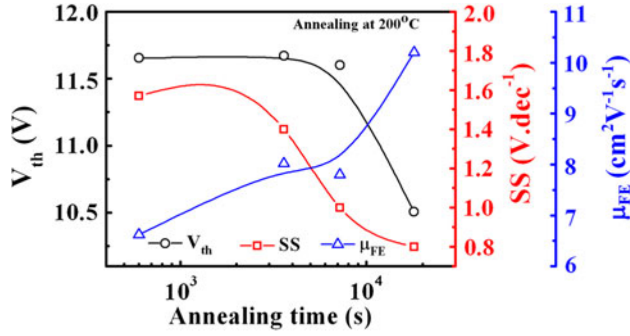

Fig. 3. Evolution of electrical parameters of IGZO TFT with annealing time: threshold voltage, subthreshold swing, and field-effect mobility.

$$I_D = \frac{W}{L}\mu_{FE}C_iV_D(V_G - V_{th}), \quad (1)$$

where W is the channel width, L is the channel length, and C_i is the capacitance per unit area of the gate insulator. Other TFT parameters, such as SS, μ_{FE}, and V_{th}, also proved the beneficial influence of a long annealing process. V_{th} slightly decreased from 11.7 V to 10.5 V while the SS reduced linearly from 1.6 V dec^{-1} to 0.8 V dec^{-1}, whereas μ_{FE} increased with increasing annealing time. The best SS value of 0.8 V dec^{-1}, high mobility of 10.3 cm^2 V^{-1} s^{-1}, and low V_{th} were obtained for the sample annealed for a long time of 18,000 s. The increase in the mobility in the long-time annealed sample can be attributed to the improvement in the structural arrangement of the IGZO layer during treatment. The structure of an amorphous metal is modeled as a dense random packing of metal spheres with occupation of interstitial positions by metalloids.[12] The improvements in SS and V_{th} were related to the reduction in the interface trap density at the interface between the active layer and the insulator. All TFT parameters depend strongly on the defect density at the insulator/semiconductor interface and inside the gate insulator. The defect density at the channel/insulator interface (N_{it}) is related to the SS value by the following relation, assuming the traps are isotropic:[13]

$$N_{it} = \left(\frac{SS\log(e)}{kT/q} - 1\right)\frac{C_i}{q}, \quad (2)$$

where e is the Euler's number (irrational constant), k is the Boltzmann constant, T is the absolute temperature, and q is the charge of an electron. The interface trap states of devices at different annealing times were extracted as 2.48×10^{12} cm^{-2}, 2.23×10^{12} cm^{-2}, 1.88×10^{12} cm^{-2}, and 1.38×10^{12} cm^{-2}, respectively. N_{it} decreased as the annealing time increased, which is consistent with previous study[4] that used various thermal treatment temperatures [room temperature (RT), 200°C, and 350°C].

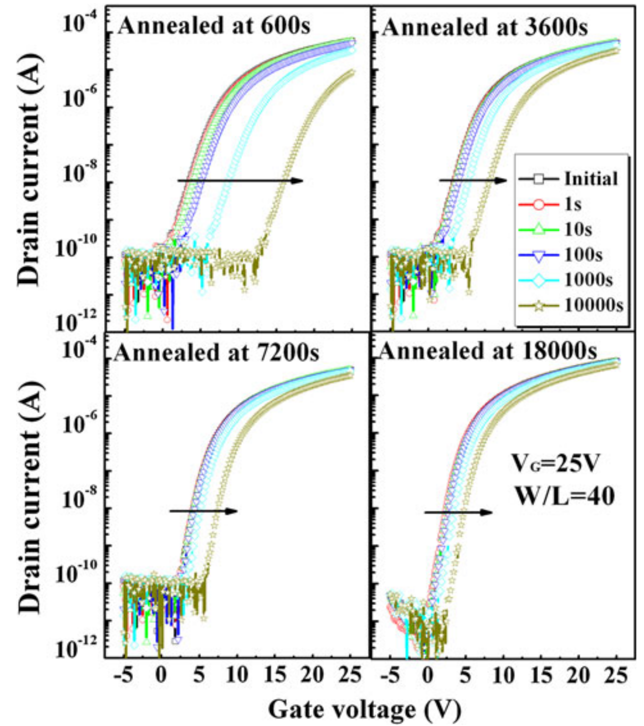

Fig. 4. Stability performance of IGZO TFTs under positive gate bias stress of V_G = +25 V as a function of annealing time.

Figure 4 shows the variations of the I_D–V_G transfer characteristics of the IGZO TFTs during positive gate bias stressing. The DC bias conditions of the positive gate bias were V_G = +25 V and V_D = V_S = 0 V. The bias condition was designed to equalize the gate electric field of each sample. All the samples showed a common behavior in which the I_D–V_G transfer curve shifts in the positive direction to decrease the drain current with increasing stress time. As shown in Fig. 4, increasing treatment time improved the stability of the devices under high bias stress. The shift in the positive direction under positive gate bias stress was due to the generation of defects originating from the creation of dangling bonds or electron trapping near the gate insulator interface. The slopes of the curves did not change much, despite the increase of the bias stress time, indicating that the change of mobility can be ignored. The lack of SS variation indicates carrier trapping in the channel/insulator interface or/and in the insulator bulk region or/and in the deep acceptor-like traps of a channel with negligible creation of defect states. The value of ΔV_{th} corresponds to the number of captured electrons, which is also proportional to the number of trapped states. The positive ΔV_{th} value is therefore explained by trapping of carriers in defect states.

Figure 5 shows ΔV_{th} as a function of time for constant V_G stress of +25 V at various annealing times. The scattered points are the measured ΔV_{th} values, and the dashed lines represent a stretched-exponential function for ΔV_{th}. The stretched-exponential

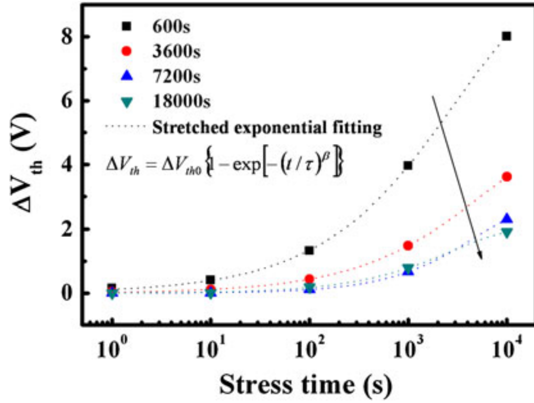

Fig. 5. Time dependence of ΔV_{th} (V_G = 25 V) of devices with different annealing times. The scatters show measured ΔV_{th} values, while the dotted line represents the stretched-exponential model for ΔV_{th}.

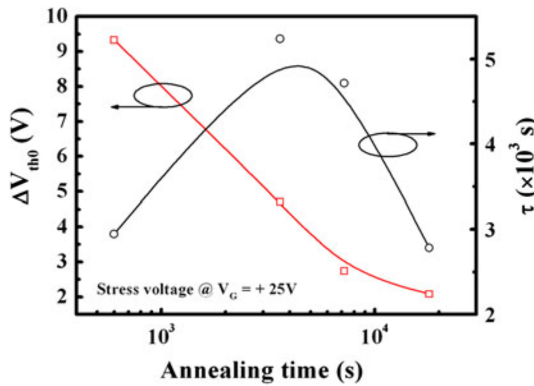

Fig. 6. Time dependence of ΔV_{th0} and the characteristic trapping time of carriers of devices with different annealing times under stress at +25 V.

function was developed to model ΔV_{th} according to the carrier trapping of a-Si:H TFTs.[14] The measured ΔV_{th} values fit well with the stretched-exponential function in Fig. 5, indicating that the carriers were trapped in the interface or bulk dielectric layers with no creation of additional defect states; this result is also consistent with the lack of SS variation with increasing stress time. The stretched-exponential function for ΔV_{th} is described as[14]

$$\Delta V_{\text{th}} = \Delta V_{\text{th0}}\left\{1 - \exp\left[-(t/\tau)^{\beta}\right]\right\}, \tag{3}$$

where ΔV_{th0} is the ΔV_{th} at infinite time, $\tau = \tau_0 \exp(E_\tau/kT)$ represents the characteristic trapping time of carriers, the thermal activation energy is given by $E_a = E_\tau\beta$, β is the stretched-exponential exponent, E_τ is the average effective energy barrier that electrons in the a-IGZO TFT channel need to overcome before they can enter the insulator, and τ_0 is the thermal prefactor for emission over the barrier. The dashed line represents the stretched-exponential model, and the stretched-exponential

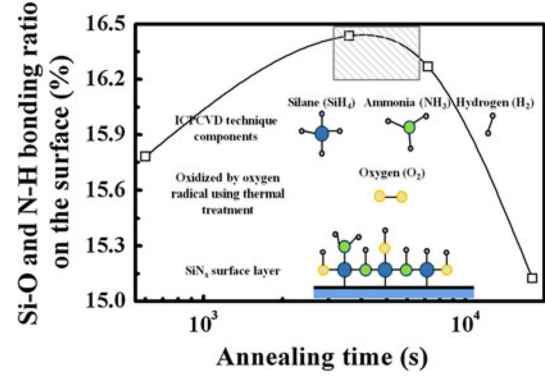

Fig. 7. Evolution of Si–O and N–H bonds in SiN_x sample as a function of annealing time.

parameters are extracted from this model. ΔV_{th0} and the characteristic trapping time of carriers, τ, for the samples subjected to various thermal treatment conditions are presented in Fig. 6 for easy observation.

In Fig. 6, ΔV_{th0} decreases from 9.4 V to ~2.0 V when the annealing time increases to 18,000 s and β is in the range of 0.55 to 0.82. Interestingly, the characteristic trapping time, τ, was modeled as increasing with annealing time from 600 s to 3,600 s and then decreasing with further increase of annealing time. The trapping time represents the ability of a carrier to trap itself inside the insulator: the carrier trapping time is faster at short annealing time than at long annealing time. This implies that, by increasing the annealing time to 3,600 s, the IGZO structure as well as the gate insulator properties are improved, reducing the amounts of dangling bonds and interface traps between the channel and gate insulators. However, further annealing leads to decrease in the carrier trapping time, as shown in Fig. 6. This may be due to deterioration of the interface between the insulator and active layer and needs further investigation.

To study the correlation between the characteristic trapping time under various annealing times and the interface properties, FTIR measurements of the SiN_x/SiO_2 double gate insulators were carried out. As presented in Fig. 7, the surface of the double insulator layers (i.e., SiN_x layer) after deposition and annealing treatment consists of various chemical bonds: Si–O, Si–H, Si–N, N–H, etc. The number of each type of chemical bond (X–Y) was calculated from FTIR spectra through the following equation:[15]

$$X - Y = A\frac{\alpha(\omega)}{\omega}\mathrm{d}\omega, \tag{4}$$

where A is the proportionality constant, α is the absorption coefficient, and ω is the wavenumber. Besides the Si–N bond, different kinds of chemical bonds that reduce the interface trap defects created by unsaturated bonds were present on the SiN_x layer. Therefore, the numbers of Si–O/Si–H and

N–H bonds relate to the characteristic carrier trapping time. As shown in Fig. 7, the calculated Si–O and N–H bond ratios as a function of annealing time revealed that increased annealing time helped to improve the interface quality of the SiN_x layer. The numbers of Si–O and N–H bonds increased with increasing annealing time to 3,600 s and decreased with further treatment; this result is consistent with the characteristic trapping time of carriers. Based on these results, one can say that thermal treatment at low temperatures for various treatment times affects the interface properties of the insulators/active layer of the TFTs in terms of modified numbers of various unsaturated bonds at the interface. Such an effect will improve the stability of IGZO TFTs under high positive gate bias stress. Thermal stress was obtained (data not shown) to confirm the improvement of interface quality under various annealing conditions. Thermal treatment helped to improve both IGZO bulk quality in terms of reducing the V_{th} shift for the thermal stress measurement and enhancing the interface quality between the active layer and gate insulator. The optimum condition for obtaining both a low threshold voltage and a high trapping time of carriers for the IGZO TFT devices was obtained by annealing at 200°C for 7,200 s.

CONCLUSIONS

Bias stress instability of IGZO TFTs was investigated for different thermal treatment times. From the V_G stress, a stretched-exponential model fitted well with the experimentally measured values of ΔV_{th}, indicating that the carriers were trapped in interface trap states and not creating additional defect states. The evolution of chemical bonding on the interface of the insulators/active layer with annealing time controlled the trapping time of the carriers. With annealing time of 7,200 s at a low temperature of 200°C, IGZO TFTs exhibited both low operation voltage ($\sim$2.5 V) and high trapping time of carriers, which are advantageous properties for flexible display applications.

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