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RF Power Effect on the Properties of Sputtered ZnO Films for Channel Layer Applications in Thin-Film Transistors

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ZnO films were processed by radiofrequency (RF) magnetron sputtering under argon gas environment at room temperature, varying the RF power (90 W, 100 W, 150 W, and 200 W), on p-Si/SiO_2 substrates. Structural, morphological, and electrical characteristics of the ZnO films were determined using several experimental techniques, and they showed a clear relationship with the RF power. All the ZnO films exhibited a hexagonal wurtzite polycrystalline structure with (002) preferred orientation. Atomic force microscopy (AFM) revealed the formation of grains or clusters as a result of the accumulation of nanoparticles, and the grain size increased with increasing power. An ascending trend of the root-mean-square surface roughness of the films with increasing power was also observed. ZnO film thickness and refractive index were determined by spectroscopy ellipsometry. In agreement with AFM results, the observed increase of refractive index from 2.15 to 2.44 was the result of improved film compactness on increasing the deposition power. The electrical resistivity ranged from 3.5×10^3 Ω-cm for ZnO film deposited at 200 W to 5×10^7 Ω-cm for that deposited at 100 W. The sputtered ZnO films were employed as the active channel layer in thin-film transistors, and the impact of the deposition power on device performance was studied. As the power was increased, the field-effect mobility increased from ~0.1 $cm^2/V\,s$ to 4.2 $cm^2/V\,s$, the threshold voltage decreased from 33.5 V to 10.7 V, and the I_{on}/I_{off} ratio decreased from 10^6 to 10^2.

Key words: Highly resistive zinc oxide films, thin-film transistor, RF power, magnetron sputtering

INTRODUCTION

Zinc oxide is a wide-bandgap n-type semiconductor (E_g = 3.37 eV) with current electronics applications in thin-film transistors (TFTs), solar cells, varistors, and piezoelectric devices.[1] ZnO films can be obtained by several deposition techniques. One of them, radiofrequency magnetron sputtering, is a well-known technique that produces high-quality polycrystalline ZnO thin films, even at room temperature and without post thermal annealing.[2,3] This characteristic makes ZnO sputtered films compatible with flexible and transparent electronics technology, where low-temperature deposition processes are required.

Depending on their electrical nature, ZnO thin films can be useful either as electrodes, specifically transparent conductive oxides (TCOs), or as active channel layers in TFTs. The first application needs highly conductive, transparent ZnO films ($\rho \approx 10^{-4}$ Ω-cm), which are attained by doping, typically with Al atoms;[4] the second application demands highly resistive ZnO films ($\rho \approx 10^5$ Ω-cm

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to 10^8 Ω-cm).[5,6] Therefore, tuning of the electrical resistivity of ZnO films is an important issue to optimize their performance in specific applications. In particular, for the case of ZnO-based TFTs, the carrier concentration in the ZnO active channel defines the electrical response of the devices. To observe pinch-off and therefore proper electrical behavior in these devices, the carrier concentration is a critical parameter. The electrical properties of ZnO films are very sensitive to deposition parameters and postdeposition treatments. Based on these features, adequate ZnO channel conductivity in TFTs has been attained either by depositing in an oxygen–argon gas flux mixture (producing a highly resistive ZnO film)[5] or by thermal annealing after deposition to reduce oxygen vacancies.[7] It has also been reported that ZnO channel conductivity depends on channel thickness,[6,8] and in a recent paper we reported the effect of deposition pressure on the electrical resistivity of ZnO sputtered films for active channels in TFTs.[9] On the other hand, the channel length (L) and channel width (W) are also important TFT parameters to achieve good device performance, since leakage current[10] and high series resistance effects can produce a drain-to-source current, resulting in degradation of TFT devices.[11]

In this work, ZnO layers were deposited by RF magnetron sputtering at room temperature, varying the deposition power. The aim of this paper is to determine the influence of the processing power in nonreactive plasma on the structural, morphological, and electrical properties of ZnO films and correlate them with the electrical response of TFTs with ZnO as the active channel. The electrical behavior of the TFT devices was studied as a function of ZnO channel layer (deposited at different powers). Finally, the dependence of main electrical parameters of ZnO TFTs, such as channel mobility, threshold voltage, and I_{on}/I_{off} ratio, on channel length is reported.

EXPERIMENTAL PROCEDURES

ZnO-based TFTs were fabricated using a bottom-common gate configuration as shown in Fig. 1a. The fabrication of TFTs started with exposure of p-Si (100) substrates to RCA standard cleaning.[12] After cleaning, the SiO_2 dielectric layer was thermally grown on the Si substrates. The ZnO layers were deposited on SiO_2/p-Si by radiofrequency magnetron sputtering at room temperature. The working pressure was maintained at 60 mTorr under argon gas flux of 50 sccm. Several ZnO layers, one per RF power, were deposited at 90 W, 100 W, 150 W, and 200 W, and the deposition time was fixed at 10 min for all cases. To create the source and drain electrodes, an aluminum blanket of 100 nm thickness was deposited by electron-beam evaporation and patterned by photolithography and lift-off processes. Dimensions of TFTs were defined by channel lengths of L = 20 μm, 40 μm, and 80 μm and channel width of W = 450 μm, as seen in the optical image of Fig. 1b. Finally, the back side of the Si substrate was cleaned with diluted hydrofluoric acid

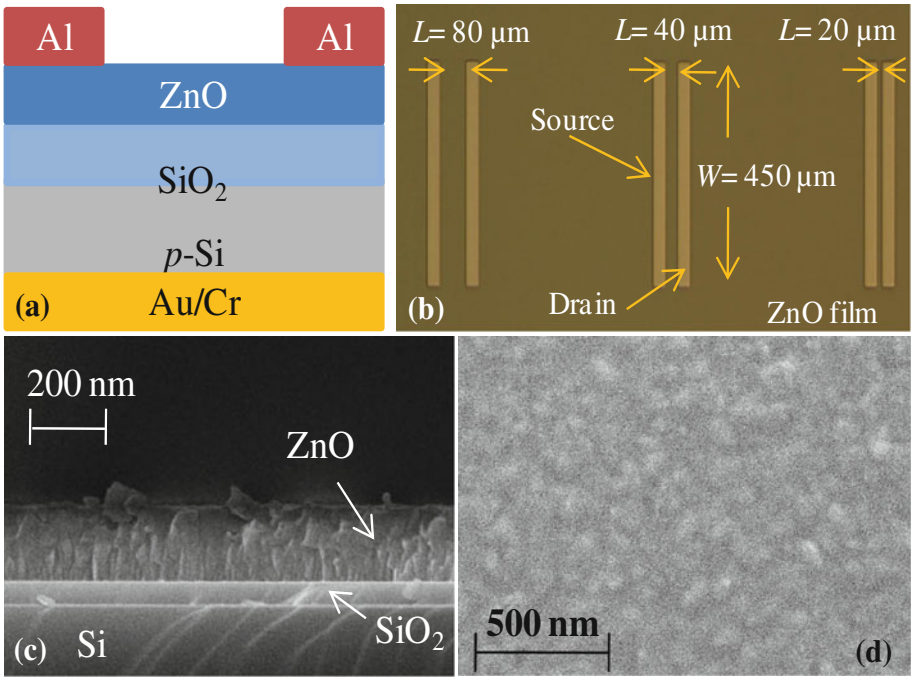

Fig. 1. (a) Schematic cross-section of the bottom-common gate ZnO-based TFT configuration. (b) Optical image of the ZnO TFTs. Device dimensions are L = 20 μm, 40 μm, and 80 μm and W = 450 μm. (c, d) Cross-sectional and top-view SEM images of ZnO film deposited on p-Si/SiO_2 substrate at 200 W, respectively.

and coated with chromium (10 nm) and gold (100 nm) films, deposited by electron-beam evaporation, as the gate layer. Figure 1c, d shows cross-sectional and top-view scanning electron microscopy (SEM) images of the ZnO film deposited on *p*-Si/SiO_2 substrate at 200 W.

The crystalline structure of the ZnO films was determined by using a Rigaku Ultima III diffractometer. Morphology and surface roughness were obtained by atomic force microscopy (AFM) measurements performed in contact mode (DI-Veeco Nanoscope IV). Film thickness and refractive index were determined by spectroscopy ellipsometry (SE) using a Jobin–Yvon Uvisel DH10 ellipsometer. Film thickness was also measured from cross-sectional images obtained with a Zeiss Supra 40 SEM. The electrical characterization of the TFT devices was performed using a Keithley 4200 semiconductor parameter analyzer.

RESULTS AND DISCUSSION

Figure 2 shows the XRD diffraction patterns of ZnO films deposited at 90 W, 100 W, 150 W, and 200 W, revealing a crystalline structure with a wurtzite (hexagonal) phase and a (002) preferred orientation (along the *c*-axis). The observed preferred crystalline orientation explains the columnar growth observed in the ZnO layer in Fig. 1c. Besides the ZnO diffraction peaks, the patterns in Fig. 2 display an additional peak centered at $2\theta \approx 60°$, which is related to the silicon substrate. The increase in intensity of the ZnO peaks evidences an increase of the film thickness with increasing deposition power. The most intense peaks, (002) and (103), were fitted to a Gaussian curve, and the fit parameters were used to calculate the particle size according to the Debye–Scherrer equation[13] and the lattice parameters *a* and *c* of the ZnO hexagonal structure. The calculated values indicate that the ZnO films are nanocrystalline. The ZnO film deposited at 90 W had the smallest particle size, 12.25 nm, while the film deposited at 150 W had the largest particle size, 15.35 nm. It has been reported that ZnO films grown by RF sputtering at room temperature are nanocrystalline with small crystallites of only a few nanometers in size.[5,14–16] Estimating the column width from the cross-sectional SEM image and the grain diameter from the top-view SEM image, both shown in Fig. 1, the estimated average values are about 60 nm and 80 nm, respectively. Thus, it is possible that the observed columns and grains in the ZnO films are structured by crystallites from 12 nm to 15 nm in size, as reported in Table I. The percentage variation of *a* and *c*, i.e., Δa and Δc, with respect to the values of bulk ZnO were also obtained and are presented in Table I.[17] These results indicate that the ZnO films are under compressive stress (in the plane of deposition), producing an increase of the *c* lattice constant oriented perpendicular to the substrate.[18]

Figure 3 depicts top-view AFM images of ZnO films deposited at different powers. Images were acquired in contact mode, and the collected scan area was 2 μm × 2 μm. It can be clearly appreciated that grain size increases with increasing power. This effect could be associated with the accumulation of nanoparticles to form grains or clusters. With increasing deposition power, these clusters grow larger, resulting in more compact film. The average

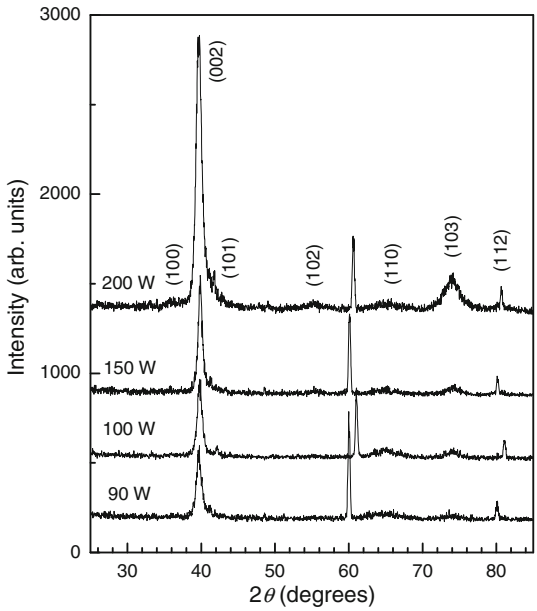

Fig. 2. XRD patterns of ZnO films deposited at different RF powers.

Table I. Lattice parameters *a* and *c* of the hexagonal structure in the ZnO crystal and their percentage variation, Δa and Δc

RF Power (W)	Particle Size by XRD (nm)	*a* (nm)	*c* (nm)	Δa (%)[a]	Δc (%)[a]
90	12.25	3.2463	5.2690	−0.100	1.194
100	12.58	3.2412	5.2536	−0.255	0.897
150	15.35	3.2350	5.2448	−0.446	0.729
200	13.48	3.2391	5.2558	−0.321	0.939

[a]c_0 = 5.2065 nm, a_0 = 3.2496 nm.

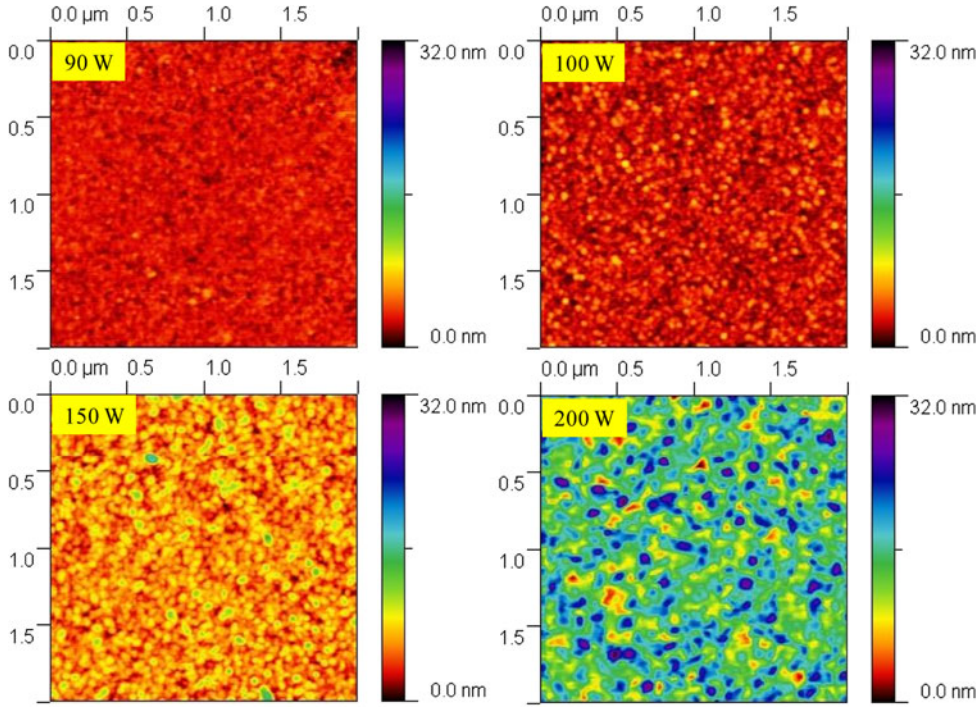

Fig. 3. Top-view AFM images of ZnO films deposited at different RF powers. The collected scan area was 2 μm $\times$ 2 μm.

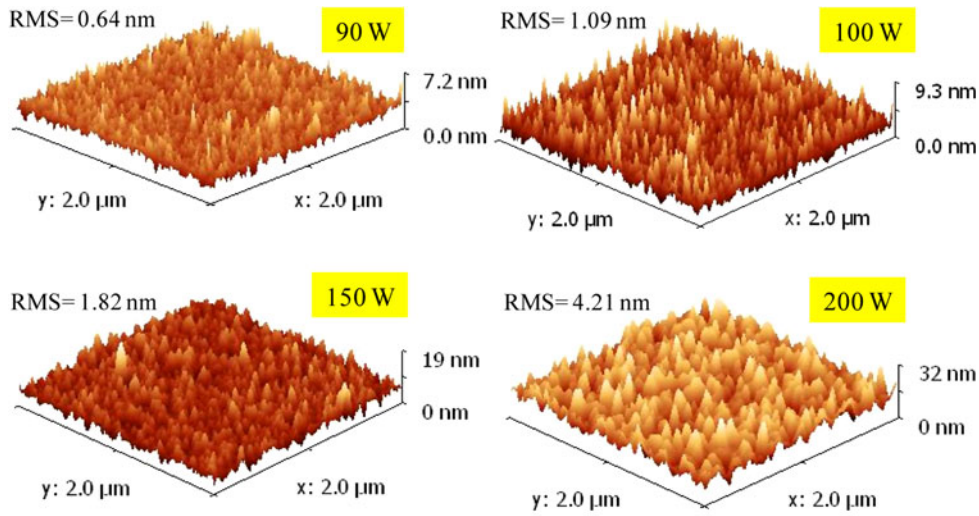

Fig. 4. 3D AFM images and RMS surface roughness values of ZnO films deposited at different powers. The collected scan area was 2 μm $\times$ 2 μm.

root-mean-square (RMS) surface roughness determined from these images also increases with power, as shown in the three-dimensional (3D) AFM images of Fig. 4. ZnO and SiO_2 film thicknesses and the ZnO refractive index were determined by SE measurements with incident angle of 70°. The physical model proposed for the system was air/roughness/ZnO layer/SiO_2 layer/Si substrate, where the surface roughness layer was modeled with Bruggeman's effective medium approximation,[19] composed of a mixture of equal volume fractions of air and ZnO. The refractive index of ZnO films was described by the Scientific Computing International (SCI) model,[20] and the SiO_2 film was represented by a homogeneous layer of well-known composition. This material type is characterized by the optical constants n (refractive index) and k (extinction coefficient) of SiO_2 as a function of wavelength, and the source file was provided by the Film Wizard software library. By minimizing the root-mean-square error (RMSE), the best fit values to the experimental data obtained for the entire system are presented in Table II. The

Table II. ZnO and SiO_2 film thicknesses and the refractive index of ZnO films determined by SE

RF Power (W)	ZnO Film Thickness (nm)	SiO_2 Film Thickness (nm)	Refractive Index of ZnO Film
90	68.45	65	2.15
100	64.40	65	2.33
150	113.90	65	2.36
200	241.55	65	2.44

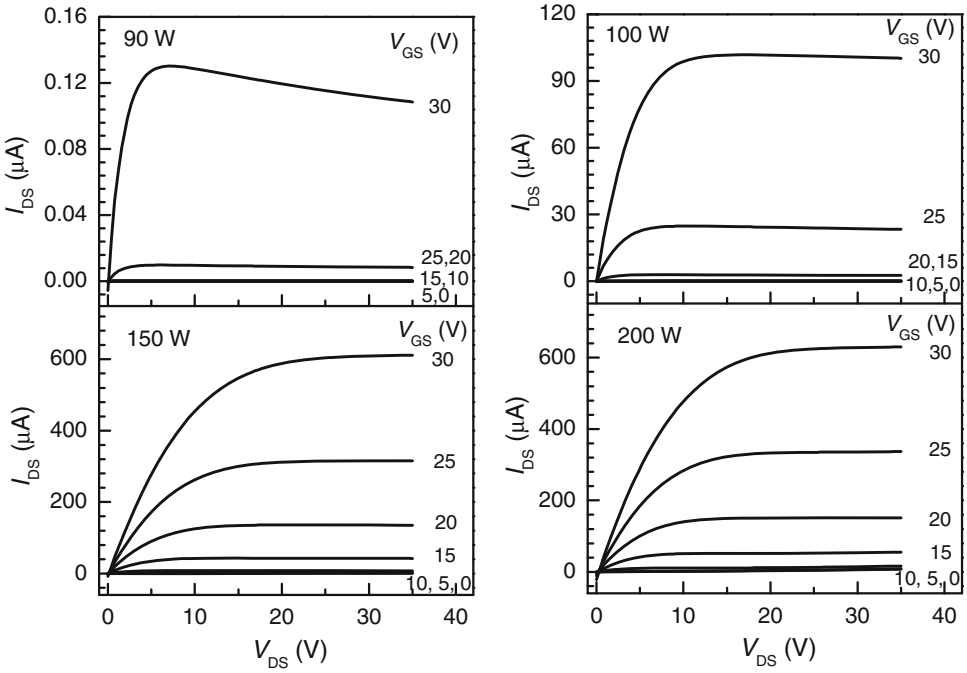

Fig. 5. I_D–V_{DS} curves of ZnO TFTs for ZnO films deposited at different powers. For these experiments, channel length L = 20 μm and channel width W = 450 μm were used.

65 nm SiO_2 film thickness determined by SE was confirmed by cross-sectional SEM (Fig. 1). As can be seen from Table II, the thickness and refractive index of ZnO films increase with deposition power. The thickness of the ZnO film deposited at 200 W also agrees reasonably well with that determined from the SEM image in Fig. 1. The increase of refractive index with deposition power can be attributed to the fact that increasing the deposition power produces greater densification of the film; for example, the AFM image of Fig. 3 corresponds to the top-view SEM image shown in Fig. 1d for the film grown at 200 W. In both cases, the observed morphology is similar, showing a dense film.

Figure 5 shows I_{DS}–V_{DS} curves of ZnO-based TFTs for all deposition powers. For these measurements, devices with channel length of L = 20 μm and channel width of W = 450 μm were used. The gate-to-source voltage (V_{GS}) was varied from 0 V to 30 V in steps of 5 V. The curves show the typical behavior of a TFT device with a n-type semiconductor active channel layer (a positive gate-to-source voltage induces electron channel accumulation). Pinch-off is observed in the electrical response of the four devices processed at different deposition powers. The main difference observed is the level of current saturation, which goes from 0.12 μA for the device processed at 90 W to about 600 μA for the one processed at 200 W (at V_{GS} = 0 V in both cases).

To understand the difference observed in the electrical response of the TFT devices, the electrical resistivity of the ZnO films was calculated using the I_{DS}–V_{DS} data of the TFTs measured at V_{GS} = 0 V. Figure 6 summarizes the estimated values of resistivity for the ZnO films deposited at 100 W, 150 W, and 200 W, with L = 20 μm, 40 μm, and 80 μm. The linear dependence of I_{DS} versus V_{DS} (at V_{GS} = 0 V), which is typical of ohmic contacts, can be seen in the inset. Clearly, the electrical resistivity of the ZnO films decreases with deposition power. The highest value of resistivity is close to 10^8 Ω-cm, for the ZnO film deposited at 100 W with L = 80 μm. When the power is increased, the ZnO films become more conductive, with resistivity on the order of 10^3 Ω-cm to 10^4 Ω-cm for the film deposited at 200 W. The resistivity of films deposited at the lowest power

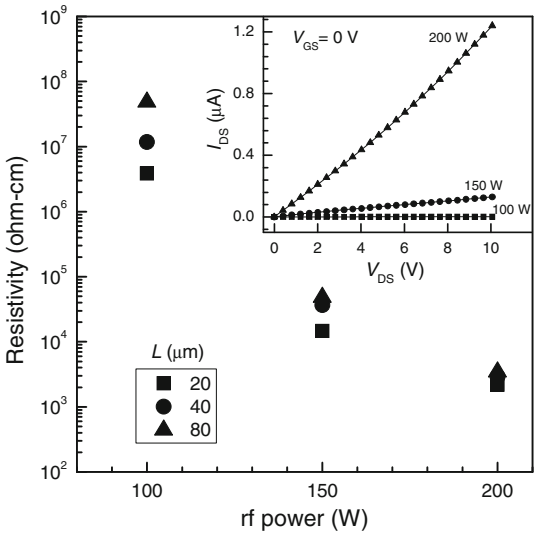

Fig. 6. Dependence of electrical resistivity on RF power and channel length. These values were calculated from the I_{DS}–V_{DS} data of TFTs measured at V_{GS} = 0 V, as shown in the inset.

(90 W) could not be measured due to its high resistivity ($>10^8$ Ω-cm). Also in Fig. 6 the variation of resistivity as a function of channel length is more noticeable in the most resistive ZnO film (100 W) but is not evident in the most conductive film (200 W). Specifically, the resistivity increases with increasing channel length, and this behavior can be attributed to series resistance effects.[11]

The magnitude of the power used during sputter deposition produces two different effects on the ZnO films: (1) The film thickness increases with increasing power, causing the channel conductance of the ZnO TFTs to vary. It has been found that this property enhances in thicker films.[4,9] (2) Grain size increases with increasing power, as seen from the AFM images. The increase in grain size reduces the density of grain boundaries and consequently enhances film conductivity. Low-power sputter deposition can be visualized as a low-energy system of ionized particles and, consequently, sputtered species. This situation could stimulate high nucleation density on the substrate and subsequent formation of a large number of small grains or clusters. Low diffusion rates, due to the low particle energy, further contribute to the formation of small grains. In contrast, high-power sputter deposition or higher-energy ionized particles (sputtered species) do not promote nucleation on the substrate; rather, they enhance diffusion of sputtered species towards previously formed grains. This case (high power) results in a smaller number of grains, of larger size, than those formed at lower powers.[21,22]

Figure 7 displays the transfer curves of drain current I_{DS} (left-side axis) and the square root of drain current $I_{DS}^{1/2}$ (right-side axis) versus gate voltage V_{GS} at fixed drain voltage V_{DS} of 40 V for TFTs with ZnO channel layers deposited at 90 W, 100 W, 150 W, and 200 W. Devices were measured for L = 20 μm, 40 μm, and 80 μm and W = 450 μm. From the I_{DS} versus V_{GS} curves it can be concluded that TFTs operate in enhancement mode, since positive gate voltages are required to turn the devices on. These graphs also show the variation of drain current in the off-state I_{off} as a function of power. Independent of the channel length, the lowest I_{off} current, on the order of 10^{-10} A, was found in the transistors with channel layers deposited at 90 W and 100 W. It increases with increasing power up to 10^{-8} A to 10^{-5} A, dependent on channel length, for devices with channel layers processed at 150 W and 200 W. Thinner and more resistive ZnO films show lower I_{off} values, as previously reported in literature.[6,9] This behavior is associated with decreasing channel conductance in the ZnO layer. The drain current in the off-state depends on the thickness and conductivity of the channel layer, as well as the TFT dimensions, as given by

$$I_{DS,off} = \frac{\sigma W t}{L} V_{DS}, \tag{1}$$

where σ and t represent the electrical conductivity and thickness of the channel layer, respectively, L and W are the channel length and channel width of the TFT, and V_{DS} is the source-to-drain voltage.[23] Thus, the behavior of I_{off} in Fig. 7 is explained in terms of Eq. 1 because the lowest values of I_{off} ($\sim 10^{-9}$ A to 10^{-10} A) correspond to the thinner and more resistive ZnO films deposited at 90 W and 100 W, whereas the higher values of I_{off} were measured on the thicker and more conductive ZnO films processed at 150 W and 200 W. In the later case, source-to-drain leakage or I_{off} increases with decreasing channel length. Due to this behavior, this leakage current can be related to the source-to-drain field strength.[10] Besides, we can observe that the morphology of the ZnO film deposited at 150 W is homogeneous, as shown in the AFM images (Fig. 3). Thus, we can assume that the number of grain boundaries along the source–drain path increases with the channel length. Consequently, the leakage current decreases. On the other hand, the on-state current I_{on} reached values up to $\sim 10^{-3}$ A for TFTs with ZnO films deposited at 100 W, 150 W, and 200 W. Figure 8 shows the variation of the I_{on}/I_{off} ratio extracted from the transfer curves of Fig. 7 as a function of deposition power. TFTs with ZnO films deposited at 100 W have the highest $I_{on}/I_{off} \approx 10^6$, and those deposited at 200 W the lowest $I_{on}/I_{off} \approx 10^2$ to 10^3, following the trend of I_{off}.

Channel mobility and threshold voltage were extracted from the $I_{DS}^{1/2}$ versus V_{GS} curves of Fig. 7 in the saturation region ($V_{DS} > V_{GS} - V_T$) for all devices. Saturation drain current $I_{DS}(sat)$ can be expressed as[24]

$$I_{DS}(sat) = \frac{W \mu_{sat} C_{ox}}{2L} (V_{GS} - V_T)^2, \tag{2}$$

where W and L are the channel width and channel length, respectively, μ_{sat} is the electron channel

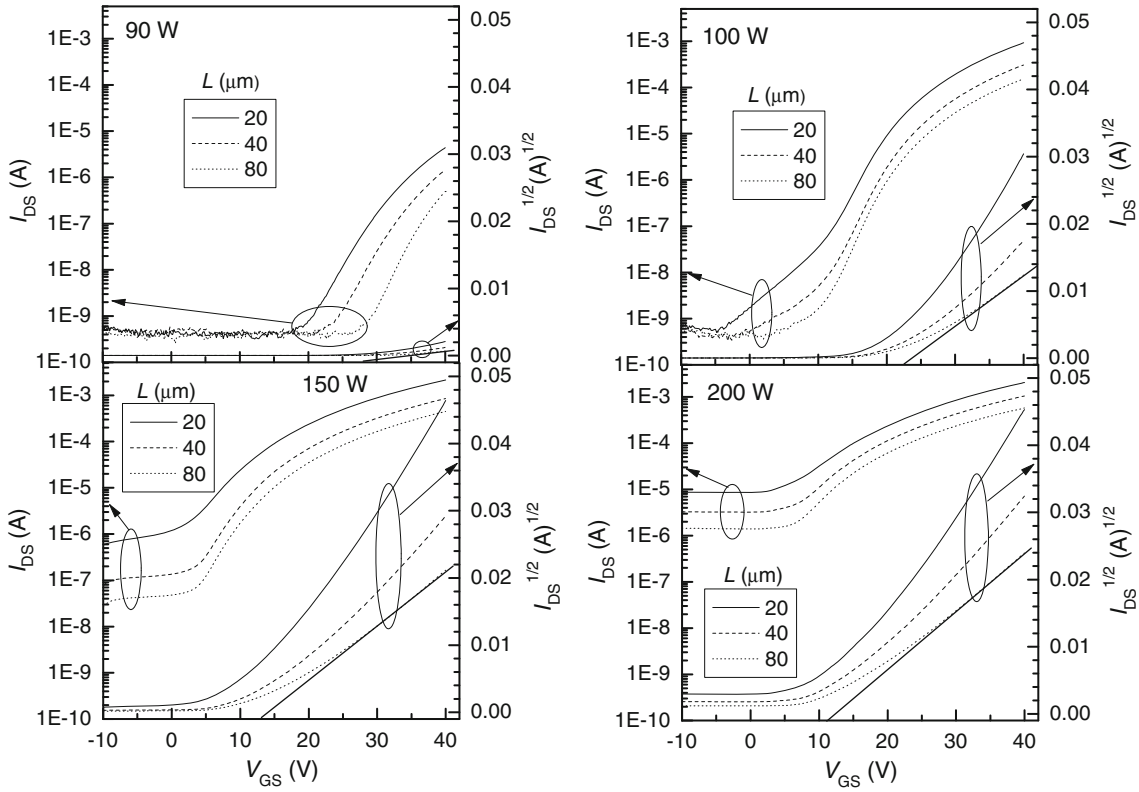

Fig. 7. I_{DS}–V_{GS} and $I_{DS}^{1/2}$–V_{GS} curves measured at V_{DS} = 40 V for TFTs with ZnO channel layers deposited at different powers.

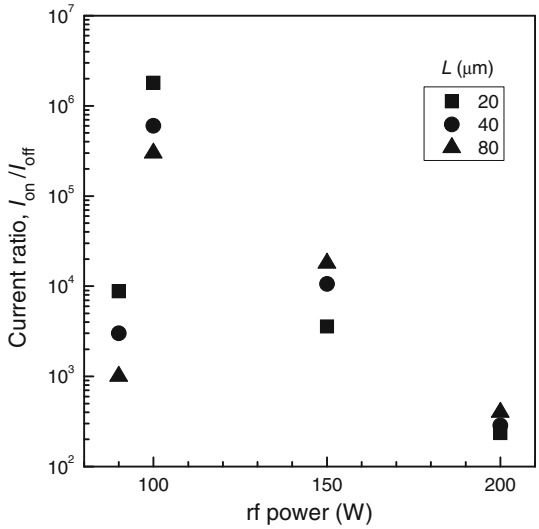

Fig. 8. Estimated I_{on}/I_{off} values for TFTs with ZnO channel layers deposited at different powers.

mobility, C_{ox} is the capacitance per unit area of the gate dielectric layer, and V_T is the threshold voltage. The saturation mobility is determined as

$$\mu_{sat} = \frac{2Lm^2}{WC_{ox}}, \quad (3)$$

where m is the slope of the $I_{DS}^{1/2}$ versus V_{GS} plot. Figure 7 shows the best fit to this equation for the devices with L = 80 μm. The threshold voltage is given by the intersection of the straight-line fit with the V_{GS}-axis. The obtained threshold voltages and field-effect mobilities (μ_{FE}) are shown in Fig. 9. The mobility was observed to increase with deposition power, with the highest value of 4.2 cm^2/Vs. The lowest $\mu_{FE} \approx 10^{-1}$ cm^2/Vs was found in TFTs with ZnO channel layer deposited at 90 W. This result could be associated with mobility degradation due to high grain boundary density in the ZnO channel, as shown in AFM images (Fig. 3). In addition, Fig. 9 shows a clear decreasing trend of V_T when the power is increased. As has been previously reported,[6,8] and according to the results of the present study, V_T is a function of the thickness and resistivity of the channel layer. The strong effect of the power on V_T could be associated with the variation of grain size with the power. As the grain size decreases, V_T increases (Fig. 9), since for a given channel dimension the number of grain boundaries increases and the carriers will therefore have to overcome additional potential barriers.[25] The channel length-dependent V_T is evident only in the TFTs with the most resistivity ZnO film (deposited at 90 W). This behavior has also been observed in polycrystalline silicon TFTs.[25]

CONCLUSIONS

We investigated the structural, morphological, and electrical characteristics of ZnO sputtered

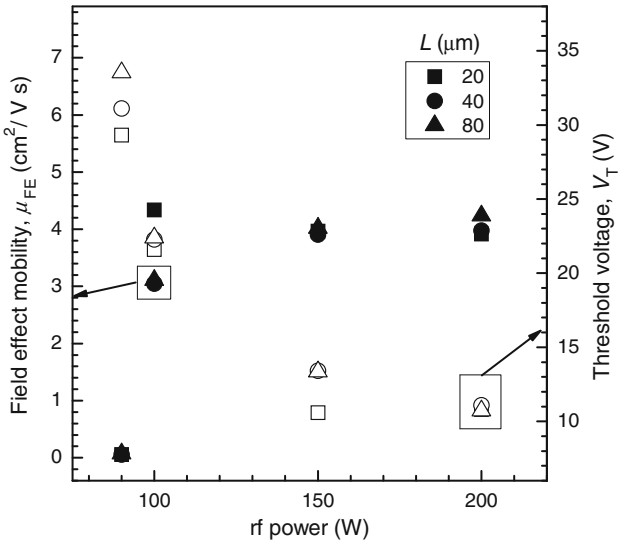

Fig. 9. Dependence of threshold voltage (V_T) and field-effect mobility (μ_{FE}) on RF power and channel length.

films, varying the deposition power at room temperature and monitoring their performance as active channels in TFT devices. ZnO polycrystalline films with high electrical resistivity in the 10^3 Ω-cm to 10^7 Ω-cm range resulted from deposition power variation with suitable characteristics to be used as active channel layers in TFTs applications. The variation of electrical resistivity of ZnO films directly impacted the channel conductance and, therefore, the electrical response of the ZnO-based TFTs. The decrease of ZnO film resistivity with increasing power was the result of increasing cluster size with more compact structure, as shown by AFM and ellipsometric measurements. Regarding the electrical behavior of ZnO-based TFTs, for thicker and less resistive ZnO films, it was found that the threshold voltage could be lowered down to 10 V with a field-effect mobility as high as 4.2 cm^2/Vs; however, the on/off ratio was degraded to $\sim 10^2$. For thinner and more resistive ZnO films, the on/off ratio was $\sim 10^6$ with field-effect mobility of ~ 3 cm^2/V s; however, the threshold voltage was too high. A notable effect of channel length on threshold voltage and on/off ratio was found in TFTs with thinner and more resistive ZnO films. The best TFT devices exhibited field-effect mobilities of ~ 3 cm^2/Vs, threshold voltages of 22 V, and on/off ratio of $\sim 10^6$. These devices contained a highly resistive ZnO channel layer, in the range from 3×10^6 Ω-cm to 5×10^7 Ω-cm, due to channel length variation.

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