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Electrical and Mechanical Properties of Through-Silicon Vias and Bonding Layers in Stacked Wafers for 3D Integrated Circuits

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Thermal stress issues in a three-dimensional (3D) stacked wafer system were examined using finite-element analysis of the stacked wafers. This paper elucidates the effects of the bonding dimensions on mechanical failure and the keep-away zone, where devices cannot be located because of the stress in the Si. The key factors in decreasing the thermal strain were the bonding diameter and thickness. When the bonding diameter decreased from 40 μm to 12 μm, the equivalent strain decreased by 83%. It is noteworthy that the keep-away zone also decreased from 17 μm to zero when the bonding diameter decreased from 40 μm to 12 μm. When the bonding thickness doubled, the equivalent strain decreased by 44%. The effects of the dimensions and arrangement of through-silicon vias (TSV) were also analyzed. Small TSV diameter and pitch are important to decrease the equivalent strain, especially when the amount of Cu per unit volume is fixed. When the TSV diameter and pitch decreased fourfold, the equivalent strain decreased by 70%. The effects of TSV height and the number of die stacks were not significant, because the underfill acted as a buffer against thermal strain.

Key words: Through-silicon via, 3D integrated circuits, thermal stress, keep-away zone, finite-element analysis

INTRODUCTION

Three-dimensional (3D) integrated circuit (IC) packaging technology is now emerging to replace conventional two-dimensional packaging technologies and meet the increasing demands for next-generation semiconductor chips, which are smaller and perform better.[1,2] Through-silicon via (TSV) technology is a method for producing electrical interconnects that vertically penetrate such stacked wafers or chips. TSV technology can reduce resistance–capacitance (*RC*) delay and power consumption, increase the number of I/O, and enhance performance because of its short connection length.[3,4]

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Thermal stress-induced failure due to the coefficient of thermal expansion (CTE) mismatch during postprocessing or operation is one of the most important issues in 3D ICs.[5,6] The CTE of Cu is 17.7 ppm/°C, which is seven times larger than that of Si (2.61 ppm/°C).[7,8] This thermal stress causes several issues, which are classified into Cu and Si problems.[5,9–13] The Cu issues are mainly related to mechanical failures, such as debonding between stacked wafers, TSV cracks, and TSV extrusion, which occurs when Cu rises up over the Si. The Si issues include the keep-away zone and Si cracking. The keep-away zone is the area where devices cannot be located because their performance could be degraded by thermal stress. It has been reported that 100 MPa of stress can induce up to a 7% change in mobility in metal–oxide–semiconductor field-effect transistor (MOSFET) devices.[14] Si cracking indicates fractures caused by thermal expansion of Cu.

Several experiments and numerical analyses have been performed in an attempt to understand the thermomechanical issues of 3D ICs, considering a single layer of Si.[5,9–13] However, stacked wafers have different issues than single-wafer systems, because of the additional structures and materials such as the Cu bonding and underfill, as shown in Fig. 1a. Change in these additional structures, especially the Cu bonding, is expected to change the thermal stress evolution in stacked wafers. Although a large bonding diameter is advantageous for wafer bonding, limits must be imposed on this parameter because of thermal stress. The thermal stress can be affected by bonding thickness as well as bonding diameter. Furthermore, it is expected that the thermal stress induced by Cu bonding causes significant variations in the keep-away zone in stacked wafers. This thermal stress in the Cu bonding affects the residual stress of Si because of the plastic behavior of Cu during heat treatments. In addition, the keep-away zone will be influenced not only by Cu bonding but also by the depth under the Si surface. There are other issues related to the variation of the TSV geometry that affect the thermal stress. It is also uncertain how the number of die stacks affects the thermal stress. To elucidate these various issues, analysis of 3D stacked wafers is required.

In this study, the thermal stress in Si and Cu was analyzed with dimensional variables, such as the diameter and the thickness of bonding, using the finite-element method (FEM). The effects of the TSV geometry, which includes TSV diameter, height, and pitch, and the number of die stacks were also considered. The effect of the air gap was examined, because underfilling for a 12-inch wafer is difficult and therefore is usually ignored when considering wafer-to-wafer bonding. Analyzing the stress in both Cu and Si is required to fully understand the mechanical and electrical issues caused by thermal stress in stacked wafers. For the Cu analysis, all components of the thermal strain were analyzed to reveal the deformation of Cu while considering the effects on Si. In the case of Si, the stress along the channel direction was analyzed to study the keep-away zone.

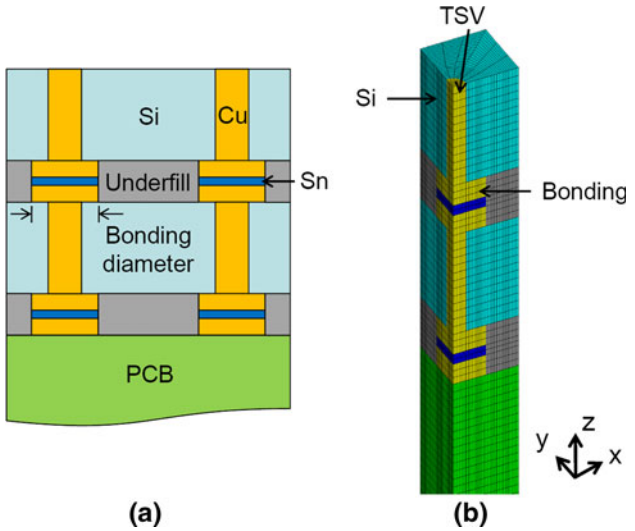

Fig. 1. (a) Schematic diagram of the 3D IC package containing the TSV and Cu bonding with two stacked layers of silicon on PCB. (b) One-quarter of a unit cell with a hexahedral mesh, as used in the finite-element analysis.

FINITE-ELEMENT MODEL

Finite-element analysis was conducted to calculate the thermal stress in stacked wafers. The simulation model of the 3D IC has the following structure: two wafers on the PCB, using Cu-Sn-Cu bonding to attach each layer. A schematic diagram of this model is shown in Fig. 1a. Underfill was inserted into the gap between the wafers. The passivation layer on the Si surface and the TSV inside, the metallization layer, the diffusion barrier, and the dielectric layer (e.g., silicon dioxide) were not considered in the model. We focused only on the principal factors that are predicted to significantly affect the thermal stress, to reduce the necessary calculations and simplify the analysis. It is assumed that the omitted layers do not considerably affect the thermal stress and its distributions as functions of various parameters. The TSV diameter, Cu bonding diameter, pitch, bonding thickness, wafer thickness, and PCB thickness were 12 μm, 30 μm, 60 μm, 25 μm, 50 μm, and 200 μm, respectively. The Cu-Sn-Cu bonding has 10 μm of Cu, 5 μm of Sn, and 10 μm of Cu.

The finite-element model used in this study was a SOLID95 20-node hexahedral element using ANSYS simulation software. A mapped mesh with a uniformly shaped element was applied. We assumed that one-quarter of the unit cell, based on symmetry, was repeated in the 3D IC structure. The symmetry condition was applied to the four side-walls of the quarter unit cell, which is shown in Fig. 1b.

The material property values are presented in Table I. The materials, except Cu, were assumed to be isotropic and linearly elastic. Bilinear isotropic strain-hardening behavior of Cu in the TSV was assumed, considering the yield of Cu to include its

Table I. Thermomechanical properties of the materials used in the finite-element calculations

Material	Young's Modulus (GPa)	CTE (ppm/°C)	Poisson's Ratio
Si	131.0[18]	2.61[7]	0.278[18]
Cu	111.5[8]	17.7[8]	0.343[19]
Underfill	9[20]	26[20]	0.3[20]
Sn	49.9[21]	23.8[21]	0.35[21]
PCB	16[20]	16[20]	0.28[20]

plastic behavior and flow stress. The initial yield stress and tangential modulus of Cu are 172.3 MPa and 517 MPa, respectively.[15,16] The elastic modulus, coefficient of thermal expansion, and Poisson's ratio of Cu are also given in Table I.

It was assumed that the 3D IC structure with the TSV was heated during the wafer bonding process, in which the temperature was 250°C. In the analysis of mechanical failure in Cu, the thermal load varied from 250°C to 25°C. In the case of the analysis of mobility change in Si, the residual stress was analyzed because the thermal stress in Cu during the heating and cooling of the wafer bonding process affects the stress in Si; the stress is presented as the residual stress of Si, which is used to calculate the keep-away zone. Therefore, we set the temperature range from 25°C to 250°C, with cooling back down to 25°C. The geometric variations included the TSV diameter, the bonding diameter, the pitch, the height, and the number of die stacks.

To elucidate the issue of mechanical failure, all components of the strain, including the equivalent strain, were considered. The equivalent strain, especially, was used to represent the strain state in stacked wafers. Values of stress cannot be compared because Cu exhibits plastic behavior and plastic deformations occur. The equivalent strain is computed using the following equation:

$$\varepsilon_{\mathrm{eq}} = \frac{1}{\sqrt{2}(1+\nu)}\left[(\varepsilon_{xx}-\varepsilon_{yy})^2+(\varepsilon_{yy}-\varepsilon_{zz})^2+(\varepsilon_{zz}-\varepsilon_{xx})^2 + \frac{3}{2}\times(\varepsilon_{xy}^2+\varepsilon_{yz}^2+\varepsilon_{xz}^2)\right]^{1/2}, \quad (1)$$

where ε_{ij} are the strain tensor elements and ν is Poisson's ratio.

To analyze the keep-away zone, it was assumed that the devices were aligned along <110> channel orientations, which corresponds to the x direction in the finite-element model of a (001) wafer. The mobility change in Si along the <110> channel direction was analyzed to determine the keep-away zone for transistors from the TSV. In a previous research study by Thompson et al.,[14] piezoresistance coefficients were measured and a relative mobility change was obtained from these results using the following simple equation:

$$\Delta\mu/\mu \approx \pi_{\parallel}\sigma_x + \pi_{\perp}(\sigma_y+\sigma_z), \quad (2)$$

where $\Delta\mu/\mu$ is the fractional change in mobility and $\pi_{\parallel}$ and $\pi_{\perp}$ are the longitudinal and transverse piezoresistance coefficients, respectively. The analysis of the keep-away zone was done separately for the p-MOSFET and the n-MOSFET because of the different piezoresistance coefficients. The longitudinal and transverse piezoresistance coefficients in the <110> channel direction on a (110) wafer for the p-MOSFET are 7.18×10^{-4} MPa and -6.63×10^{-4} MPa^{-1}, respectively; they are -3.16×10^{-4} MPa and -1.76×10^{-4} MPa^{-1}, respectively, for the n-MOSFET.[14] A path plot for the keep-away zone near the Si surface was performed along the channel direction. The Si surface was interesting, because the devices are most likely to be located near the Si surface. The criterion for the keep-away zone was set based on a 5% carrier mobility change, as reported previously.[15]

RESULTS AND DISCUSSION

Effects of Bonding Layers on Mechanical Failure

The points where thermal stress and strain were localized were calculated for various dimensions by finite-element analysis. The thermal strain was calculated by finite-element analysis for various dimensions. The maximum equivalent strain was at the point where Cu, Si, and underfill converged, with a value of 1.1%. This point is labeled "Bonding" in Fig. 1b. In addition, the equivalent strain at the edge of the top interface between the Cu TSV and Si was 0.45%, which was the highest value among the points of the Cu TSV. The edge of the top interface is labeled "TSV" in Fig. 1b. The strains at these points were higher than those of other points in the bonding or the TSV, even when the geometry changed. Hence, if a deformation or crack occurs because of the thermal load, it is predicted that these points, especially the bonding, will be the first sites of failure.

The equivalent strain as a function of bonding diameter is shown in Fig. 2a. This result shows that the bonding diameter was a critical factor that significantly affected the thermal strain at the bonding. The other dimensional parameters, except bonding diameter, were fixed. In this figure, bonding diameter is plotted on the x-axis, and equivalent strain on the y-axis. The diameter difference between the TSV and the bonding is also presented on the x-axis. The diameter difference was 0 μm when the bonding diameter was 12 μm because the TSV diameter was fixed at 12 μm. The equivalent strain at the bonding significantly increased as the bonding diameter increased, as shown in the graph. When the bonding diameter decreased from 40 μm to 12 μm, the equivalent strain decreased by 83%. Considering the diameter difference between the TSV and the bonding, this result also means that the equivalent strain at the bonding increased as the diameter difference between the TSV and the bonding became larger. The primary reason why the equivalent strain reduced to near zero for small bonding diameter is that the site at which thermal strain was localized disappeared. In other words, as the bonding diameter increased, the diameter difference between the TSV and bonding increased, which created and increased new stress-localized sites. The equivalent strain at the TSV did not change significantly. This is because variation in the bonding diameter did not affect the geometry at

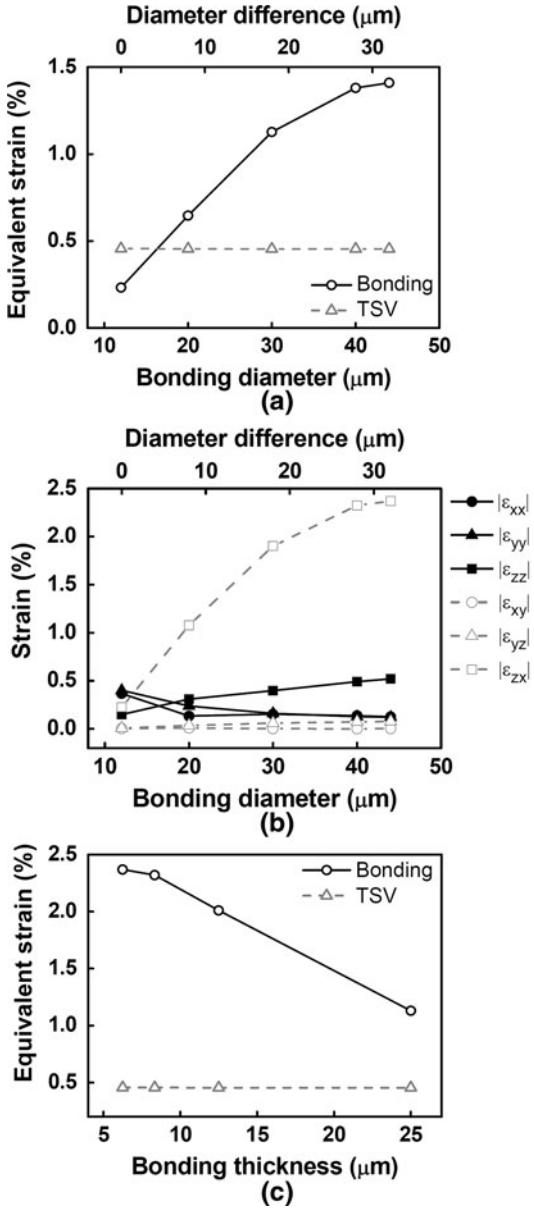

Fig. 2. (a) Equivalent strain change at the bonding and the TSV as a function of bonding diameter and diameter difference. (b) Normal and shear strain change at the bonding as a function of bonding diameter. (c) Equivalent strain change at the bonding and the TSV as a function of bonding thickness.

the TSV. It is noteworthy that increasing the bonding diameter or diameter difference is predicted to cause deformation of Cu at the bonding.

The strain components including normal and shear strains were calculated to analyze the increase in the equivalent strain only at the bonding, as shown in Fig. 2b. The increase of the equivalent strain at the bonding occurs because of the change of the shear strain. Except for the shear strain (ε_{zx}), strains were not affected by changes in the bonding diameter, but the shear strain (ε_{zx}) increased significantly as the bonding diameter increased. The equivalent strain at the bonding increased as the bonding diameter became larger because of the increase in the shear strain (ε_{zx}), as shown in Eq. (1). This result also implies that failure at the bonding can be a form of delamination between the stacked wafers.

The increasing shear strain was closely connected with the increasing amount of Cu and the generation of a new interface. The shear strain (ε_{zx}) increased with the bonding diameter because of an increase in the amount of Cu in the x direction, which results in more thermal strain in the x direction. This thermal strain is then localized at the bonding. Therefore, the shear strain (ε_{zx}) increased as the bonding diameter became larger. On the other hand, this behavior could be explained by the generation of a new interface. The lowest values of the equivalent strain and shear strain (ε_{zx}) in the graphs are shown at the first point for which the bonding diameter and the TSV diameter are the same. Figure 2b shows that the absolute value of the shear strain (ε_{zx}) at the bonding increased from approximately 0.2% to 1.1%. When the bonding diameter became larger than the TSV diameter, the strain increased significantly as well. A bonding diameter that is larger than the TSV diameter means that an interface in the z-plane between Si and Cu was generated. Therefore, the shear strain (ε_{zx}) increased with the bonding diameter because of the formation of a new interface between Si and Cu.

The values of the equivalent strain at the bonding and the TSV as functions of bonding thickness are shown in Fig. 2c. Reducing the bonding thickness significantly increased the equivalent strain at the bonding, whereas the equivalent strain at the TSV did not change. When the bonding thickness increased from 12.5 μm to 25 μm, the equivalent strain decreased by 44%. It is an important discovery that thin bonding is expected to increase the thermal strain. This result is attributed to thinning of the bonding and underfill. Considering the thermal strain in the thickness direction (z-direction), the PCB is the principal factor that creates thermal strain, because the PCB is relatively thick and has large CTE in the 3D IC. The PCB induces significant thermal strain by pulling or pushing the whole 3D IC structure during thermal loading. The bonding layer with the Cu bonding and the underfill has to withstand this force induced by the PCB. It is harder for the thin bonding layer to withstand this force than the thick bonding layer, and therefore the thermal strain becomes more localized in the thin bonding layer.

Regarding these results for the bonding dimensions, it is suggested that the bonding diameter or the diameter difference between the TSV and the bonding should be decreased to diminish the possibility of Cu deformation at the bonding. In addition, thick bonding should be required to decrease the thermal strain. Therefore, it is important to manufacture small and thick bonding to prevent

deformation at the bonding, even though this will make the fabrication of Cu pillars or pads and the alignment of wafers for the wafer bonding process more difficult.

Impacts of Bonding Layers on Carrier Mobility Change in Si

The bonding structure played a crucial role in changing the keep-away zone, where devices cannot be located because of the change in mobility. The mobility change was calculated from the residual stress of Si using Eq. (2). This residual stress in the TSV structure is caused by the plastic behavior of Cu after thermal loading. Figure 3a shows the mobility change as a function of the distance from the TSV. It was revealed that the bonding induced significant mobility change. The TSV diameter and bonding diameter were 12 μm and 40 μm, respectively. The keep-away zone for the p-MOSFET was found to be 17.5 μm, while that for the n-MOSFET was 15.6 μm. The mobility change of the p-MOSFET first decreased from zero to a negative value with distance from the TSV. After reaching the most negative value of the mobility change, it increased from a negative to a positive value. It is important that the maximum mobility change appeared near the end of the bonding diameter. This implies that the bonding structure affects the keep-away zone. After the maximum mobility change, it decreased in inverse proportion to the distance from the TSV.

The reason for these profiles of the mobility change lies in the interaction among the component stresses induced by the contraction of Cu, as shown in Fig. 3b. The shape of the curve for the mobility change is similar to that for the longitudinal stress (σ_{xx}). This is because the absolute value of the longitudinal stress (σ_{xx}) is much greater than those of the transverse stresses (σ_{yy}, σ_{zz}) throughout the region in the graph. The predominance of the longitudinal stress reduced the effect of the transverse piezoresistance coefficient, which was negative. This tendency of the longitudinal stress is due to the contraction of Cu during the temperature decrease from the bonding temperature to room temperature. The shrinkage of the Cu bonding caused compressive stress in the Si, which was just above the Cu bonding. The shrinkage of the Cu bonding pulled the Si that was just above the underfill, that is, the Si at the edge of the Cu bonding, toward the center of the Cu bonding. This caused tensile stress in Si in the region past the edge of the bonding. At the point where the distance from the TSV was 14 μm, the mobility change showed an abrupt drop to almost zero. This occurred because the transverse stress (σ_{zz}) became similar to the longitudinal stress at this point where the end of the Cu bonding contacts the underfill. The CTE difference between these two materials caused this longitudinal stress. The p-MOSFET was revealed to be more sensitive to the stresses than the n-MOSFET. This is because the effect of the piezoresistance coefficients of the p-MOSFET is much greater than that of the n-MOSFET. In the case of the n-MOSFET, the predominance of the longitudinal stress decreased the effect of the transverse piezoresistance coefficient, similar to the behavior observed for the p-MOSFET. The profile of the mobility change was reversed when compared with the p-MOSFET, which was due to the negative values of the piezoresistance coefficients. A sudden change of the mobility similar to the p-MOSFET was not observed, because the longitudinal and transverse piezoresistance coefficients were both negative.

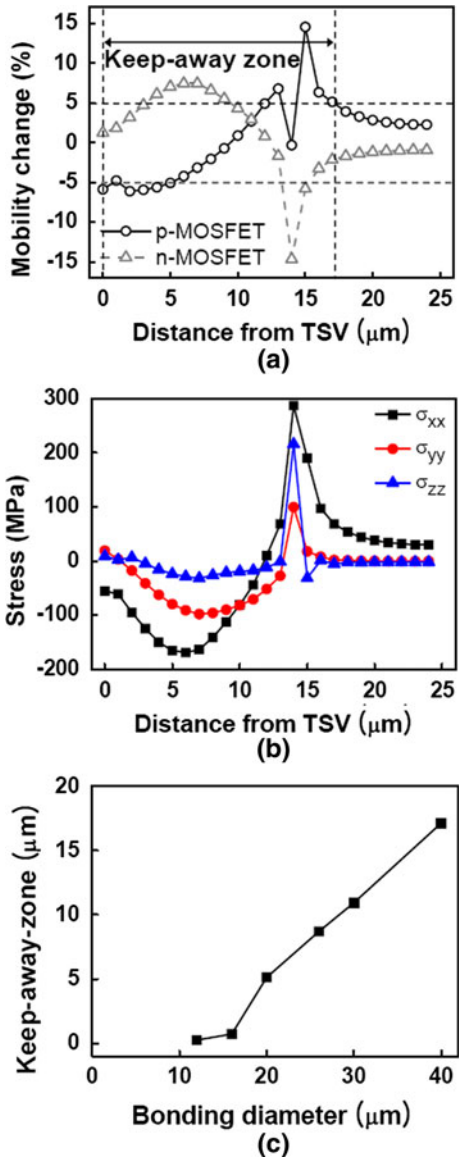

Fig. 3. (a) Carrier mobility change showing the keep-away zone near the Si surface with the distance from the TSV for bonding diameter of 12 μm. (b) Variation of stresses according to distance from the TSV. (c) Change in the keep-away zone as a function of bonding diameter.

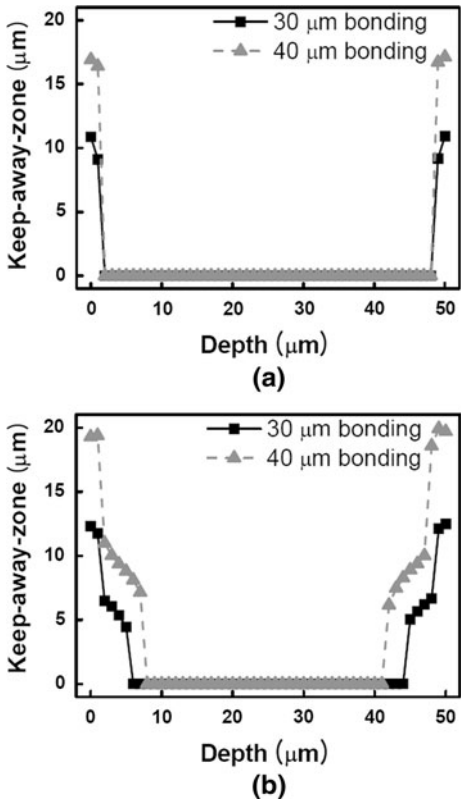

Fig. 4. Change in keep-away zone as a function of depth from the Si surface for bonding diameter of 30 μm and 40 μm, assuming carrier mobility change tolerance of (a) 5% and (b) 3%.

The keep-away zone as a function of bonding diameter is shown in Fig. 3c. Increasing the bonding diameter was the most significant cause of increasing keep-away zone. The TSV diameter, TSV height, and pitch were 12 μm, 50 μm, and 60 μm, respectively. The keep-away zone increased dramatically when the bonding diameter increased. When the bonding diameter decreased from 40 μm to 12 μm, the keep-away zone decreased from 17 μm to zero. This finding is similar to previously reported results[5] in which a single wafer was considered and the keep-away zone increased as the TSV diameter became larger. From both previous and our results, it is revealed that an increase in TSV diameter and bonding diameter, which means an increasing amount of Cu, causes greater thermal strain and expansion of the keep-away zone. On the other hand, variations in pitch, TSV height, and number of die stacks did not significantly affect the residual stress of Si or the keep-away zone. Furthermore, variation of the TSV diameter did not affect the keep-away zone significantly in our results for the 3D IC structure. From these results, we can conclude that only the bonding diameter, among other dimensional parameters, affects the keep-away zone, and that a decrease in the bonding diameter is needed to reduce the keep-away zone.

The keep-away zone was also closely related to the depth of Si where devices are located, as shown in Fig. 4a. The graph shows the depth dependence of the keep-away zone based on a carrier mobility change tolerance of 5% for bonding diameter of 30 μm and 40 μm. The depths of 0 μm and 50 μm on the x-axis indicate the surfaces of the Si, and the curves on the graph have bilateral symmetry. The keep-away zones for bonding diameter of 40 μm at depths of 0 μm and 1 μm under the Si surface are significantly higher than those for bonding diameter of 30 μm. These keep-away zones disappeared 2 μm below the Si surface for both bonding diameters of 30 μm and 40 μm. This result reveals that the mobility change decreases sharply with distance from the Si surface. However, if the devices are too sensitive to perform normally for a mobility change smaller than 5%, the keep-away zone will increase significantly. Figure 4b shows the keep-away zone as a function of depth, assuming that the criteria for the keep-away zone were set based on a 3% carrier mobility change. In this case, the keep-away zones disappeared at a depth of 9 μm under the Si surface for bonding diameter of 40 μm. From these results, it is suggested that devices should be placed at a depth of a few micrometers under the Si surface to reduce the keep-away zone.

Effects of TSV Structure and Arrangement

The dependence of the equivalent strain on the TSV diameter is shown in Fig. 5a, considering the effects of the diameter difference between the TSV and the bonding. Small TSV diameter proved to be the only factor that decreased the thermal strain at the TSV. It is also noteworthy that small diameter difference between the TSV and the bonding was a primary factor to decrease the thermal strain at the bonding. When the TSV diameter was 8 μm, the diameter difference was 22 μm because the bonding diameter was fixed at 30 μm. As the TSV diameter increased, the equivalent strain at the TSV increased, which means that the deformation of Cu at the TSV increased. This is due to the fact that increasing the amount of Cu results in more thermal strain, which is then localized at the edge of the TSV, similar to the result for the bonding diameter. In other words, the equivalent strain at the TSV reduced to near zero for small TSV diameter because the amount of Cu, which induces thermal strain, decreased. This result of the dependence of the strain on the TSV diameter is similar to a previously reported result.[17] We also found a correlation between the TSV and the bonding diameter that affects the thermal strain at the bonding. The equivalent strain at the bonding decreased as the TSV diameter increased. This is because the diameter difference between the TSV and the bonding decreased when the TSV diameter increased. This tendency is similar to the result for the bonding diameter dependence, as shown in Fig. 2a, in which the equivalent strain at the bonding increased as the diameter difference increased. From these

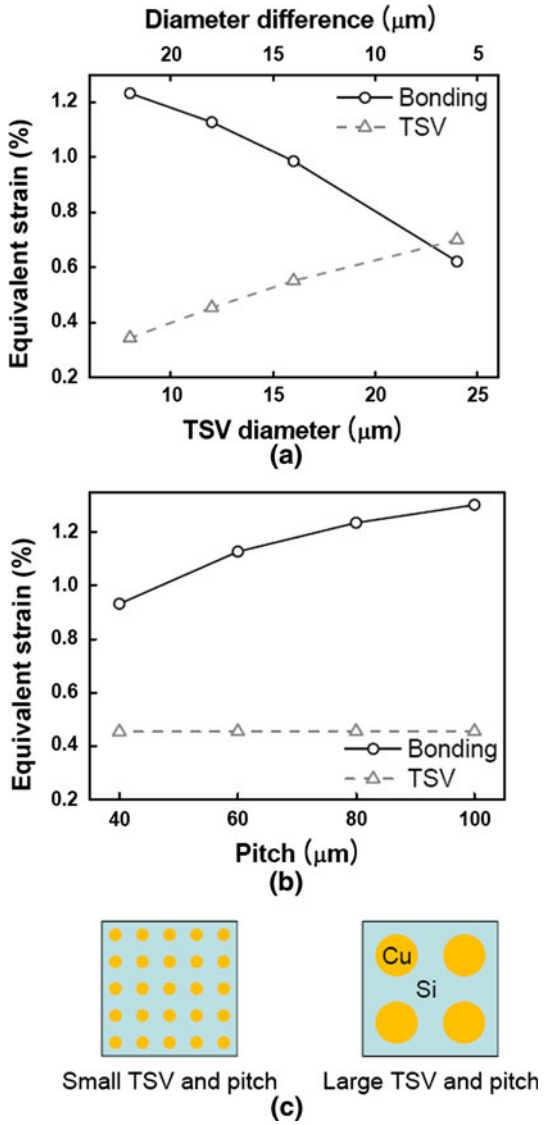

Fig. 5. Variation in equivalent strain at the bonding and the TSV as a function of (a) TSV diameter and diameter difference, and (b) pitch. (c) Schematic diagram of small TSVs and pitch versus large TSVs and pitch for a fixed amount of Cu per unit volume.

results, it can be concluded that this diameter difference is the important factor that affects the thermal strain at the bonding.

Small pitch was also important to decrease the thermal strain at the bonding, as shown in Fig. 5b. The equivalent strain at the bonding increased when the pitch became longer. This result is similar to a previous result.[17] The strain increased because of the decrease in the number of TSVs and bondings per unit volume. The PCB generates significant thermal strain by pulling or pushing the whole 3D IC structure. The bonding is composed of Cu, which has relatively large elastic modulus, playing an important role in withstanding the thermal strain induced by PCB. When the pitch increased, the number of bondings per unit volume decreased, and then fewer bondings had to withstand the same thermal strain. Therefore, the thermal strain that each bonding had to withstand was increased.

Additional analyses were performed to consider the case in which the TSV diameter, bonding diameter, and pitch were changed together but with the amount of Cu per unit volume fixed. A schematic diagram of this case is shown in Fig. 5c. Considering the dimensions and arrangement of the TSV, small TSV diameter and pitch were important to decrease the thermal strain at the TSV and the bonding. The equivalent strain at the bonding was 0.45% when the TSV diameter, bonding diameter, and pitch were 4 μm, 12 μm, and 20 μm, respectively. On the other hand, the equivalent strain at the bonding increased from 0.45% to 1.5% when the TSV diameter, bonding diameter, and pitch became 16 μm, 40 μm, and 80 μm, respectively. From these results, it is concluded that small TSV and bonding diameter and narrow spacing between the TSVs are needed to minimize deformation, although this is difficult to fabricate because a small via hole has narrow spacing to be etched, and filling it with Cu is costly and requires more advanced technology.

Figure 6 shows that the effects of TSV height and the number of die stacks were not significant. These are matters of interest regarding the vertical structure of stacked wafers. The equivalent strain at both the TSV and the bonding did not change as the TSV height increased, as shown in Fig. 6a. The change in the TSV height did not affect the thermal strain even at the other points. The equivalent strain did not change significantly even when the number of die stacks increased, as shown in Fig. 6b. These results are due to the effect of the underfill. The underfill has the lowest elastic modulus in the 3D IC, and it acts as a buffer against thermal strain. It is concluded that variations in the thickness direction (z-direction), such as the TSV height and the number of die stacks, except for the bonding thickness, can be ignored when considering the thermal strain. This result is an important discovery that clarifies the dependence of thermal strain on variations in the thickness direction.

Figure 7 shows the equivalent strains at the bonding according to the TSV height and the number of die stacks with the air gap, compared with those with underfill. It was revealed that the underfill is an important factor for decreasing the thermal strain with various geometric parameters. When considering the air gap, the thermal strain at the bonding increased by more than three times. The maximum increase was seven times. The slopes of equivalent strain were also steeper with air gap than with underfill, especially in the case of TSV height. The equivalent strain with the air gap significantly increased from 5% to 7% when the TSV height increased, as shown in Fig. 7a. However, the equivalent strain with the underfill did

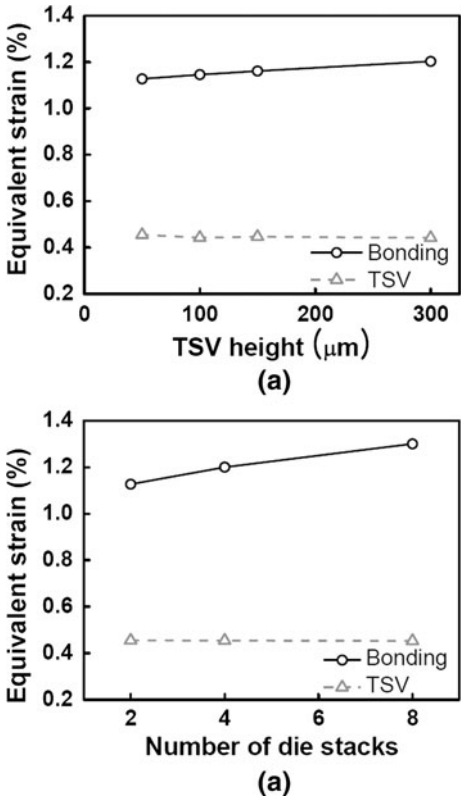

Fig. 6. Equivalent strain change at bonding and TSV as a function of (a) TSV height and (b) number of die stacks.

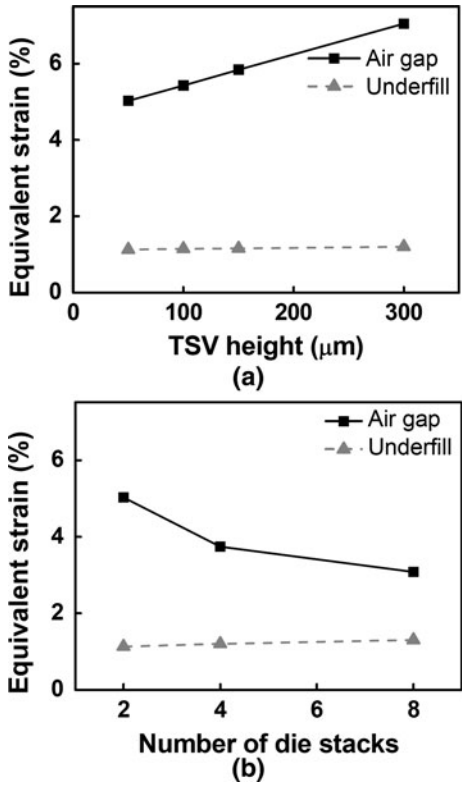

Fig. 7. Equivalent strain change at the bonding with the air gap and the underfill as a function of (a) TSV height and (b) number of die stacks.

not change. This increase is because the thickness of the bonding became relatively thin, compared with the Si. In the analysis of the bonding thickness, the thickness of the bonding itself became thin, which made the thickness of the bonding relatively thin, compared with both the Si and the PCB. This is why the equivalent strain increased even with the underfill when the bonding thickness became thin.

The equivalent strain with the air gap decreased when the number of die stacks increased, as shown in Fig. 7b. The overall equivalent strain at the bonding with the air gap increased. The equivalent strain with the air gap decreased from 5% to 3% when the number of die stacks increased, whereas the equivalent strain with the underfill did not change significantly. This is because the thickness of the bonding increased together with the number of bondings when the number of die stacks increased. The thickness of the bonding became relatively thick, compared with the PCB. Therefore, the equivalent strain decreased with the number of die stacks. From these results, it is concluded that the underfill eliminates the change of the thermal strain with geometric parameters when the thickness of the bonding became relatively thin, compared with either the Si or the PCB. It is noteworthy that these results show that the underfill acts as a buffer against the thermal strain, especially for variations in the thickness direction such as the TSV height or the number of die stacks.

CONCLUSIONS

The effects of various dimensional variables on the stress in Si and Cu in a 3D IC were investigated using finite-element analysis, and the following conclusions were drawn: The equivalent strain of Cu at the bonding increased as the diameter difference between the bonding and the TSV increased. The thin bonding also significantly increased the equivalent strain at the bonding. The only factor that affected the strain at the TSV was the TSV diameter. The TSV diameter should be reduced to decrease the strain at the TSV. Variations in the thickness direction (z-direction), such as the TSV height and the number of die stacks, did not affect the thermal strain significantly due to the underfill. The underfill decreased the overall equivalent strain at the bonding. In the case of the keep-away zone, the important geometric factor was the bonding diameter. A small bonding diameter is required to decrease the keep-away zone. The keep-away zone also decreased when the depth from the Si surface increased. These results suggest that smaller bonding diameter, TSV diameter, and pitch should be prepared to reduce thermal strain and decrease the keep-away zone.

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