Journal of ELECTRONIC MATERIALS, Vol. 40, No. 7, 2011
DOI: 10.1007/s11664-011-1623-z

Mobility Enhancement Technology for Scaling of CMOS Devices: Overview and Status

YI SONG,[1,2] HUAJIE ZHOU,[1] QIUXIA XU,[1] JUN LUO,[1] HAIZHOU YIN,[1] JIANG YAN,[1] and HUICAI ZHONG[1]

1.—Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China. 2.—e-mail: songyi@ime.ac.cn

The aggressive downscaling of complementary metal–oxide–semiconductor (CMOS) technology to the sub-21-nm technology node is facing great challenges. Innovative technologies such as metal gate/high-k dielectric integration, source/drain engineering, mobility enhancement technology, new device architectures, and enhanced quasiballistic transport channels serve as possible solutions for nanoscaled CMOS. Among them, mobility enhancement technology is one of the most promising solutions for improving device performance. Technologies such as global and process-induced strain technology, hybrid-orientation channels, and new high-mobility channels are thoroughly discussed from the perspective of technological innovation and achievement. Uniaxial strain is superior to biaxial strain in extending metal–oxide–semiconductor field-effect transistor (MOSFET) scaling for various reasons. Typical uniaxial technologies, such as embedded or raised SiGe or SiC source/drains, Ge pre-amorphization source/drain extension technology, the stress memorization technique (SMT), and tensile or comprehensive capping layers, stress liners, and contact etch-stop layers (CESLs) are discussed in detail. The initial integration of these technologies and the associated reliability issues are also addressed. The hybrid-orientation channel is challenging due to the complicated process flow and the generation of defects. Applying new high-mobility channels is an attractive method for increasing carrier mobility; however, it is also challenging due to the introduction of new material systems. New processes with new substrates either based on hybrid orientation or composed of group III–V semiconductors must be simplified, and costs should be reduced. Different mobility enhancement technologies will have to be combined to boost device performance, but they must be compatible with each other. The high mobility offered by mobility enhancement technologies makes these technologies promising and an active area of device research down to the 21-nm technology node and beyond.

Key words: Nanoscale CMOS device, mobility enhancement technology, process-induced strain, high-mobility channel

INTRODUCTION

In the past half-century, the integrated circuit (IC) industry has been growing rapidly, benefiting from the dimensional downscaling of transistors according to Moore's law as well as larger wafer sizes. This downscaling results in higher performance, lower power consumption, more complex functionality, faster device speeds, and lower cost per transistor. As the feature size of MOSFETs shrinks down to sub-21-nm nodes, CMOS technology faces tremendous challenges, including severe short-channel effects (SCEs), degraded drive

(Received April 18, 2010; accepted March 6, 2011; published online May 15, 2011)

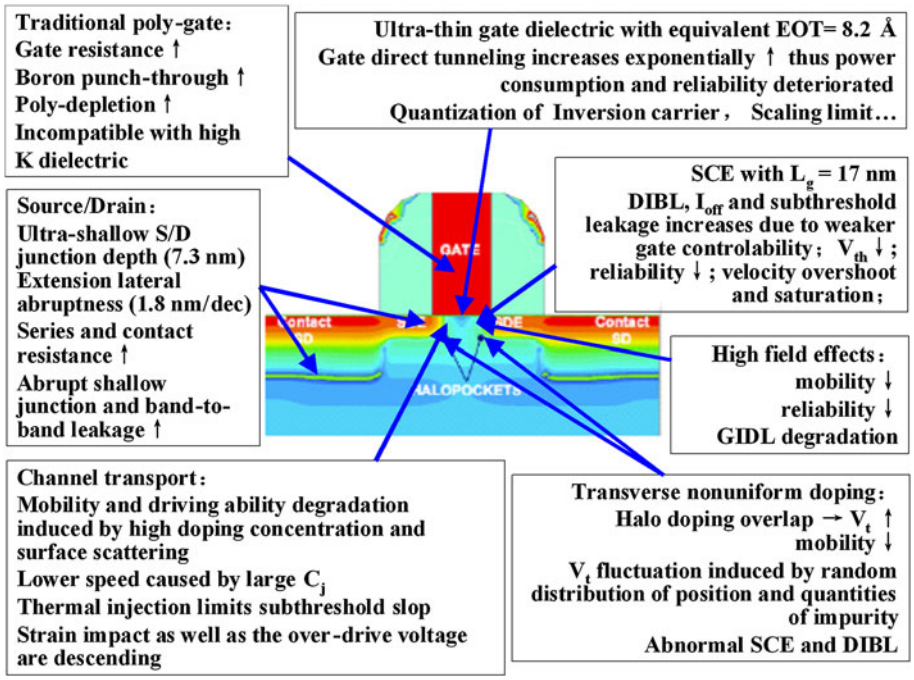

Fig. 1. Main challenges for CMOS technology at the 21-nm technology node. DIBL: drain induced barrier lowering.

Table I. High-performance logic technology requirements for extended planar bulk at the 21-nm technology node as predicted by ITRS 2009 edition

MPU physical gate length (nm)	Mobility enhancement factor due to strain	Electrical equivalent oxide thickness in inversion (Å)	Maximal gate leakage current density (kA/cm^2)
17	1.8 (nMOS)/2.3 (pMOS)	8.2	1.3

Average V_{dd} (V)	Maximal I_{on}/I_{off} (μA/μm)	Saturated threshold voltage (V)	Intrinsic delay (ps)
0.81	1680/0.1 (nMOS), 1377/0.1 (pMOS)	|0.302|	0.45 (nMOS)/0.55 (pMOS)

MPU: Micro processor unit.

capability, boron penetration and polysilicon depletion, high-field effects, direct gate tunneling current, and high series resistance. Unprecedented difficulties must be overcome if Moore's law is to be followed. Figure 1 summarizes the main challenges in the scaling of traditional planar bulk MOSFETs, and Table I provides the main projected targets for high-performance logic technology at the 21-nm technology node, as predicted by the *International Technology Roadmap for Semiconductors* (ITRS).[1]

As channel gate lengths are scaled down to the sub-21-nm range, mobility degradation becomes more severe, though mobility still effectively describes FET performance in the quasiballistic conduction state for the overall consideration of different degradation mechanisms.[2] The degradation of carrier mobility and SCEs caused by ultra-high and nonuniform channel doping, high surface scattering, and vertical electric fields makes mobility enhancement engineering the most important technique in improving device performance.[3] Three common mobility enhancement methods are (1) uniaxial strain through stress liners, embedded SiGe source/drain for pMOS and SiC source/drain for nMOS, stress memorization or biaxial global strain generated by epitaxial growth of a thin Si layer on top of a relaxed SiGe substrate; (2) the adoption of a hybrid-orientation substrate; and (3) the utilization of group III–V materials or pure germanium as the channel. Mobility enhancement technologies are still effective, even in the ballistic region, where ballistic efficiency and the injection velocity can be increased.[4]

In the following sections of this paper, various mobility enhancement technologies will be thoroughly reviewed, and possible future trends will also be discussed.

GLOBAL (BIAXIAL) AND PROCESS-INDUCED (UNIAXIAL) STRAIN

The introduction of stress into a silicon channel is desirable because of its low cost, compatibility with traditional CMOS processing, and high efficiency compared with new channel materials with high mobility, such as Ge and III–V materials. There are two major techniques to exert strain on a Si channel: imposing global biaxial strain on the entire wafer and locally applying uniaxial strain to certain areas.

Global Biaxial Strain

In Fig. 2, the biaxial tensile strain at an interface, induced by the crystal lattice mismatch between Si and SiGe, can be realized either by growing a thin Si layer on a relaxed SiGe substrate epitaxially[5] or growing strained silicon directly on an insulator by a bond and etch-back technique.[6] Consequently, in the energy band of the strained Si, the sixfold-degenerate valleys are split into two sets of twofold and fourfold bands, giving rise to enhanced carrier transport. Furthermore, the repopulation of the energy bands and the reduction of intervalley phonon scattering boost carrier mobility significantly, especially for bulk nMOSs.[7] Biaxial strain can also be introduced by SiGe-free strained silicon-on-insulator (SOI) technology, which uses a wafer bonding technique. Devices fabricated using this method are free of high off-state leakage due to the elimination of dislocation cores at the strained Si/SiGe interface.[8,9] It was demonstrated that nMOSs exhibit a 112% electron mobility enhancement and nearly ideal subthreshold slopes of 66 mV/dec.[10]

Biaxial global strain technology possesses inherent and obvious drawbacks, however, which make it difficult to implement in practice. First, when the Ge content (%) reaches a moderate value, the electron mobility enhancement will saturate. Moreover, this mobility enhancement will be significantly impaired at high electric fields due to surface roughness scattering. Additionally, to enhance the mobility for holes, high Ge contents (>30%) are usually required, which conflicts with the moderate Ge content requirement for electron mobility enhancement. Therefore, the compromise in mobility enhancement between electrons and holes remains a significant challenge.[11] Complex processes, defects, high costs, and self-heating effects arising from the low thermal conductivity of SiGe also limit its applicability.

As device dimensions shrink, strain is, however, offset by the augmented effective field and corresponding quantum confinement effects, which lead to reduced hole mobility. Moreover, at high processing temperatures, the strain will be released in the form of dislocations, and Ge may diffuse into the strained Si layer or even further to the interface of the strained Si/gate dielectric layer, which narrows the processing window of the thermal budget.

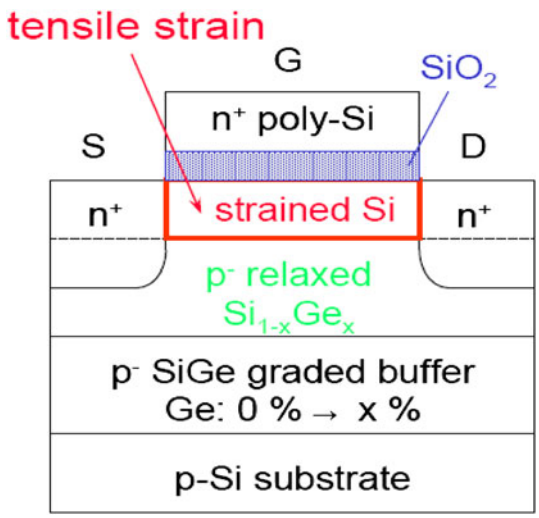

Fig. 2. nMOS with strained Si channel grown epitaxially on relaxed SiGe substrate (Reprinted from Ref. 11 with permission. Copyright 2001, IEEE publisher).

Uniaxial Process-Induced Strain

With respect to aggressively downscaled MOSFETs, uniaxial strain is superior to biaxial strain in the following aspects: (1) Uniaxial stress can offer high hole mobility enhancement in both low strain and high vertical electric fields due to additive strain and confined splitting, larger two-dimensional in-plane density of states, and smaller conductivity mass;[12] (2) Uniaxial stress-enhanced electron and hole mobilities mainly arise from reduced conductivity effective mass[13] versus reduced scattering for biaxial stress. Therefore, uniaxial stress provides larger drive current improvement for nanoscaled short-channel devices with minimal increases in manufacturing complexity.[14] (3) Uniaxial stress causes *n*-channel threshold voltage shifts that are approximately five times smaller[15] and, thus, do not require adjustment in substrate doping. (4) Process-induced uniaxial stress increases with decreasing channel length.[16] (5) A uniaxially strained device shows much better reliability.[17] (6) Smaller leakages arise from reduced bandgap narrowing, as compared with biaxial tensile stress, which causes much greater band-to-band tunneling (BTBT) leakage.[18] (7) Significantly less strain (5×) is required for hole mobility enhancement when applying longitudinal uniaxial compression versus in-plane biaxial tension using the conventional SiGe substrate approach. Therefore, process-induced uniaxial stress is very promising for scaling down CMOS technology as per the goals of the proposed roadmap.

However, the drawbacks of uniaxial stress (e.g., the localized stress dependence on device size and defects from additional processes) may affect the overall performance and must be addressed carefully.

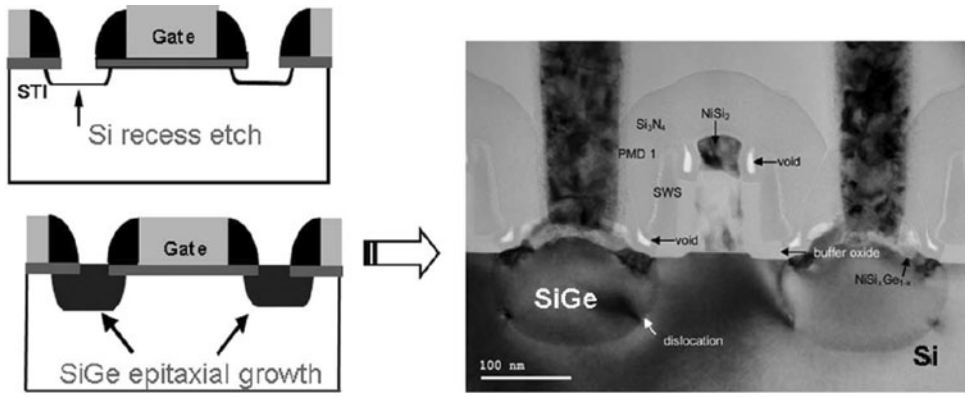

Fig. 3. Formation of embedded source/drain regions (left panel) and a cross-sectional transmission electron microscopy image of a pMOS transistor with an embedded SiGe stressor (right panel). (Reprinted from Ref. 16 with permission. Copyright 2006, IEEE publisher).

Uniaxial stress introduced from manufacturing processes, such as shallow-trench isolation (STI)[19] or silicidation, have already been implemented at the 90-nm technology node.[20] However, STI-originated stress causes both dislocations and electron mobility degradation as well as increased junction leakage as a result of bandgap narrowing.[21] Moreover, the gate direct tunneling current of holes in the inverted regime increase as STI-induced stress increases, as the growth of the gate oxide is slowed by the stress.[22] Therefore, uniaxial stress introduced by STI and silicide may need to be suppressed[23] to suppress junction leakage.[24]

Other promising ways to induce uniaxial strain, such as use of a stress nitride contact etch-stop layer (CESL)[25,26] in the recessed source/drain regions filled with SiGe for pMOSs[27] and SiC for nMOSs, and the stress memorization technology[28,29] for nMOSs, are discussed below.

Embedded or Raised SiGe and SiC Source/Drain

Figure 3 shows one way to fabricate an embedded or raised SiGe/SiC source/drain. First, the source/drain regions are etched to form recessed regions. Then, SiGe (pMOS) or SiC (nMOS) grows epitaxially in the recessed regions. A 35% improvement in the drive current of pMOSs with embedded SiGe source/drain was demonstrated.[30]

To drive Ge deeper into the source/drain regions and, thus, further increase the strain, a local Ge condensation technique without recessed etching was proposed.[31,32] The key to this technique is selective epitaxial growth (SEG) of $Si_{0.7}Ge_{0.3}$ in the source/drain regions, followed by dry oxidation at 950°C or higher to drive Ge into the source/drain regions. The embedded SiGe induces lateral compressive stress, which leads to the reduction in the effective mass of holes and consequently a significant saturation drive current enhancement of 38%.[33]

Regarding the application of $Si_{1-x}Ge_x$ stressors, trade-offs between performance and leakage as a function of $Si_{1-x}Ge_x$ depth, Ge concentration, process sequence, geometry, and layout must be considered carefully.[32,34] Although deeper $Si_{1-x}Ge_x$ layers, higher Ge concentration, and higher source/drain elevation result in larger strain, the leakage simultaneously increases because SiGe approaches the metallurgical junction. Implantation and annealing after SiGe regrowth is not desirable because of the high junction leakage induced by bandgap narrowing due to the Ge mole fraction as well as the compressive stress in SiGe. The improvement in the current is also sensitive to the orientation of the Si channel because the piezoresistance is directional.

With a longitudinal compressive stress above 1 GPa in the channel, a low-field mobility enhancement of 140% is observed. This significant improvement is explained by band repopulation and transverse mass modulation.[35]

The incorporation of a Si:C stressor in source/drain regions could exert lateral tensile stress in the channel, which is beneficial to nMOSs. A straightforward approach is to recess the source and drain regions by etching and then deposit Si:C using a selective epitaxial process.[36] High-performance nMOSs with epitaxially grown phosphorus-doped SiC source/drain stressors have been demonstrated.[37] SiC strain is fully preserved through epitaxial-last processes with only one laser annealing step, and low parasitic resistance is achieved by *in situ* phosphorus-doping (3×10^{20} cm^{-3} to 4.8×10^{20} cm^{-3}) and intimate stressor-to-channel proximity (10 nm to 20 nm). A mobility enhancement of 13% and a corresponding on-current enhancement of 9% in control devices with gate lengths of 60 nm have been achieved. Furthermore, the Si:C stressor and tensile stress liner (TL) are integrated at the 45-nm node. The ground rules and processes involved in the aforementioned techniques are shown in Fig. 4. nMOSs with Si:C stressors (1.9% substitutional C and 3×10^{20} cm^{-3} P) showed a 25% enhancement in mobility and 9% enhancement in on-current over the best 45-nm node baseline using the stress memorization technique (SMT) and tensile liner stressors.[38]

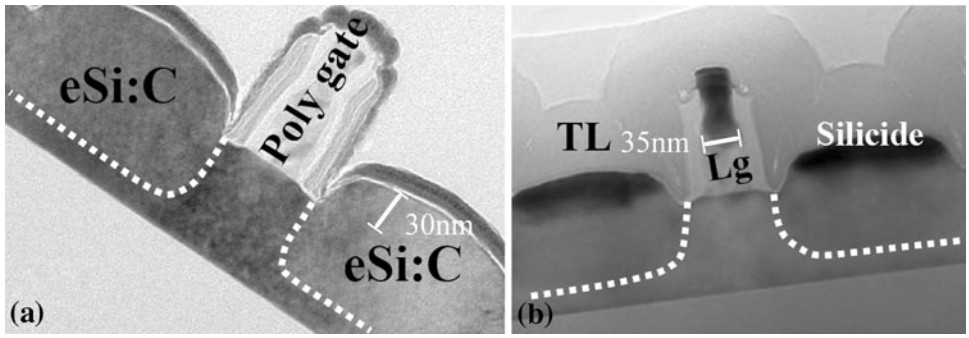

Fig. 4. Cross-sectional transmission electron microscopy (TEM) images of typical eSi:C poly-gate nMOS device: (a) post epitaxial growth and (b) post device fabrication to first metal (M1) (Reprinted from Ref. 38 with permission. Copyright 2008, IEEE publisher).

The critical issue in enabling eSi:C stressors for high-performance nMOSs with short channels and thin gate oxides is the source/drain extension doping concentration, which strongly affects the extension structural and electrical connectivity. The drawbacks of *in situ*-doped SiC stressor technology are also evident. It is difficult to grow Si:C stressors with $[C]_{sub} > 1$ at% due to the extremely low solid solubility of C in Si; it is also difficult to keep C atoms at substitutional sites during thermal processing, which causes stress loss. Recently, solid-phase epitaxy (SPE) has provided an excellent way to fabricate nMOSs with eSi:C stressors. For SPE growth of eSi:C stressors, C is first implanted into a Si substrate, and then an amorphous layer with C atoms is formed. Upon thermal treatment at low temperature, the amorphous layer will completely regrow with C atoms at the substitutional positions.[39] A tensile stress of 615 MPa was generated in a channel with a record high 1.65 at.% substitutional C concentration in the source and drain regions, resulting in a 35% improvement in electron mobility.

Ge Pre-amorphization Source/Drain Extension Technology

Germanium pre-amorphization implantation (PAI) for source/drain extension of pMOSs is a meaningful method for maintaining a high effective hole mobility at a high vertical electric field. An improvement of up to 32% in the effective mobility of holes is obtained at a vertical electric field of 0.6 MV/cm for a pMOS with a gate length of 90 nm, as shown in Fig. 5.[40] The scalability of this technique has been demonstrated without any influence on electron mobility. source/drain extension implantation is performed by Ge PAI and low-energy implantation after offset spacer formation. The Ge PAI method not only suppresses boron ion channeling but also improves the activation efficiency of boron. This leads to a 38% and 109% improvement in junction depth and surface concentration, respectively. More importantly, the Ge PAI method also introduces a large uniaxial compressive stress in the channel, which significantly improves the hole mobility. As an ion implantation process, the dose and energy of Ge implantation should also be optimized carefully to balance between strain effects and the leakage of ultrashallow junctions.

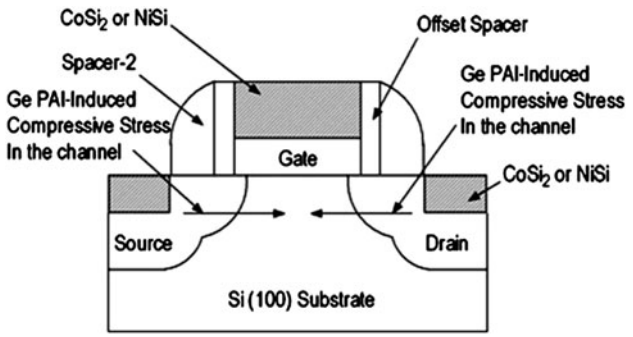

Fig. 5. Schematic of a strained-channel pMOS with uniaxial compressive stress of the channel induced by Ge PAI for source/drain extension (Reprinted from Ref. 40 with permission. Copyright 2008, IEEE publisher).

An improvement in the effective hole mobility of up to 43% has been achieved for a pMOS with a 35-nm gate length and optimized Ge PAI with a vertical effective field of 1.1 MV/cm. A significant comprehensive strain of up to −3.0% has been confirmed by zero-order Laue zone diffraction with large-angle convergent-beam electron diffraction patterns in a transmission electron microscope. The depth profiles of residual compressive strain and shear strain in the channel are also shown.[41] By using Ge PAI, a high-performance CMOS of 22-nm-gate-length, and well behaved 32 dividers embedded with a 201-stage ring oscillator based on the 27-nm-gate-length CMOS technology, have been fabricated. The strained channel induced by Ge PAI for source/drain extension demonstrates that this technique is simple, low cost, and highly manufacturable.

Stress Memorization Technique (SMT)

As a design rule, such as for the shrinking of gate pitch, the effects of stress liners and epitaxial SiGe growth in the source/drain regions are weakened because of reduced source/drain areas. Therefore, the SMT is emerging as a way to overcome the drawbacks of stress liners and epitaxial stressors. As shown in

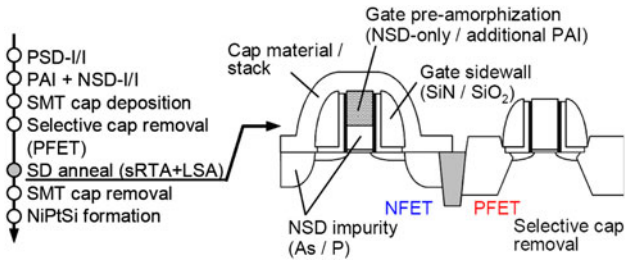

Fig. 6. Typical process sequence and key process parameters of the selective SMT for nMOS. NSD: NFET source/drain, PSD: PFET source/drain (Reprinted from Ref. 43 with permission. Copyright 2008, IEEE publisher).

Fig. 6, the SMT for nMOS devices is introduced by selective deposition of a high-tensile nitride layer on an n^+ poly-Si gate electrode as a stressor with poly-amorphous implantation performed in advance. This high-tensile nitride capping layer is removed after poly-recrystallization and source/drain activation. A current drivability improvement greater than 15% has been obtained for nMOSs due to the memorized strain underneath the poly-gate electrode without any degradation of the pMOS.[42]

Grain growth leads to gate volume expansion, which induces large stresses in polysilicon. The memorized stress in the poly-gate results in high vertical compressive strain in the channel.[43] Because P diffuses into the channel, deteriorating the short-channel effects, it is not suitable as an n-type impurity. Using additional laser-spike annealing (LSA) after spike rapid thermal annealing (RTA) for SMT annealing, a thicker SMT layer and sidewall spacer materials with high Young's moduli will induce larger stain; however, physical damage to the gate oxynitride is also induced. Therefore, compromises between larger strain and lower leakage are required. Optimized PAI conditions and tilted buffer implantation technique are required to suppress implantation damage to the upper part of the sidewalls and the defects at the sidewall edges.

When SMT applied to an initially low-stress film, its stress significantly increases after spike annealing. This distinct shift in stress effectively memorizes the stress in the poly-Si gate; additionally, it reduces the gate leakage of an nMOS because the grain size changes during the SMT process, affecting the interface between poly-Si and the gate oxide, which modulates the barrier height in poly-Si.

The layout dependency of the SMT is small due to uniform strain across the channel, which makes the SMT suitable to be integrated into aggressively scaled CMOS with tight scaling rules. The SMT does not degrade V_{th} mismatch, and the T_{pd}–power curve is shifted to the left, which denotes a lower standby power.[44,45]

A surprising discovery was that the performance improvement of nMOSs is not related to the intrinsic stress level of the nitride layer but merely relates to the SiN porosity. As the density and Young's modulus of SiN increase, the stress created in the poly-Si gate increases, which is more beneficial to an nMOS. Reducing either the gate length or width is significantly helpful for the stress level as well as the transconductance. Reducing the gate pitch, however, will impair drive current gain because of the lower SiN layer rigidity between two neighboring gates with reduced SMT efficiency.

The incorporation of the SMT into CMOS fabrication should ideally improve the performance of an nMOS without degradation of pMOS. Selective removal of the capping tensile layer in a pMOS requires four additional process steps, including a specific lithography step, which significantly complicates the fabrication process. By optimizing the properties of the capping nitride, dopant activation, and poly-Si gate mechanical stress, a novel SMT for 45-nm CMOS with neither additional steps nor masks was proposed,[46] displaying a performance improvement of 7% for nMOS and no performance degradation for pMOS. The possible performance degradation of a pMOS (i.e., reduction in the inversion capacitance slope and increase in subthreshold slope) is attributed to hydrogen within the capping oxide, which cannot be flushed out due to the SiN capping layer, causing B deactivation and exodiffusion, as shown in Fig. 7a. A porous SiN layer with a high deposition temperature can prevent the performance degradation of pMOS due to the removal of H, as shown in Fig. 7b.

Recently, Ortolland claimed that the degradation of pMOS is not simply due to strain effects but is strongly influenced by the hydrogen content of the SMT stressor layer. Based on this assumption, a maskless SMT process without pMOS performance degradation (Fig. 8) has been proposed.[47] The key to this technique is to utilize an ultraviolet (UV)-cured nitride stressor with a low concentration of hydrogen in conjunction with optimized channel orientation to avoid the degradation of pMOSs while maintaining the performance improvement of nMOSs. X-ray diffraction (XRD) results show that the performance gain in an nMOS results not only from the mechanical stress created in the poly-Si gate during SMT processing but also from the additional contribution of the source/drain regions.

Stress Liners as a Contact Etch-Stop Layer

The introduction of a strain CESL (tensile and compressive liners for nMOSs and pMOSs, respectively) is an efficient way to enhance mobility. A CESL with intrinsic tensile stress tends to shrink; however, the shrinkage is counteracted by the stress induced in the source/drain, gate, and spacer regions, as the CESL is restrained within these regions. The stress in the source/drain, spacer, and gate regions is finally transferred to the channel. For the case of intrinsic tensile stress, the CESL expands the poly-gate and the channel regions, resulting in tensile stress in the channel. On the

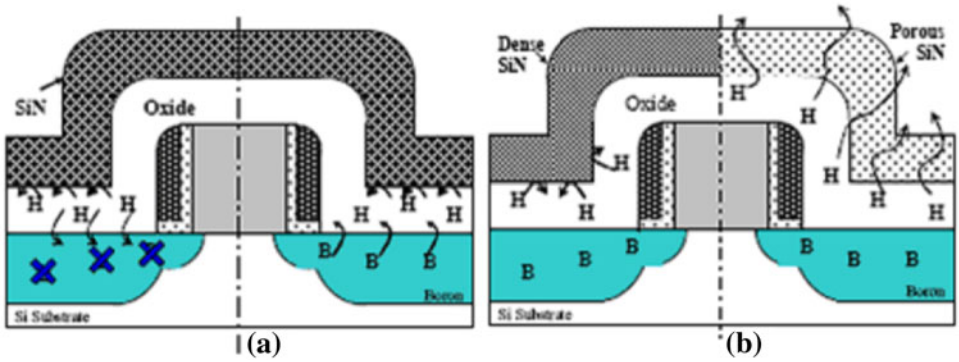

Fig. 7. (a) Schematic representation of hydrogen effects on boron deactivation and exodiffusion; (b) schematic representation of nitride with/without hydrogen flush through (Reprinted from Ref. 46 with permission. Copyright 2006, IEEE publisher).

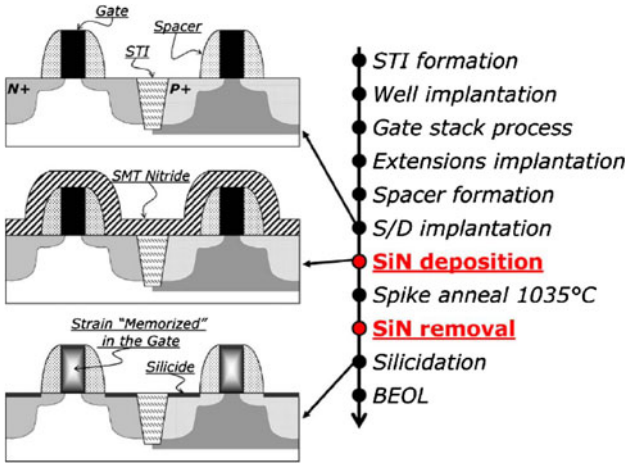

Fig. 8. Schematic illustration of the maskless SMT process without degradation of pMOS performance. BEOL: back end of the line (Reprinted from Ref. 47 with permission. Copyright 2009, IEEE publisher).

sidewall of the spacers, the vertical shrinkage of the CESL leads to compression of the poly-gate region, which, in turn, produces compressive vertical stress in the gate material and channel. It is worth noting that CESL technology is not compatible with source/drain stressors such as $Si_{1-x}Ge_x$ and $Si_{1-x}C_x$ for reduced gate topography. An intrinsic tensile (compressive) stress in a CESL results in a tensile (compressive) parallel stress in the channel and a compressive (tensile) vertical stress. A thicker CESL leads to larger channel stress, but the stress starts to saturate for CESLs thicker than 40 nm to 50 nm.[48] A parallel tensile stress and a vertical compressive stress induced by a CESL with intrinsic tensile stress are favorable for electron mobility, whereas only the parallel stress induced by a CESL with intrinsic compressive stress is helpful for enhancement of hole mobility. It is crucial that the spacer width is scaled proportionally to the gate length in order to reduce the layout sensitivity of both the vertical and parallel stress and to preserve the highest possible stress level in the densest layouts.

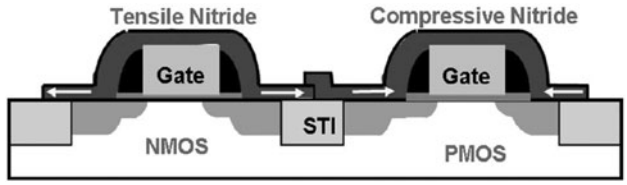

Fig. 9. Dual stress liner process architecture with tensile and compressive silicon nitride capping layers (Reprinted from Ref. 16 with permission. Copyright 2006, IEEE publisher).

A novel method for depositing a liner-stressor material composed of diamond-like carbon (DLC) with a very high intrinsic compressive stress up to 6 GPa is applied to FinFETs.[49] An enhancement above 30% in I_{dsat} is observed for FinFETs with a 20-nm-thick DLC liner stressor over control devices, which is attributed to the coupling of compressive stress from the DLC liner to the channel. The physical origin of hole mobility enhancement has proven to be the small effective mass of the top valence band rather than any scattering modification; this mobility gain is maintained even at high electric field.[50]

Plasma-enhanced chemical vapor deposition could be used to produce a SiN CESL. The intrinsic stress in the SiN CESL could be modulated using different radiofrequency (RF) powers or thicknesses. A highly tensile-strained layer with 1.2 GPa of pressure and a highly compressive-strained layer with −1.8 GPa of pressure have been demonstrated to be responsible for the performance enhancement (10% for nMOS, 17% for pMOS).[51] Strain edge effects are dominant when the gate length is extremely small, whereas stress becomes less tensile for larger devices. The strain in the channel is also strongly dependent on geometrical parameters (W, L_{gate}).

Efforts to integrate strain in CMOS could resort to dual CESL technology, as illustrated in Fig. 9.[52] The tensile and compressive SiN layer in nMOS and pMOS devices, respectively, are deposited sequentially and etched selectively. The resulting nMOS delivers an on-current of 1.05 mA/μm and an

off-current of 70 nA/μm at a 1-V drain bias. A pMOS exhibits a 66% increase in linear drain current and a 55% increase in saturation current. The improvement in the drain current for nMOS and pMOS devices depends on the channel doping concentration. Channel doping should be kept as low as possible to avoid deterioration of the improvement in drain current.

Complicated process steps are required in dual stress liner technology to enhance the drive currents for both nMOS and pMOS devices simultaneously. Therefore, a novel ultimate spacer process (USP) with a single stress liner has been developed, resulting in a 15% and 7% drive current improvement for nMOS and pMOS devices, respectively.[53] Except for the single USP step inserted into the salicide module for both nMOS and pMOS devices, the whole process is commonly exempt from extra lithography steps. In combination with the oriented channel and poly stressors, current increases of 25% for nMOSs and 35% for pMOSs are achieved

Combination of Different Strain Schemes

As the dimensional shrinkage of devices proceeds, different schemes must be combined together. Preliminary research has focused mainly on the combination of CESLs and source/drain stressors for CMOS integration, for example, SiGe stressors for pMOS and CESLs for nMOS.

By integrating a HfO_2/TiN/poly gate stack with a SiGe stressor and a compressive nitride CESL, as shown in Fig. 10,[54] an improvement of up to 65% for I_{dsat} has been demonstrated for pMOS devices. A 100-nm-thick CESL with 1.5 GPa of compressive stress is added after Ni silicidation in the typical epitaxy SiGe source/drain process. An on-current of 422 μA/μm and off-current of 20 pA/μm are obtained at V_{dd} = 1.1 V and 25% Ge concentration. Furthermore, a recessed $Si_{0.8}Ge_{0.2}$ stressor and compressive CESL have been successfully integrated, resulting in an 85% I_{dsat} improvement and a nearly 200% improvement in the hole mobility of a pMOS with a 70-nm gate length.[55]

The drive current improvements from recessed $Si_{0.8}Ge_{0.2}$ plus a compressive nitride layer are additive; furthermore, it has been shown that the mobility enhancement is a superlinear function of stress, leading to larger additive gains in drive current when combining several stress sources.

The most important step in CESL technology is the deposition of highly stressed nitride. During the deposition of a SiN film in an optimized plasma environment in combination with heavy-ion bombardment, an engineered compressive stress of 2.5 GPa could be used to form source/drain regions with SiGe stressors. A uniaxial compressive stress greater than 1 GPa and a drive current greater than 1 mA/μm have been achieved for pMOS devices.[56]

By adopting both compressive stress liners and embedded SiGe stressors, the achieved stress (as high as -2.4 GPa for pMOS devices) formed on (100) substrates is larger than that for pMOS devices formed on (110) substrates. These findings make CMOS integration with stressors on (100) substrates very promising.[57] Figure 11 shows the saturation velocity of holes as a function of effective gate length with and without stressors, strongly suggesting that the stress is additive, and the saturation velocity of holes on (100) substrates is larger than that on (110) substrates for pMOSs. When the effective gate length becomes shorter, the saturation velocity of holes on (100) substrates is superior to that on (100) substrates.

A two-step method for creating recessed SiGe stressors was developed to boost the performance of pMOS devices. The process flow is detailed in Fig. 12. The hole mobility, short-channel effects, and source/drain resistance of pMOSs are notably improved by carefully optimizing the device structure, such as the recess depth of source/drain extension (SDE) and source/drain offset spacer width.[58] The combination of SiGe stressors formed by a two-step method with compressive stress liners would lead to a further enhancement of perfor-

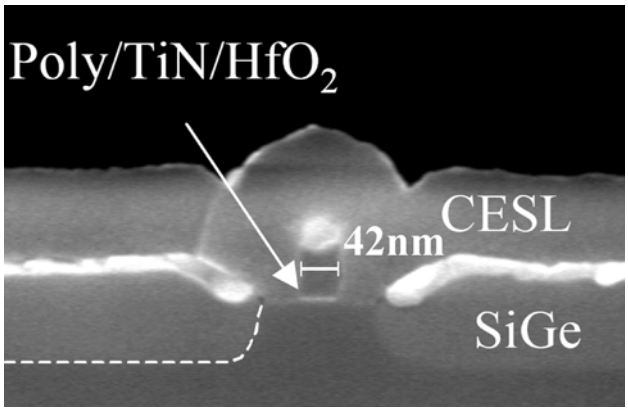

Fig. 10. Cross-sectional scanning electron microscopy (SEM) image showing SiGe in source/drain area, combined with a TiN and HfO_2 combination and CESL stress booster, showing a 42-nm-gate-length device (Reprinted from Ref. 54 with permission. Copyright 2005, IEEE publisher).

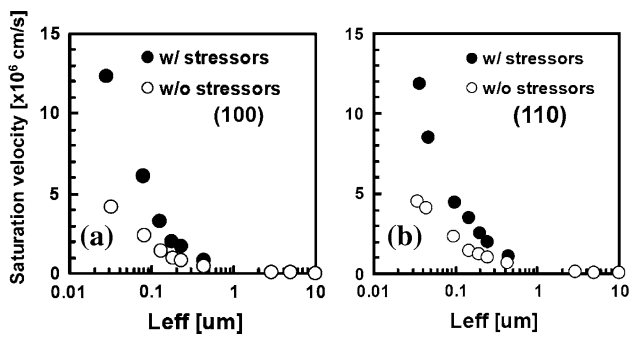

Fig. 11. Saturation hole velocity dependence on effective gate length (L_{eff}) for devices with and without stressors on (a) (100) and (b) (110) substrates (Reprinted from Ref. 57 with permission. Copyright 2009, IEEE publisher).

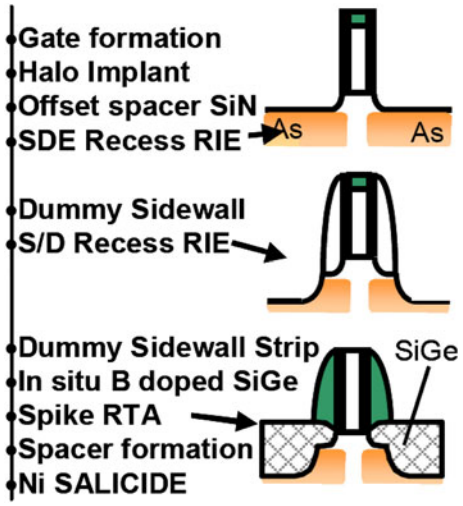

Fig. 12. Schematic flow of the two-step process for recessed SiGe source/drain (Reprinted from Ref. 58 with permission. Copyright 2006, IEEE publisher).

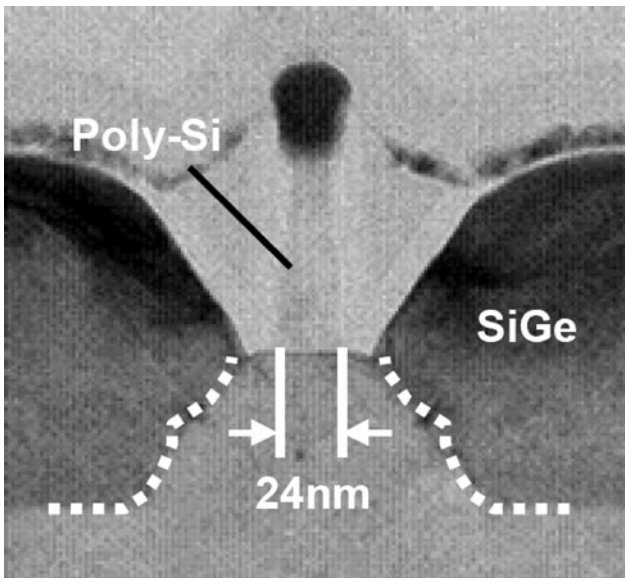

Fig. 13. Cross-sectional TEM of a pMOS device with a two-step recessed SiGe source/drain structure and compressive stress liner (Reprinted from Ref. 58 with permission. Copyright 2006, IEEE publisher).

mance.[59] A record-high drive current of 714 μA/μm at V_{dd} = 1.0 V and I_{off} = 100 nA/μm was reported by optimizing the source and drain overlap, defect control, and elevated SiGe stressor structure.[59] Figure 13 shows a cross-sectional TEM image of a pMOS with SiGe stressors formed by combining the two-step method with compressive stress liners.

Epitaxial SiGe stressors and tensile SiN CESL stressors are integrated to improve the performance of pMOS and nMOS devices simultaneously.[60] The saturated drive current of an nMOS and pMOS is increased by 10% and 25%, respectively. By carefully adjusting the stress in the capping layer for nMOS devices and adjusting the Ge concentration in SiGe stressors for pMOS devices, the strain level of each can be tuned independently. At large vertical electric fields, the hole mobility is increased by 50% because of the large longitudinal uniaxial compressive stress induced by SiGe stressors; at the same time, the tensile stress induced by the SiN capping layer does not degrade the hole mobility but enhances the electron mobility by 20%.

Reliability Issues

Due to the reorientation of the band structure caused by the strain, both nMOS devices with uniaxial tensile strain and pMOS devices with compressive strain show improved drive current. However, because of the introduction of additional processes and new materials that give rise to tensile or compressive strain, reliability issues may also arise.

With uniaxial tensile strain induced by a SiN cap layer on polysilicon gate/SiON oxide, a 15% improvement in the drive capability of nMOS devices has been demonstrated without degrading the noise performance.[61] The cap-layer-induced strain neither degrades the low-frequency drain noise nor increases the degradation rate in accelerated stress tests. Hot-carrier stress, bias-temperature instability, and time to breakdown are also robust in this type of strained device. No significant degradation of intrinsic negative-bias temperature instability (NBTI) behavior is observed because of post-oxide-growth process-induced strain on various gate stacks, such as poly-Si/SiON, TiN/HfO_2/SiO_2, and Ni fully-silicided (FUSI)/HfSiON/SiO_2.[62]

However, instead of the strain itself, it is the SiN CESL that influences device performance and reliability characteristics. Hydrogen passivation at the interface accounts for the deteriorated reliability characteristics.[63]

Compressive CESLs may worsen dynamic NTBI characteristics. This is attributed to the high hydrogen content within the SiN CESL layer as well as the high strain placed on the channel. A strong dependence on the alternating-current (AC) stress frequency is observed due to excess hydrogen content in strained devices. However, the NBTI instability of strained devices could be alleviated by operating at high frequency.[64]

The excess hydrogen content within SiN CESLs can also lead to increased substrate current and potentially aggravate hot-electron effects. The deposition of a tetraethyl orthosilicate (TEOS) buffer layer prior to that of a SiN CESL could block the diffusion of hydrogen and thus improve the hot-electron reliability.[65]

The increased strain has not been found to fundamentally limit hot-carrier reliability in submicron MOS technologies and can actually improve intrinsic hot-carrier lifetime.[66] However, the strain leads

to bandgap narrowing and an increase in the phonon mean free path,[67] both of which contribute to improved impact ionization. The improved impact ionization for short-channel pMOS devices with uniaxial strain is also ascribed to the strain-enhanced mobility. In this case, V_{dsat} becomes lower, which results in observable V_g-dependent enhancement in I_{sub}/I_d.[68]

The enhanced mechanical stress may degrade flicker noise characteristics, especially for pMOS devices, due to the trap states and dipoles generated by the stress. The flicker noise could be reduced, and the device performance could be improved, by optimizing the nitrogen profile in the gate dielectric (i.e., reducing the surface nitrogen concentration and increasing the total number of nitrogen atoms in the dielectric to prevent boron penetration from the gate electrode).[69]

For pMOS devices with HfO_2/TiN gate stacks, using a cap layer does not degrade the magnitude of $1/f$ noise. However, an increase in $1/f$ noise is found for pMOS devices with SiGe stressors, which results from additional traps created in high-k dielectrics during the epitaxial growth of SiGe stressors.[70] The applied stress does not directly correlate with the noise magnitude. For HfSiON/SiO_2 and a fully silicided gate stack, the $1/f$ noise is not affected by SiGe stressors, indicating that the embedded (source/drain) processing does not degrade the quality of the gate stack and that the intrinsic strain does not affect $1/f$ noise.[71]

Briefly, strain engineering, when properly characterized and implemented, has only a marginal impact on oxide quality and does not compromise long-term reliability. Strain has no intrinsic effect on $1/f$ noise.[72] For nMOS devices, CESL strain (uniaxial) is much better in terms of reliability, performance, and process simplicity, whereas pMOS devices with SiGe stressors have the drawback of Ge outdiffusion. Strained SOI requires special care due to its channel interface defects. Although they suffer from junction leakage, nMOS devices with SiC stressors show high drive capability. Therefore, SiC stressors with low defect densities are important for nMOS devices. As shown in Fig. 14, pMOS devices with SiGe stressors combined with embedded diffusion barriers (EDBs) exhibit much better NBTI characteristics as a result of the improved junction quality. Therefore, SiGe stressors seem to be promising in terms of performance and reliability, but SiGe channel exhibits worse NBTI and complex process characteristics.[17]

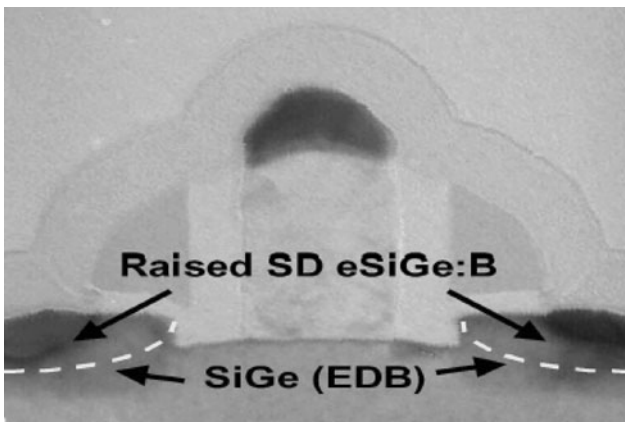

Fig. 14. Cross-sectional TEM image of epitaxial SiGe source/drain stressor formed by the EDB process (Reprinted from Ref. 17 with permission. Copyright 2008, IEEE publisher).

HYBRID-ORIENTATION CHANNEL

Because of the low oxide-interface charge density and the highest electron mobility, a silicon substrate oriented along the (100) crystalline plane is desirable for nMOS devices. However, the highest hole mobility occurs in Si(110) with a channel along the <110> direction; moreover, the peak mobility of Si(110) is more than twice than that of Si(100). Therefore, to take full advantage of electron and hole mobility simultaneously, nMOS devices should be fabricated on Si(100) and pMOS devices on Si(110).

Hybrid-orientation technology (HOT), in which wafer bonding and selective silicon epitaxy are utilized to improve the mobilities in both nMOS and pMOS devices simultaneously, as shown in Fig. 15, has been proposed.[73,74] Symmetrical performance of nMOS and pMOS devices is achieved by using this novel technology, so that area can be significantly saved. HOT is fully compatible with existing very large-scale integration (VLSI) technology in that no new material is introduced, and the device structure remains planar. Moreover, HOT is also compatible with dual stress liners, which further improve carrier mobility by local strain engineering.

There are many difficulties in fabricating pMOS devices on Si(110), such as channelling effects of dopants along the (110) axis. Furthermore, a higher density of surface atoms and available bonds on Si(110) compared with Si(100) leads to a higher interface trap density. Different surface properties also result in orientation dependence of oxidation and epitaxial deposition. To maximize the hole mobility, all gates of pMOS devices must be aligned along a single direction, because hole mobility is strongly anisotropic in Si(110).[12] Therefore, the ground rules of layout design must be modified. Fortunately, the impact of oxide-interface charge on threshold voltage and subthreshold slope decreases with gate oxide thickness. Because the nitrogen concentration in current gate oxides is increased and because of the expected introduction of high-k gate dielectric materials, the detrimental effects from surface orientation are diminishing.

Hybrid-Orientation Substrate Preparation

Hybrid-orientation substrates could be formed by layer transfer through a wafer bonding technique,

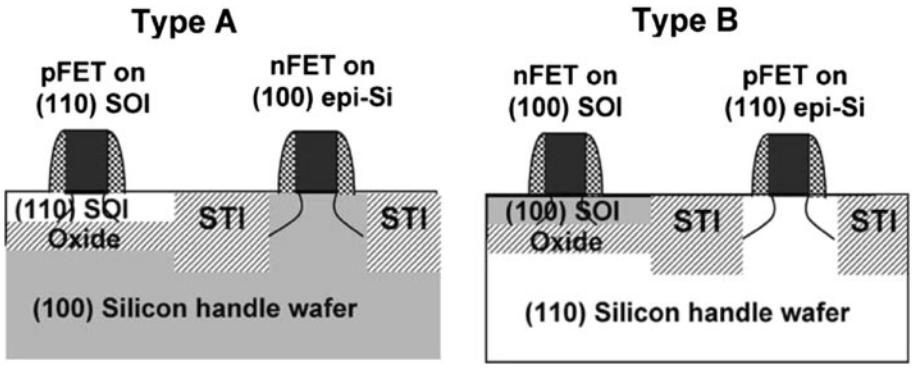

Fig. 15. Schematic cross-section of CMOS on hybrid-orientation substrates, including two types: type A with pFET on (110) SOI and nFET on (100) silicon epitaxial layer and type B with nFET on (100) SOI and pFET on (110) silicon epitaxial layer (Reprinted from Ref. 73 with permission. Copyright 2006, IEEE publisher).

as shown in Fig. 16. A 150-nm-thick oxide is thermally grown on a starting Si(110) substrate for type A or Si(100) substrate for type B. Hydrogen is then implanted through the oxide at a tilt of 7° at room temperature to form a sheet near the interface. Then, the H-implanted wafer is hydrophilically bonded at room temperature to a handle wafer with a different surface orientation. Low-temperature (300°C to 500°C) annealing is performed in N_2 to reinforce the bonding interface before mechanical stripping. The bonding interface is further reinforced by subsequent high-temperature (1100°C) annealing. Finally, the top SOI layer is chemically and mechanically polished and thinned down to the desired thickness.

The crystal orientation of single-crystal silicon layers could be changed in selected areas from one orientation to another by an amorphization/templated recrystallization (ATR) process. Therefore, ATR could serve as an alternative approach to fabricating planar hybrid-orientation substrates with both Si(100) and Si(110) surfaces.[75]

Figure 17 shows the ATR process schematically. The process starts with substrates composed of "direct-silicon-bonded" (DSB) overlayers of Si(110) on Si(100) handle wafers, giving rise to a Si-to-Si interface that is free of interfacial oxide. A DSB substrate could be formed by a "quasi-hydrophobic" bonding method in which ultrathin (1 nm to 2 nm) oxide present on the wafer surfaces during bonding is removed by high-temperature (1320°C to 1325°C) oxide dissolution annealing, leaving the desired direct Si-to-Si contact at the bonding interface.[76] ATR is performed on these selected regions of Si(110) bonded to a Si(100) handle wafer. The Si regions selected for ATR are first separated from those that are not selected for ATR by SiO_2 trenches. The selected regions are then amorphized by ion implantation through openings in a resist mask and recrystallized to form Si(100), whereas nonselected regions remain on Si(110).

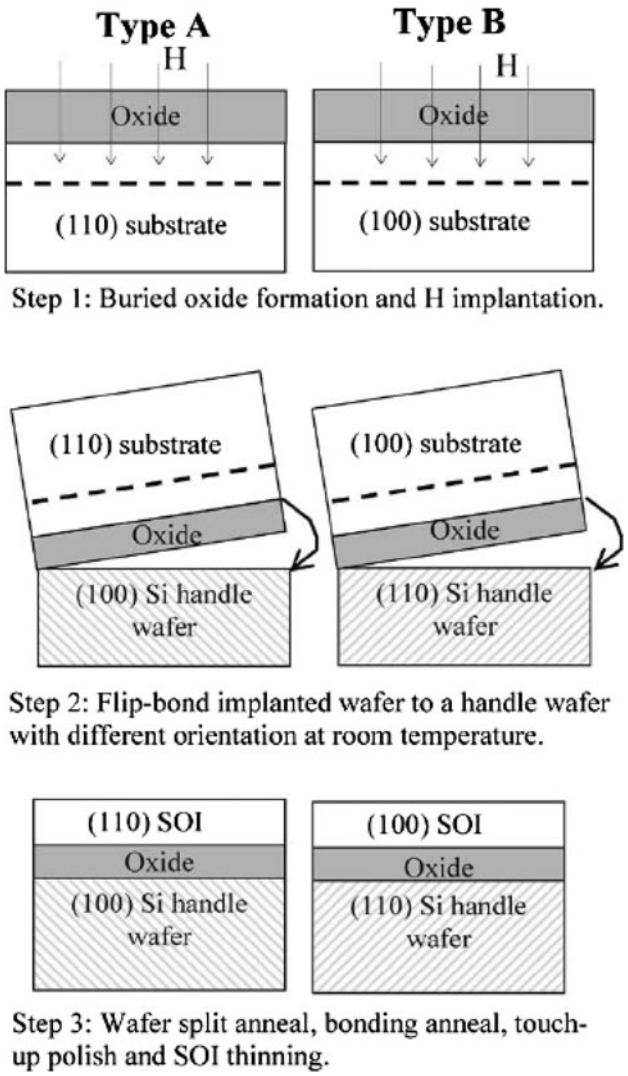

Fig. 16. Process flow of hybrid-orientation substrate fabrication using wafer bonding technology (Reprinted from Ref. 73 with permission. Copyright 2006, IEEE publisher).

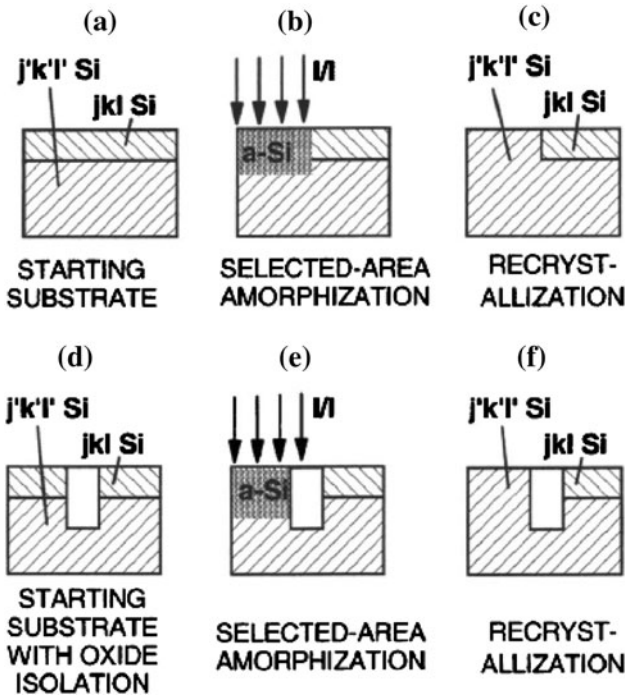

Fig. 17. Schematic of the ATR approach for forming hybrid-orientation substrates in substrates without (a–c) or with (d–f) trench isolation regions (Reprinted from Ref. 75 with permission. Copyright 2005, American Institute of Physics).

Integration of nMOS devices on Si(100) and pMOS devices on Si(100) in the vertical direction is also applicable.[77] The key to this integration strategy relies on low-temperature molecular bonding, in which independent optimization of channel materials and the crystalline orientation of top and bottom FETs is allowed. This method makes full use of a hybrid-orientation substrate and high integration density. The best hole mobility for pMOS devices on Si(110) is obtained by rotating the top wafer by 90° during bonding. The optimization of NiSi silicide, SPE, and *in situ*-doped SiGe stressors is also carried out to achieve low parasitic resistance. Hybrid-orientation technology (HOT) exhibits excellent scalability due to its low thermal budget.

Device Fabrication and Characterization

Figure 18 shows a typical integration process flow of CMOS fabrication using HOT on a hybrid-orientation substrate composed of bulk and SOI.[73,78] Starting with a hybrid-orientation substrate, a thin oxide/SiN stack is deposited. One additional block lithography and reactive ion etching (RIE) step is used to etch through the entire stack, and the surface of the underlying handle wafer is exposed. Following spacer formation, epitaxial silicon is selectively grown in the openings by rapid thermal chemical vapor deposition. Owing to the nature of epitaxy, this epi-Si has the same crystal orientation as the handle wafer. Chemical mechanical polishing (CMP) is performed, and the dielectric layer on top of the SOI is removed, followed by standard CMOS fabrication.

A significant enhancement in the performance of pMOS devices (I_{on} = 730 μA/μm at V_{dd} = 1.0 V and I_{off} = 90 nA/μm) without degrading nMOS performance is achieved. Wafer bonding and the selective silicon epitaxy process introduce process integration and circuit design complexity, which result in a mixture of bulk and SOI devices. The HOT should be carefully optimized for the sake of reducing R_{ext} and defect density, as pMOS devices fabricated by HOT suffer from significant external resistance (R_{ext}).[74]

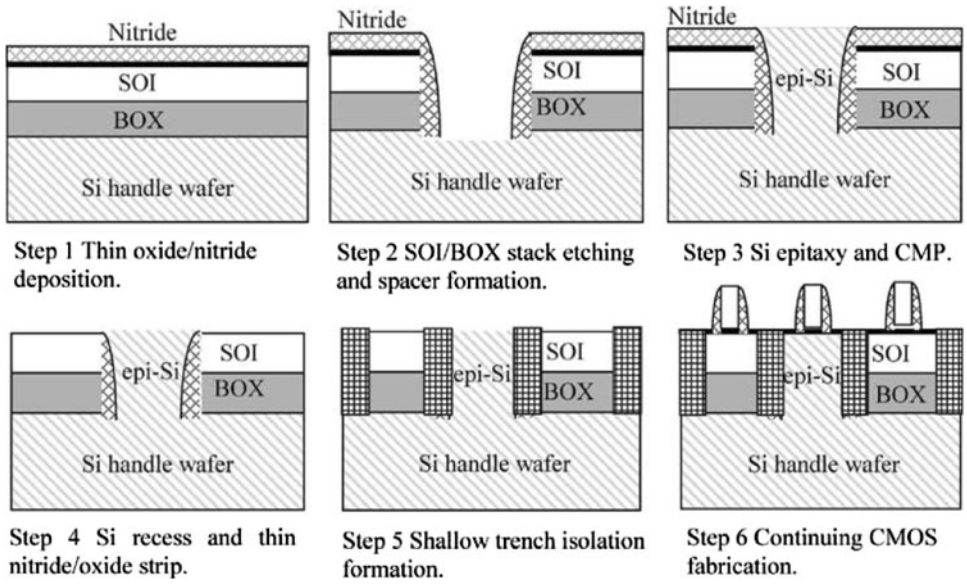

Fig. 18. Integrated process flow for HOT CMOS fabrication on a hybrid-orientation substrate mixed of bulk and SOI, where nMOS is on the (100) surface and pMOS is on the (110) surface (Reprinted from Ref. 79 with permission. Copyright 2005, IEEE publisher).

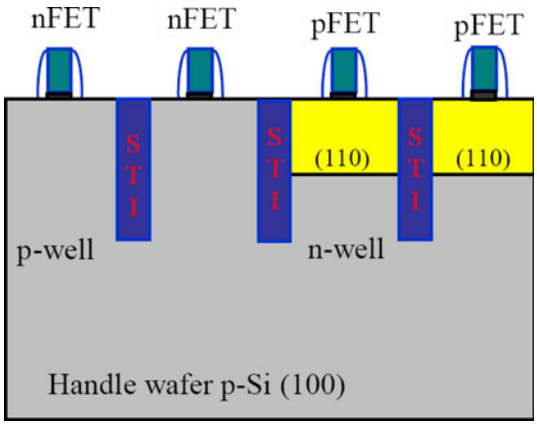

Fig. 19. Schematic of a CMOS structure fabricated on a DSB bulk substrate with SPE (Reprinted from Ref. 79 with permission. Copyright 2005, IEEE publisher).

High-performance 65-nm-technology [L_{poly} = 45 nm, equivalent oxide thickness (EOT) = 1.2 nm] bulk CMOS devices have been demonstrated on mixed-orientation substrates using DSB wafers and a SPE process, as shown in Fig. 19. nMOS devices on SPE-converted Si(100) exhibit the same performance as the controls on Si(100) (I_{on} = 1000 μA/μm at V_{dd} = 1.0 V and I_{off} = 40 nA/μm), as shown in Fig. 20a. pMOS performance is improved by 35% because of the hole mobility enhancement observed on Si(110) compared with Si(100) surfaces, as shown in Fig. 20b.[79] DSB substrates and the SPE process are fully compatible with conventional CMOS processes, and no new material is introduced. Only one extra lithography step is included in this process; this includes amorphization and solid-phase epitaxy, which bring marginal additional cost.

APPLYING NEW HIGH-MOBILITY CHANNELS

A 40% performance enhancement can be achieved in pMOS devices by strain engineering to reach the end of the ITRS roadmap; however, less than 5% enhancement is expected for nMOS devices, indicating that nMOS technology is at its limits. Applying new channel materials, such as SiGe,[80–82] Ge,[83] and group III–V materials[84] (GaAs, InAs, InSb, and InGaAs), will improve the carrier mobility through effective mass modulation and subband structure engineering.[85] The guidelines for modulating effective mass are summarized as follows:[86] (1) heavier m_z for reducing inversion-layer thickness and increasing $C_{inv.}^{thickness}$; (2) lighter m_x for increasing υ_s; (3) optimized D_{2D} in thin t_{ox} for tradeoffs between $C_{inv.}^{DOS}$ and υ_s; and (4) $m_y > m_x$, where m_x, m_y, and m_z represent directional components of effective mass, respectively, and $C_{inv.}^{DOS}$ and $C_{inv.}^{thickness}$ represent inversion-layer capacitance due to finite density-of-states (DOS) and quantum-mechanical thickness of inversion layers, respectively; D_{2D} represents the DOS of the two-dimensional (2D) subband, and υ_s is the carrier velocity near the source edge. In particular, a thinner t_{ox}, shorter L_g, and lighter m_x are better under a given D_{2D}. The selection of appropriate channel materials is based on these considerations.

Table II shows the mobility and effective mass of both electrons and holes, bandgap, DOS, and permittivity of Si, Ge, and main III–V semiconductors.

The electron mobilities of III–V materials are quite high, such that the enhancement factor of electron mobility against Si can amount to 3 to 50 in bulk Si. Such high mobilities could be attributed to the light effective mass of the electrons. However, there are also some fundamental deficiencies in material properties, such as a typically low DOS, small direct bandgap, and high permittivity, as shown in Table II. Many difficult theoretical and technological issues remain unsolved, which prohibits mass production of CMOS devices using these new materials. In the following sections, the current progress and difficulties concerning these issues are reviewed.

SiGe Channel

Due to their high mobility, pMOS devices with compressively strained SiGe channels are promising. However, the small bandgap of Ge-rich materials inevitably leads to an increase in I_{off}, which

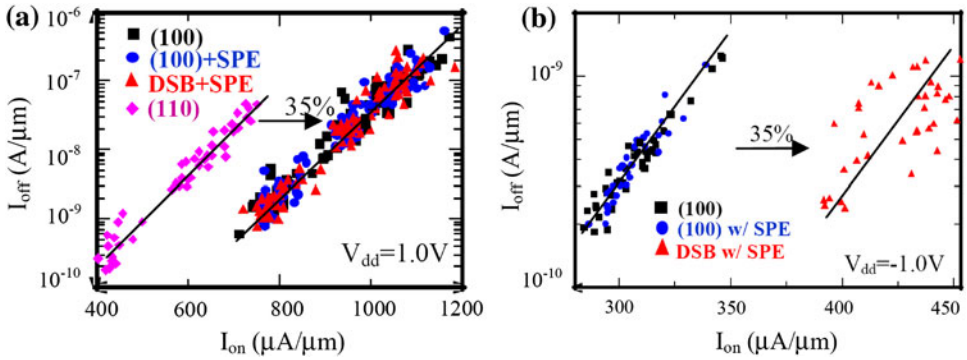

Fig. 20. (a) I_{on} versus I_{off} from nFETs on (100), (100) with SPE, and DSB with SPE, and (110) control; (b) I_{on} versus I_{off} from pFETs on (100), (100) with SPE, and DSB with SPE, L_{poly} = 45 nm, EOT = 1.2 nm (Reprinted from Ref. 79 with permission. Copyright 2005, IEEE publisher).

Table II. Electron and hole mobilities, electron and hole effective mass, bandgap, DOS, and permittivity for Si, Ge, and typical III–V compound semiconductors (Reprinted from Ref. 86 with permission, copyright 2008, IEEE publisher, and from Ref. 165 with permission, copyright 2010, American Institute of Physics)

		Si	Ge	GaAs	InP	InAs	InSb
Electron mobility (cm^2/Vs)		1600	3900	9200	5400	42000	77000
Electron effective mass (m_0)		m_t: 0.19 m_l: 0.916	m_t: 0.082 m_l: 1.467	0.067	0.082	0.023	0.014
Electron DOS (/eV·cm^2)	Valley 1	6.97×10^{14}	5.01×10^{14}	2.76×10^{13}	3.34×10^{13}	9.61×10^{12}	5.85×10^{12}
	Valley 2	1.59×10^{14}					
Hole mobility (cm^2/Vs)		430	1900	400	200	500	850
Hole	Heavy	1.22×10^{14}	5.6×10^{13}	1.95×10^{14}	2.5×10^{14}	6.27×10^{13}	1.79×10^{14}
DOS (/eV·cm^2)	Light	1.05×10^{14}	8.94×10^{12}	3.13×10^{13}	3.71×10^{13}	3.59×10^{12}	6.27×10^{12}
	Split-off	1.21×10^{14}	3.51×10^{13}	7.1×10^{13}	7.09×10^{13}	5.85×10^{13}	7.94×10^{13}
Hole		m_{HH}: 0.49	m_{HH}: 0.28	m_{HH}: 0.45	m_{HH}: 0.45	m_{HH}: 0.57	m_{HH}: 0.44
Effective mass (m_0)		m_{LH}: 0.16	m_{LH}: 0.044	m_{LH}: 0.082	m_{LH}: 0.12	m_{LH}: 0.035	m_{LH}: 0.016
Bandgap (eV)		1.12	0.66	1.42	1.34	0.36	0.17
Permittivity		11.8	16	12	12.6	14.8	17

mainly consists of junction leakage and band-to-band tunneling.[87]

High-performance devices are only fabricated on selective SiGe-on-insulator (SGOI) or Ge-on-insulator (GOI) regions to maintain low I_{off}. A method of epitaxial growth using a SiGe layer with an initially low Ge fraction and a local Ge-condensation technique[87] has been developed to form compressively strained SGOI channels, allowing fabrication of MOSFETs with very high Ge fractions in selected regions on SOI substrates.[82]

The fabrication process is shown in Fig. 21. First, a low-Ge-fraction SiGe layer is grown epitaxially on an SOI substrate by low-pressure chemical vapor deposition. This is followed by conventional local oxidation of silicon (LOCOS) isolation to form a recessed channel underneath. After stripping the LOCOS layer, a second oxidation is performed to grow the gate oxide at 900°C. Using this process, pMOS devices with Ge-rich (up to 96%) strained SiGe layers are fabricated locally in selected areas and exhibit significant enhancements in hole mobility up to 10 times that of control devices.

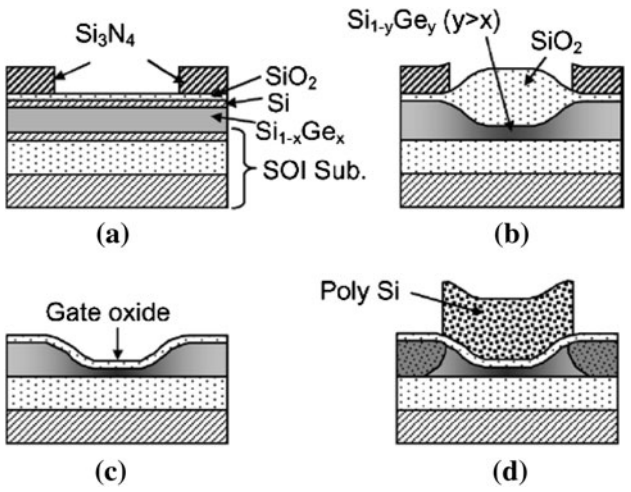

Fig. 21. Fabrication procedure for strained SGOI MOSFETs by a local condensation technique (Reprinted from Ref. 82 with permission. Copyright 2005, IEEE publisher).

The combination of uniaxial compressive stress with SiGe (Ge) channel materials can potentially provide stress greater than 1 GPa. The lateral strain relaxation technique is proposed for this purpose.[88] Preserving the strain along the channel direction while relaxing it along the width direction is the key to this technique. Moreover, the elastic strain relaxation from pattern edges effectively suppresses dislocation nucleation. Therefore, dislocation-free SGOI channels with only longitudinal compressive stress along the channel can be realized.

The fabrication process is compatible with that of standard CMOS technology, except for the compressively strained SGOI substrates formed by the above-mentioned Ge-condensation technique. One minor flaw is the thicker gate oxide compared with that of control devices because of the Ge-induced enhancement of the oxidation rate. In Fig. 22, the fabricated pMOS on uniaxially strained SGOI (Ge content 20%) exhibits a high mobility enhancement of 100% and I_{on} enhancement as high as 80% over control devices. This enhancement effect could be maintained at high vertical field as well as in the short-channel regime.

A Si cap layer is always deposited on the SiGe channel to reduce interface trap density and gate leakage. However, avoiding the Si capping layer is necessary to further scale down the gate oxide due to Ge-enhanced Si oxidation. Therefore, an optimized epitaxial SiGe on Si and high-k dielectric/metal gate process is proposed.[89] The formation of high-quality epitaxial SiGe films with optimized Ge concentration as well as excellent wafer uniformity and $HfSiO_2$ gate dielectrics of improved interface

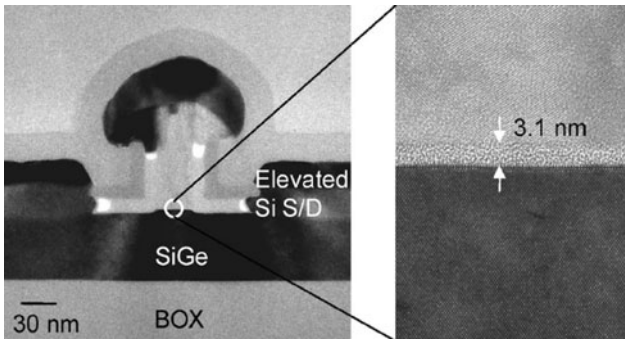

Fig. 22. Cross-sectional TEM images of 30-nm-L_{poly} strained SGOI pMOS (Reprinted from Ref. 88 with permission. Copyright 2006, IEEE publisher).

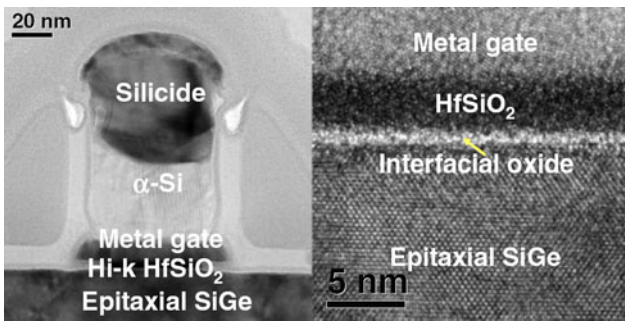

Fig. 23. TEM images of a gate stack with $HfSiO_2$ high-k gate dielectrics and metal gates fabricated on high-quality epitaxial SiGe layers selectively grown on Si(100) substrates (Reprinted from Ref. 89 with permission. Copyright 2008, The Japan Society of Applied Physics).

quality and surface roughness are critical. These can be achieved by optimizing the temperature of the Si substrate and partial pressure of the chemical vapor deposition gases.

Figure 23 shows TEM images of a pMOS architecture with a $HfSiO_2$ gate dielectric/metal gate deposited on an epi-SiGe channel. $HfSiO_2$ remains amorphous with a visible SiO_2 interfacial layer. The resulting gate stack of $HfSiO_2$ on the SiGe channel exhibits minimal C–V hysteresis (<20 mV) and low gate leakage current (3×10^2 times lower than SiO_2/Si channel) at an EOT of 14 Å. High I_{on} is achieved through the effective suppression of off-state leakage. V_{th} roll-off, Subthreshold slope (S_s), and gate-induced drain leakage (GIDL) decrease when Ge% increases due to the variation in the bandgap E_g and dielectric constant of the SiGe channel.

Threshold voltage (V_{th}) variation and strain maintenance are also important concerns for aggressively scaled strained MOSFETs. By adopting millisecond flash annealing, the severe issues of Ge diffusion and strain relaxation during source/drain activation may be solved. pMOS devices with high Ge% (50%) in their SiGe channels demonstrate 2.8× mobility gain with superior NBTI (<30 mV) reliability.[80] V_{th} can be flexibly controlled by Ge% in the SiGe channel and the Si cap effect. High Ge% (50%) as well as preserved strain in the SiGe layer is achieved even at high temperature, resulting in low (−0.2 V to −0.3 V) and tight V_{th} distributions ($\delta V_{th} < 30$ mV) at low EOT (1 nm).

Germanium (Ge) Channel

A Ge channel can be considered as the extreme case of a Si_xGe_{1-x} channel (i.e., when x is 0). However, band-to-band tunneling due to the small bandgap of Ge[90] must be carefully optimized as downscaling is pursued. Although large-diameter Ge wafers are available, one may resort to strained-Si/strained-Ge heterostructure MOSFETs on bulk substrates, which can be fabricated by a bond and etch-back technique.[91] High-mobility carriers in strained-Ge channels are confined in strained-Si/strained-Ge heterostructures with discontinuous valence bands. To deposit Ge layers as smooth, atomically flat, relaxed interfaces, $Si_{1-x}Ge_x$ dislocation blocking layers can be used to fabricate high-mobility Ge-channel pMOSs.[92,93] This process is quite interesting, because it facilitates Si/Ge integration.

With regards to Ge channels for nMOS devices, the small process window is a hindrance to application. Depositing a stable gate stack and improving dopant activation in the source/drain remain challenging.[94,95] Therefore, most work focuses on Ge-channel pMOS devices.

The problems with Ge MOSFETs are low interface quality,[96] high leakage, compromises between high channel mobility and low band-to-band tunneling leakage, and compatibility with the traditional CMOS process. The problems of broadening of the energy band as described by quantum mechanics and understanding the activation and diffusion mechanism of Ge in Si are also urgent. These critical issues could cause researchers to resort to gate dielectric/channel interface optimization, source/drain engineering, new gate stack, and device architecture integration. Among these strategies, the most effective strategy is to engineer the interface.

Slot-plane-antenna (SPA) radical oxidation of Ge could provide high-quality GeO_2/Ge interfaces, as the atomic oxygen radical (O*) is more active than molecular oxygen (O_2). Consequently, it can effectively repair oxide defects. GeO_2 grown by such SPA radical oxidation is amorphous, and the GeO_2/Ge interface is smooth with a low density of interfacial states.[97]

Surface passivation is another effective way to achieve smooth interfaces. A 4-nm-thick defect-free silicon capping layer on an ultrathin strained Ge channel could improve the mobility and reduce the leakage current significantly.[90] The improved interface between Ge and the gate dielectric accounts for the improvement in hole mobility in

Ge-channel pMOS devices with Si capping layers. At low effective field (E_{eff}), the reduction of Coulomb scattering due to the separation of mobile carriers from interface charges by inserting a Si layer, as well as the reduction in the density of Coulomb scattering centers, is believed to contribute to the mobility enhancement. However, at high E_{eff}, the reduction in the surface roughness due to the change in the channel region from SiO_2/Si interfaces to Si/Ge interfaces is responsible for the mobility enhancement.[98]

It is critical to control the thickness of the capping Si layer precisely, because excessively thick Si capping layers cause mobility degradation. This degradation is ascribed to generated dislocations, which result in spatial strain distribution in Si.[98] A small change in the thickness of the Si capping layer will strongly affect electrical parameters such as hole mobility and drive current.[99] The optimal Si thickness is about 0.8 nm, which produces the peak mobility.[100]

The mobility variation can be explained by the charged centers in the gate oxide and strong remote Coulomb scattering due to defects at the Si/SiO_2 interface.[101] The fact that the increase in I_{on} is inversely proportional to the EOT reveals the important scattering mechanisms due to defects located within the gate dielectric.

Although a Si capping layer could be employed on top of relaxed Ge,[102] it results in a buried channel. For Ge-channel devices, a high-k dielectric/metal gate is indispensable, because native Ge oxide is water soluble. Additionally, Ge-channel devices cannot withstand high-temperature annealing due to Ge diffusion.

A low-thermal-budget (≤400°C) process to fabricate Ge MOS devices, in which a high-k gate dielectric (ZrO_2) of 6-Å to 10-Å EOT and platinum gate electrode are used, has been demonstrated.[103] A novel self-isolated process is employed to simplify the fabrication of a ring transistor. The key to this process is the formation of the gate stack and source/drain junction. The high-k dielectric is formed by ultrahigh vacuum (UHV) sputtering of 20-Å to 30-Å Zr films followed by *in situ* UV ozone oxidation at room temperature. The resulting Ge/ZrO_2 interface offers excellent C–V characteristics. The Pt gate electrode is formed by a lift-off process. BF_2 is implanted in a lightly Sb-doped Ge substrate, which is covered by low-pressure chemical vapor deposition (LPCVD) SiO_2. Activation of dopants is performed at 400°C in a N_2 atmosphere. Dopants are sufficiently activated, and a low sheet resistance is attained. The resulting pMOS device shows low field mobility, twice that of Si MOSFETs.

To further scale the EOT, molecular-beam epitaxy/deposition (MBE/MBD) techniques have been exploited for fabrication of Ge pMOS devices with TaN/HfO_2 gate stacks.[96,104] An ultrathin Ge oxynitride layer is deposited as the interfacial layer between HfO_2 and Si. The resulting EOT is 0.7 nm thick after quantum-mechanical correction, and the gate leakage is extremely low,[96] which indicates that MBD offers advantages over conventional processes. The hole mobility is enhanced by a factor of 2, as compared with TaN/HfO_2/Si control devices without interfacial Ge oxynitride layers.

Plasma-PH_3 and thin AlN between a high-k film and Ge substrate as surface passivation layers are efficient in suppressing the formation of GeO and preventing Ge outdiffusion, resulting in improved interfaces in nMOS devices with extremely low leakage. Enhancements in hole (1.6×) and electron mobility (1.8×) are obtained under optimized postannealing conditions.[83]

It is necessary to avoid the formation of GeO_2 at high-k/Ge interfaces to achieve thin EOT. Therefore, an approach to form a Sr germanide layer as an insulating interlayer for the high-k/Ge gate stack has been proposed to avoid the formation of a Ge oxide interlayer. The corresponding high-k/Ge pMOS with low gate leakage designed for ultrathin EOT (1 nm) and high hole mobility (481 cm^2/Vs) has been fabricated.[105] The standard high-k/gate-last process is applied with a slight modification to the Sr deposition process, and an MBE apparatus is used to provide an oxide-free Ge surface. A thermally stable amorphous $SrGe_x$ interlayer exists at the high-k/Ge interface without diffusing into the high-k film after annealing at 400°C, which provides fair interfacial properties and EOT scalability.

Another gate dielectric that could be used is Ge oxynitride (GeON) and a low-temperature oxide (LTO) stack, where GeON is formed by nitridation of a thermally grown Ge oxide.[106,107] A smooth interface between Ge and Ge oxynitride is produced, and no interface between GeON and LTO is observed, as shown in Fig. 24. The drive current and transconductance of the fabricated pMOS devices are high compared with Si control devices. Excellent

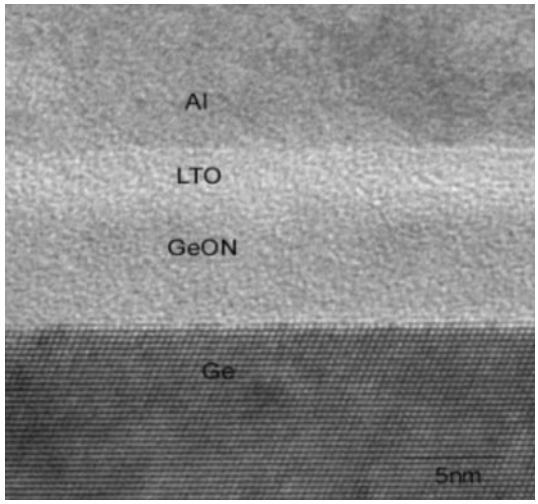

Fig. 24. TEM image of Al/LTO/GeON/Ge stack. A smooth interface between Ge/GeON is achieved using this GeON process (Reprinted from Ref. 106 with permission. Copyright 2003, IEEE publisher).

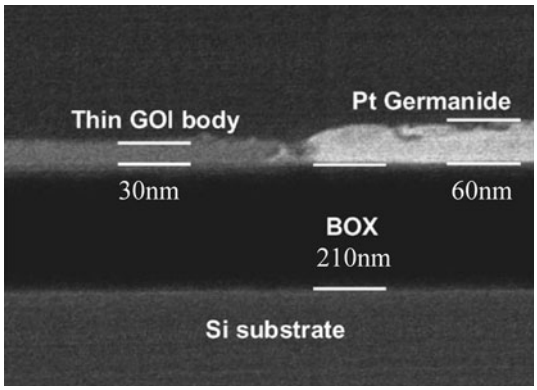

Fig. 25. X-ray secondary emission microscopy (XSEM) image of thin-body GOI Schottky-barrier MOSFET with Pt germanide source/drain (Reprinted from Ref. 108 with permission. Copyright 2005, IEEE publisher).

subthreshold characteristics with 82 mV/dec are attributed to low interface trap density as well as low leakage junction.

To solve the problems of high resistance and deep junctions due to low dopant solubility in Ge and fast dopant diffusion, Schottky barrier source/drain Ge transistors with intrinsic low thermal annealing temperature are considered an alternative solution. Excellent performance of pMOS devices with thin GOI channels using Pt germanide Schottky barrier source/drain with low barrier height has been demonstrated.[108] The buried oxide and Si substrate are used as a gate dielectric and a bottom gate electrode, respectively, as shown in Fig. 25. The reaction of Pt with Ge leads to the formation of Pt germanide, which exhibits an extremely low Schottky barrier height, reducing the parasitic source/drain resistance greatly. GOI substrates are prepared by using Ge-condensation technology,[87] followed by conventional Schottky Barrier MOSFET processing. A high hole mobility with an enhancement of 40% to 50% against the universal hole mobility of Si MOSFETs is obtained for the accumulated GOI channel.

Fabricating Ge pMOS devices on ultrathin layers of insulator is advantageous in terms of increasing the bandgap and better V_{th} control. A method of localized GeOI on Si substrates with Ge-condensation based on silicon-on-nothing (SON) technology has been developed.[109] The process is presented in Fig. 26. Nonuniform ultrathin Ge (8 nm) on buried dielectrics in source/drain areas makes it impossible to obtain Ge raised source/drain and germanidation, thus causing high access resistance, which is responsible for drive current degradation. A new process that uses direct Ge epitaxy, as shown in Fig. 27, has been proposed to overcome this issue.[110] Ultrathin pure Ge capped with thin Si epitaxial layers is directly integrated just under the gate of localized-SOI devices that benefit from high-mobility channels without the associated penalty of degraded parasitic resistance. Junctions in Si areas are activated by SPE with Ge amorphization of Si junctions. Boron atoms are implanted for the formation of extensions. Crystallization annealing is performed at 600°C to activate the dopants. Ge is only localized below the gate stack. NiSi silicidation is performed after the SPE process. The latter approach seems to be compatible with the low parasitic resistance requirement for performance improvement. Functional localized-GeOI pMOS transistors scaled down to 75-nm gate lengths with drive currents up to 600 μA/μm at −1.1 V have been demonstrated.

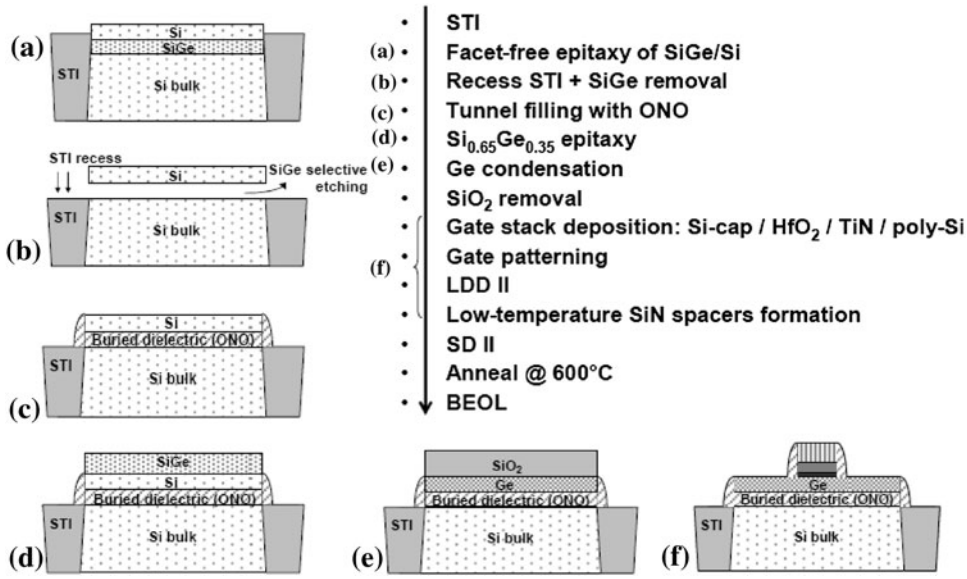

Fig. 26. Process flow description: localized-GeOI technology is based on SON technology. LDD II: Lightly-doped-drain ion implementation, BEOL: back end of the line, ONO: $SiO_2/Si_3N_4/SiO_2$, SD II: source/drain ion implementation (Reprinted from Ref. 110 with permission. Copyright 2008, IEEE publisher).

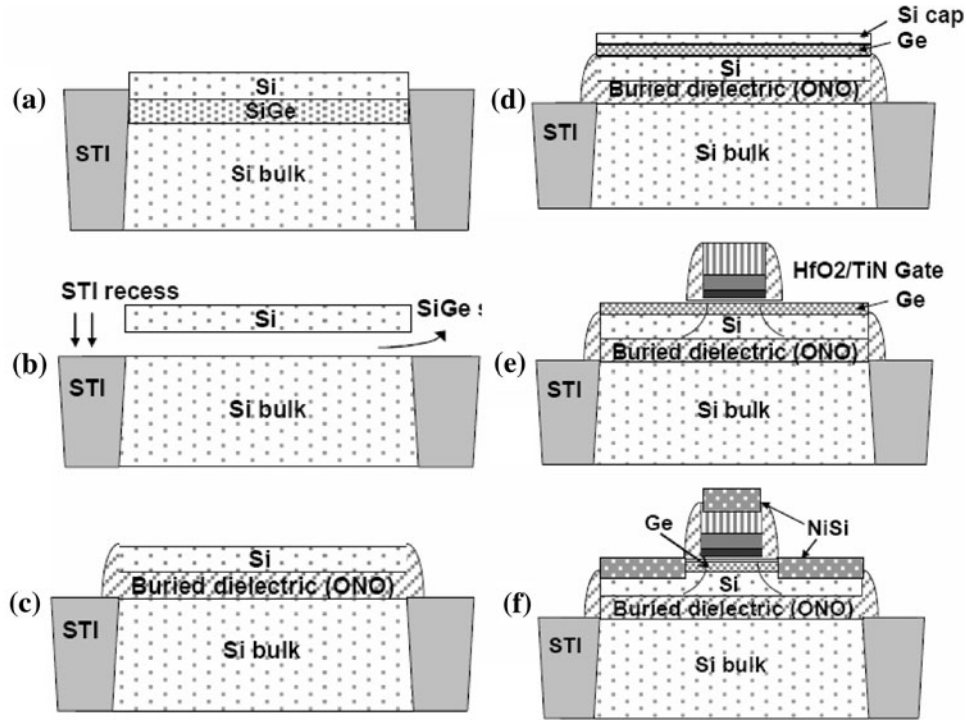

Fig. 27. Process flow description of the localized ultrathin GeOI technology with pure Ge epitaxy (Reprinted from Ref. 110 with permission. Copyright 2008, IEEE publisher).

Fabrication of Ge nMOS devices is challenging for the reasons outlined above. The intrinsically low density of states in conventional (100) channel directions and the high conductivity effective masses of electrons that populate L valleys are believed to be the major causes of the low electron mobility and carrier concentration, resulting in the relatively low on-state current of Ge nMOS devices.[111] The first conventional, self-aligned Ge nMOS device with fully activated phosphorus-doped Ge source/drain junctions was demonstrated in Ref. 112. The fabrication process is a standard planar bulk process with improved low-temperature junction annealing performed to minimize junction leakage. GeON and a LTO stack with a total equivalent oxide thickness of 8 nm and a W gate electrode are used as the gate stack. Device characteristics are less than satisfactory, with a subthreshold slope of 150 mV/dec and an on–off current ratio of only 10^4.

Breakthroughs in Ge nMOS fabrication have been recently reported. Fast traps due to the charge neutrality levels (i.e., interface donor and acceptor states close to the valence band)[113–115] make contributions to the reduction of nMOS inversion mobility. The related density of interface states could be significantly reduced by improving GeO_2 quality by ozone oxidation.[116] Low-temperature dopant activation is also required to suppress Ge suboxides. Slow traps in the bulk and borders of high-k dielectric due to the low conduction-band offset of GeO_2 and large source/drain series resistance due to the insufficient activation of n-type dopants are considered the major causes of nMOS performance degradation. The highest electron mobility for Ge nMOS devices (1.5× universal Si mobility) has been determined by Hall measurements, which excludes the effects of source/drain series resistance and trapping states.[117]

Another experiment also reports a high electron mobility greater than 1000 cm^2/Vs by careful thermodynamic and kinetic control of the Ge/GeO_2 interface on Ge(111).[118] High-pressure oxidation (HPO) and post-low-temperature oxygen annealing (LOA) processes have been developed to suppress GeO desorption and reduce the density of interfacial states, respectively. The physical nature is well explained through the kinetic and thermodynamic control of the GeO_2/Ge system.[119] This interface-conscious nMOS fabrication is implemented by gate-last processing at a relatively high phosphorus activation temperature (580°C). Further progress should focus on eliminating scattering by charged interface states and surface roughness.

In addition to interface engineering, source/drain junctions are also critical issues for Ge nMOS devices, because the implanted As and P have low solubilities and large diffusion constants. For fair interface quality, the activation temperature should be as low as possible, which makes it difficult to form a source/drain that simultaneously has low resistance and small junction leakage. Metalorganic vapor-phase epitaxy (MOVPE)-based gas-phase doping (GPD) has been explored to yield superior n^+/p junctions in Ge by reducing damage and crystal

defects.[120] Both the As diffusion constant and junction leakage are significantly reduced. Benefiting from the GPD and low interface states, the fabricated nMOS device exhibited electron mobility as high as 840 cm^2/Vs.

Obtaining highly active sources/drains through low-temperature annealing for the integration of high-performance Ge CMOS devices is challenging. Metal (Co)-induced dopant activation (Co MIDA) and Ge crystallization are used to achieve very low series resistance (2.23×10^{-4} Ω cm) and shallow (92 nm) source/drain junctions with a high degree of dopant activation fabricated at low temperatures (below 380°C).[121] Figure 28 shows Ge nMOS and pMOS devices with a $GeO_2/Al_2O_3/Al$ gate stack and a novel source/drain formed by Co MIDA; these were fabricated on epi-Ge (at 360°C) and bulk Ge (at 380°C), respectively. The fabricated Co MIDA n^+/P junction diode has an on/off ratio of 10^4, and the resulting Ge nMOS and pMOS devices provide a reasonable I_{on}/I_{off} ratio (10^3) and a high I_{on} per width (1.4 $\mu A/\mu m$ for nMOS and 1.17 $\mu A/\mu m$ for pMOS at L_g = 100 μm).

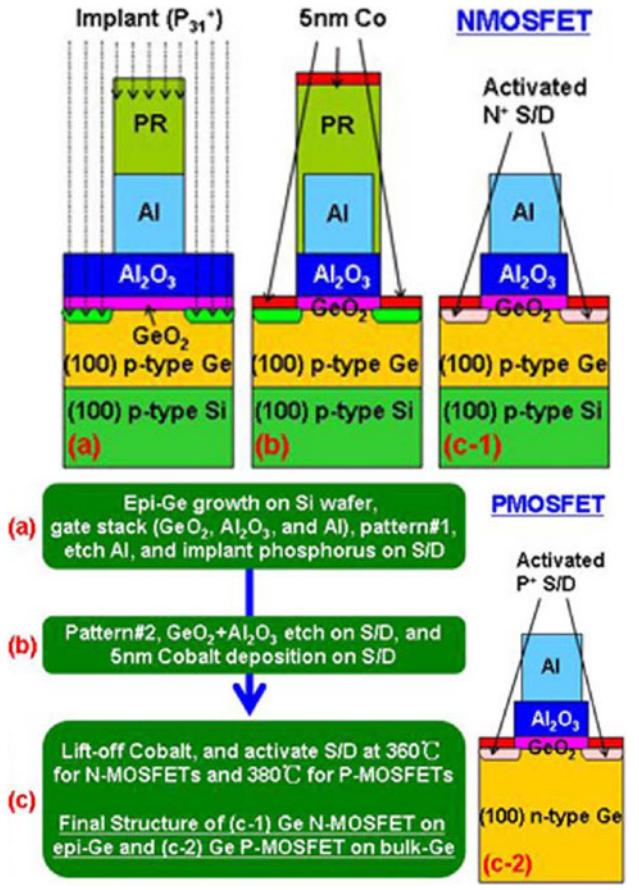

Fig. 28. Ge nMOS and pMOS process flow at sub 380°C. (a, b) The same process steps are applied for both nMOS and pMOS, but (c) different activation temperatures for source/drain are used (360°C for nMOS and 380°C for pMOS in RTA) (Reprinted from Ref. 121 with permission. Copyright 2008, IEEE publisher).

Ultrashallow junctions with highly reduced contact resistance could also be achieved by the combination of high-concentration Sb δ-doping techniques with the formation of atomically controlled metal/Ge.[122] MBE Sb doping followed by homoepitaxial growth of Ge not only avoids ion implantation and thermal activation annealing, but also provides precisely controlled shallow doping depth. An atomically controlled interface between metal/Ge could alleviate Fermi-level pinning in metal/Ge contacts.[123,124] Ohmic conductance of Fe_3Si/Ge Schottky junctions is obtained with Sb concentrations as high as 10^{20} cm^{-3} for Ge(111). Doped epi-Si passivation layers for n-Ge contacts could even eliminate Fermi-level pinning effects by incorporating an NiGe snow-plow to achieve contact resistivity as low as 2×10^{-6} Ω cm.[125]

Uniaxial stress is believed to be indispensable for the performance enhancement of Ge nMOS to satisfy the high-performance specifications of the ITRS-defined 22-nm technology node.[97] For Ge CMOS integration, a combination of a SOI nMOS device with tensile strain and a GOI pMOS device with compressive strain on the same wafer is proposed,[83,126] combining multiple selective growth with the local Ge-condensation technique, as shown in Fig. 29. Strained-Si layers as n-channels are selectively grown on p-well regions of the relaxed SGOI substrates that are formed during the first condensation process. Strained-SGOI layers with Ge content of 66% are formed as p-channels on the n-well regions after the second condensation process, resulting in compressive strain of 1.3%. Conventional SiO_2/poly-Si is used as the gate stack. The

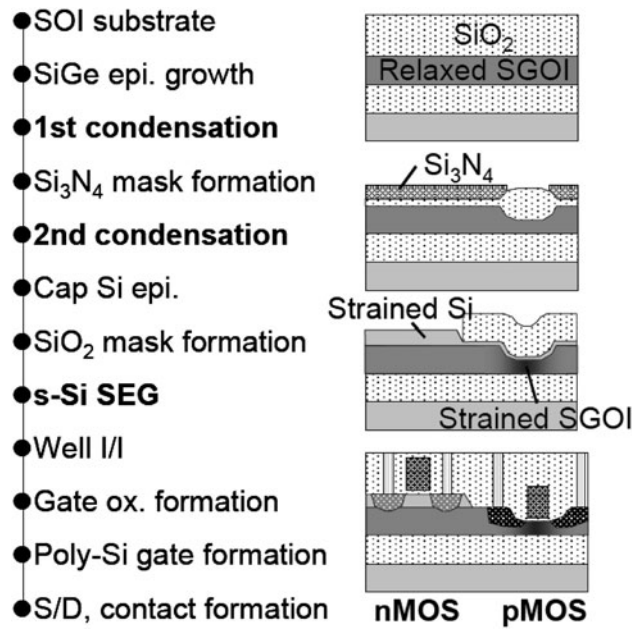

Fig. 29. Schematics of fabrication procedures and device structures of dual Ge CMOS integration (Reprinted from Ref. 126 with permission. Copyright 2005, IEEE publisher).

fabricated CMOS devices show over fourfold higher hole mobility enhancement in the GOI pMOS structure and a comparable current drive to that of the strained-Si nMOS structure.

There is a debate over whether GeOI by Ge condensation is an appropriate substrate for integration,[127] as GeOI pMOS suffers from, among other things, parasitic leakage at the back Ge/buried oxide (BOX) interface, which degrades the I_{on}/I_{off} ratio.[128] Schottky–Read–Hall and trap-assisted tunneling contribute to this leakage at high temperature, whereas dominant band-to-band tunneling produces strong accumulation.[129] Although the leakage could be reduced by silicon passivation at the Ge/BOX interface, the mobility decreases as the thickness of the silicon capping layer increases.[130] Moreover, the thick layer fabricated by Ge-condensation technology may only be suitable for advanced device structures such as FinFETs for fully depleted applications.

Group III–V Material Channels

Group III–V materials, which include GaAs, InGaAs, and InAs, could be a source for channel materials with high carrier mobilities, as shown in Table II; these materials are considered strong contenders to replace Si in strained-Si channels for logic applications beyond the 22-nm node.[59,131,132] However, applying new substrate materials causes tremendous difficulties due to the deviation from the well-rounded Si process platform. The most urgent challenge is the lack of high-quality and thermodynamically stable gate dielectrics. Other intractable problems are the formation of low-resistance CMOS-compatible ohmic contacts and the achievement of high dopant activation, as the gold-based contact technologies that are commonly used for compound semiconductors cannot be employed for CMOS device integration.

The most critical challenge for III–V MOSFETs is the realization of high-quality metal–insulator–semiconductor (MIS) interfaces. The introduction of high-k materials or back-gate modes could greatly improve the interface quality.[131–135] The requirements for high-k gate stacks are scalability, low leakage, thermal stability, and passivation of surface traps.[135]

α-Si passivation could provide excellent interfaces between Al_2O_3 gate dielectrics and $In_{0.7}Ga_{0.3}As$ channels by reducing the interface state density for high-performance $In_{0.7}Ga_{0.3}As$-channel MOSFETs.[136] Removing native oxides and surface As pileup on $In_{0.53}Ga_{0.47}As$ is critical for surface self-cleaning by atomic layer deposition HfO_2.[137] *In situ* plasma PH_3 surface passivation benefits the fabrication of InGaAs MOS devices with HfO_2/TaN and HfAlO/TaN gate stacks.[131] The process flow and a device schematic are shown in Fig. 30. MBE is used to grow 200-nm phosphorus-doped 1×10^{18} cm^{-3} InP buffer and 500-nm phosphorus-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$, where Zn is used as the p-type dopant. After a 10% HCl pre-gate cleaning and $(NH_4)_2S$ treatment, plasma PH_3 passivation at 430°C for 60 s is performed, followed by HfO_2/HfAlO/TaN deposition, which is patterned as a gate stack. The source/drain is implanted with silicon, and Au or Pd contacts are deposited as source/drain front contacts. The results show that plasma PH_3 passivation effectively improves interface quality, minimizes leakage, and increases electron mobility (1600 cm^2/Vs), thus resulting in significantly reduced Ss (96 mV/dec at room temperature) and increased I_{on} (401 mA/mm at V_g and V_d of 3 V) of the fabricated InGaAs nMOS.

A surface-channel GaAs nMOS process has been developed;[132] it incorporates several advanced process modules such as an *in situ* surface passivation scheme for the formation of the TaN/HfAlO/GaAs gate stack with high interface quality, silicon and phosphorus co-implanted source/drain for high dopant activation, and CMOS-compatible PdGe source/drain ohmic contacts that alleviate gold-contact contamination problems. An oxidized Si interfacial layer (1 nm) is formed between HfAlO

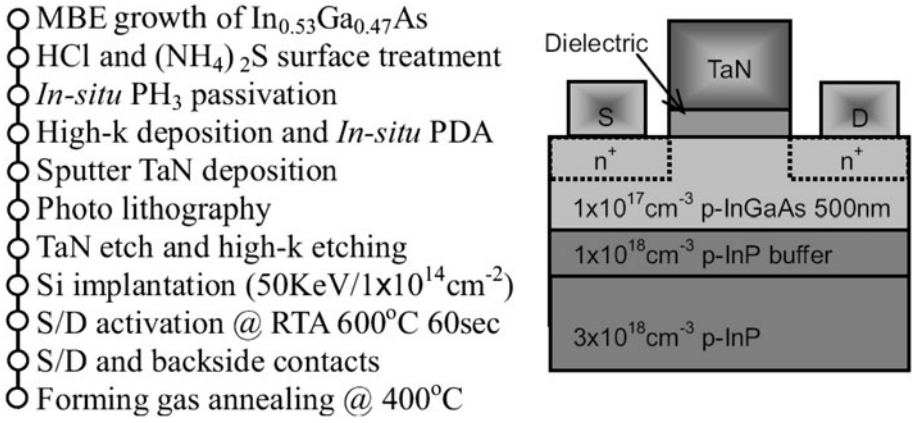

Fig. 30. Process flow and device schematic of self-aligned gate-first InGaAs channel MOSFET (Reprinted from Ref. 131 with permission. Copyright 2008, IEEE publisher).

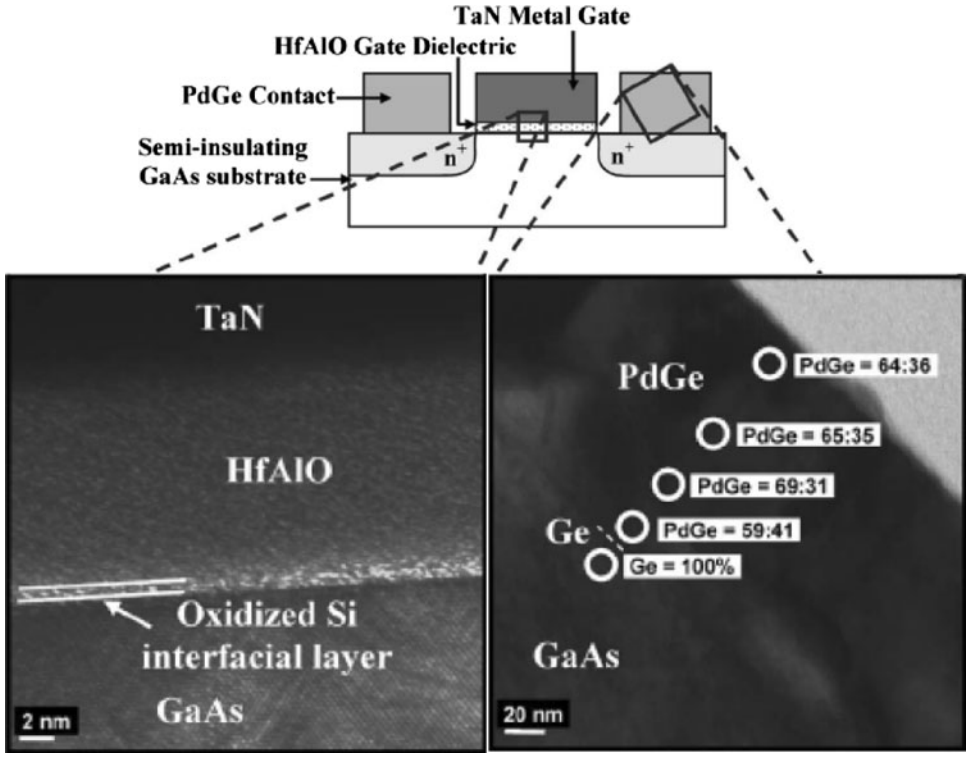

Fig. 31. Schematic and TEM images showing TaN/HfAlO gate stack formed with an *in situ* surface passivation process as well as a PdGe ohmic contact technology (Reprinted from Ref. 132 with permission. Copyright 2008, IEEE publisher).

dielectric and GaAs during the *in situ* surface passivation process, as shown in Fig. 31. Good device characteristics are obtained with a high drain current on/off ratio of 10^5 and a high peak electron mobility of 1230 cm^2/Vs.

Parasitic resistance constitutes a large problem for III–V channel MOSFETs. This problem becomes severe if devices are fabricated by non-self-aligned methods, which could result in large parasitic resistance due to the separation between gate and source/drain.[138] The first III–V *n*-MOSFETs with self-aligned contact technology to be demonstrated were GaAs MOSFETs.[139] A SiGe epitaxy layer is formed in GaAs source/drain, and Ni is deposited to form NiGeSi ohmic contacts. Heavily doped n^+ source/drain is achieved by Ge and Si diffusion into GaAs. The contact resistivity of NiGeSi on Si piled up *n*-GaAs is determined to be as low as 5.7×10^{-4} Ω/cm^2. Self-aligned gate technology has also been developed for InGaAs high-electron-mobility transistors. The process combines lift-off and double-exposure e-beam lithography. The novel structure leads to very low parasitic gate capacitance. The nonalloyed Mo-based ohmic contacts result in very low contact resistance (7 Ω μm).[140]

Recently, performance breakthroughs in reducing contact resistance have been made by carefully considering the surface conditions before metal deposition. *In situ* ohmic contacts between Mo/InGaAs without vacuum break are obtained, achieving contact resistivity as low as $(1.1 \pm 0.6) \times 10^{-8}$ Ω/cm^2.[141] By carefully treating the surface with UV-ozone/HCl and atomic H, *ex situ* ohmic contacts with $(1.1 \pm 0.6) \times 10^{-8}$ Ω/cm^2 have also been achieved.[142]

The solid solubilities of dopant impurities in III–V semiconductors are always low; thus, we could resort to metal source/drain structures. Self-aligned metal source/drain InGaAs MOSFETs could be achieved by using Ni-InGaAs alloy.[143] The low Schottky barrier height for *n*-InGaAs could be modulated by the In content, with a sheet resistance of Ni-InGaAs alloy as low as 25 $\Omega/\square$. This low resistance is only one-third of that obtained by doping donor impurities into InGaAs up to the solid solubility limit (80 $\Omega/\square$). Another significant advantage of this process is its extremely low annealing temperature, which can be as low as 250°C.

Introducing new device architectures in III–V MOSFETs could suppress short-channel effects and provide additional performance enhancement. There are many problems associated with the formation of high-quality III-V group materials on insulator (III-V-O-I) layers: (1) further suppression of the generation of dislocations, point defects, and antiphase domains; (2) III-V-O-I thickness control under ultrathin regime; and (3) control over surface flatness and edge shapes of III-V-O-I films. Direct wafer bonding (DWB) technology is considered to be a promising method to prepare high-quality III–V films on insulators.[144]

Ultrathin-body InGaAs-on-insulator nMOS devices fabricated by DWB on a Si substrate with

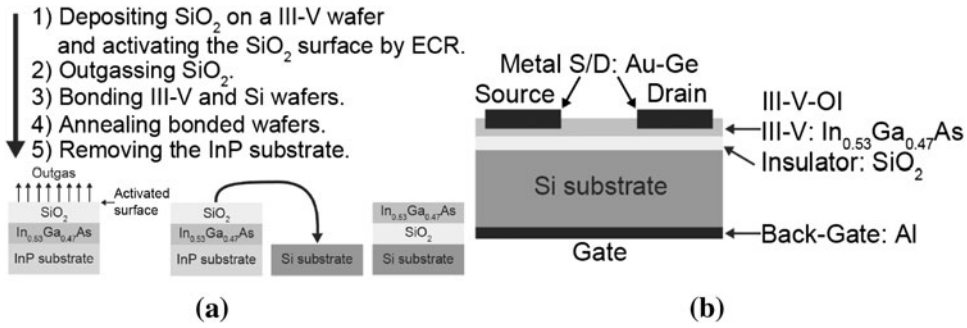

Fig. 32. Process (a) and schematic illustration (b) of metal source/drain III-V-O-I MOSFET on Si with back gate, fabricating on III–V-on-insulator substrate using DWB. ECR: electron cyclotron resonance (Reprinted from Ref. 134 with permission. Copyright 2009, IEEE publisher).

metal source/drain have been demonstrated.[134] Figure 32 shows the process flow with emphasis on plasma-assisted DWB. The III-V-O-I interface where the actual channel exits is away from serious damage during the bonding process, therefore producing a fair interface between the gate dielectric and channel. Excellent characteristics with high electron mobilities of 1000 cm^2/Vs are achieved due to the enhancement factor of 1.59 in the electron mobility as compared with control Si nMOS devices.

Introducing strain technologies could further enhance carrier mobility in III–V MOSFETs. *In situ*-doped lattice-mismatched source/drain stressors for III–V nMOSs are used to induce lateral tensile by $In_{0.4}Ga_{0.6}As$ source/drain in the $In_{0.53}Ga_{0.47}As$ channel, as well as for series resistance reduction.[145] Be is used as a *p*-type acceptor impurity. The key process includes $SiH_4 + NH_3$ passivation of the interface between $In_{0.4}Ga_{0.6}As$ and HfAlO, $In_{0.4}Ga_{0.6}As$ source/drain recess etching, and selective epitaxy of *in situ*-doped $In_{0.4}Ga_{0.6}As$ process. Significant I_{on} enhancement in InGaAs nMOSs is obtained.

There is a significant challenge in identifying high-mobility III–V pFET candidates, as there are less promising materials for hole transport due to intrinsic disadvantages such as low hole mobility compared with strained Si.[146] Most researchers are looking into antimonides as possible *p*-channel materials for pMOS devices. The III-Sb materials are garnering attention for application in deeply scaled devices due to their lower in-plane hole effective mass in strained heterostructures, simplicity of band engineering,[147] reduced leakage, and improved ohmic contacts. Strain technologies, as performance enhancers for III–V channels in pMOS devices, are necessary.[16] Based on band edge and lattice constant considerations, InSb, InGaSb, and GaSb grown on GaAs substrate using solid-source MBE could achieve large biaxial compressive stress. The AlGaSb buffer layer accommodates lattice mismatch, thus minimizing dislocations/defects near the channel layer. High hole mobilities are obtained (1230 cm^2/Vs, 960 cm^2/Vs, and 860 cm^2/Vs for InSb,[148] InGaSb,[149] and GaSb,[150] respectively) due to strain and confinement effects by a large valence-band offset.

pMOS devices show even greater improvements through uniaxial compressive stress, similar to Si devices, and these improvements are particularly prominent in InSb/GaSb devices due to their lower elasticity constant.[151] Biaxial compressive strain could also be explored for hole mobility enhancement. By combining atomic layer deposition Al_2O_3 with low defects in $In_xGa_{1-x}Sb$ pMOS, device performance would even exceed that of its Ge counterpart.[152] At the same time, nMOS devices do not benefit from uniaxial stress but show enhancements via biaxial tensile stress using the representative prototypical GaAs MOSFETs. Hence, strain-enhanced III–V pMOS devices and high-mobility III–V nMOS devices show promise for incorporation as CMOS channels at the sub-22-nm technology node.[153]

Heterogeneous integration of III–V or Ge materials on Si substrates is attractive because of its compatibility with mainstream Si CMOS platforms without the need for developing large-diameter III–V (Ge) substrates. Among such devices, the InGaAs quantum-well field-effect transistor on a Si substrate[154] is one of the most promising candidates for high-speed and low-power digital logic applications due to its high electron mobility, large Γ-to-L valley separation, and good short-channel performance. As shown in Fig. 33, a thin composite metamorphic buffer architecture consisting of GaAs and graded $In_xAl_{1-x}As$ layers by MBE is applied to fabricate the $In_{0.7}Ga_{0.3}As$ quantum well (QW) structure on Si. A 2-nm InP upper barrier layer and a 4-nm $TaSiO_x$ high-*k* gate dielectric form a composite $TaSiO_x$-InP gate stack. The L_g = 75 nm *n*-type $In_{0.7}Ga_{0.3}As$ QWFET on Si with this composite high-*k* gate stack achieves a high transconductance of 1750 $\mu S/\mu m$ and high drive current of 0.49 $mA/\mu m$ at V_{ds} = 0.5 V, as shown in Fig. 34.[155]

There is a significant problem with DWB technology for fabricating III–V materials (i.e., InP) on Si substrates, because III–V wafers with large diameters and smooth surfaces are unattainable.[156] MBE could also be applied for fabricating III–V

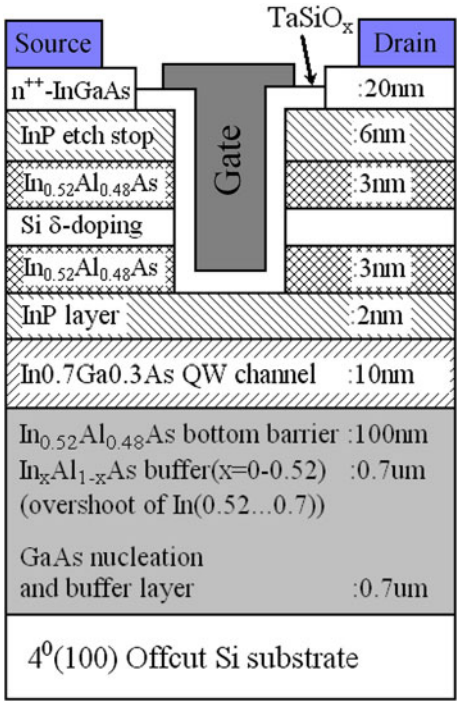

Fig. 33. Schematic of $In_{0.7}Ga_{0.3}As$ QWFET on silicon with composite 4-nm $TaSiO_x$-2 nm InP composite gate stack (t_{OXE} = 22 Å) (Reprinted from Ref. 155 with permission. Copyright 2009, IEEE publisher).

heterointegrated on a Si substrate, but the areal defect density and surface roughness require continuous improvement.[157] It is challenging to obtain good quality (low defectivity) III–V heteroepitaxial layers on large-diameter Si wafers to ensure manufacturability and volume production on large-area wafers, and thick buffer layers are required to minimize defects.

"Aspect ratio trapping" (ART) technology provides a solution to integrate III–V materials or Ge with silicon CMOS.[158] In ART, dislocations are eliminated by trapping them at the bottom of deep, narrow trenches using standard bulk STI technology, producing a low-dislocation region at the top of the trench. In this way, low-defectivity thin heteroepitaxial layers of Ge,[159–161] InP,[162] and GaAs[163] or InGaAs[164] may be obtained, which allows integration of high-mobility channel devices directly on Si.

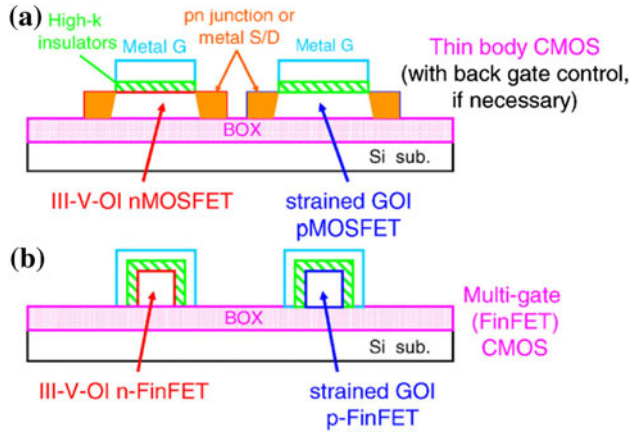

Fig. 35. Ultimate CMOS structure composed of the combination of III–V semiconductor *n*-channel MOSFETs and Ge *p*-channel MOSFETs: (a) ultrathin-body CMOS, and (b) CMOS (Reprinted from Ref. 84 with permission. Copyright 2006, Elsevier publisher).

As shown in Table I, channels using III–V materials with high bulk electron mobility are beneficial for the realization of higher electron mobility and high current in nMOS devices. Ge has the highest hole mobility among Si and III–V materials. Therefore, the best CMOS structure in terms of drive current should be a combination of a III–V semiconductor nMOS and Ge pMOS. A drawback of III–V channels, which usually have larger permittivity than Si and Ge, is the deteriorated short-channel effects; thus, optimization of device structures might be needed. SOI structures on Si substrates can minimize the influence of impurities from the Si standard processing and apparatus, allowing for the combination with a Si platform.

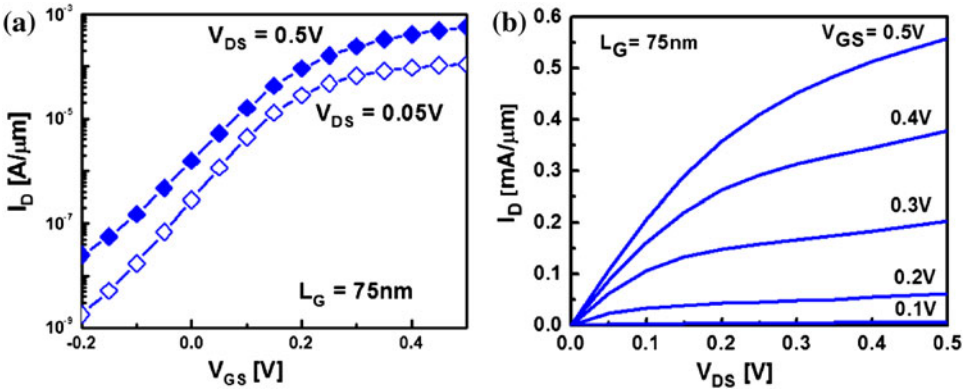

Fig. 34. Transfer (a) and output (b) characteristic profiles of L_g = 75 nm $In_{0.7}Ga_{0.3}As$ QWFET with composite 4-nm $TaSiO_x$/2-nm InP gate stack (t_{OX} = 22 Å) (Reprinted from Ref. 155 with permission. Copyright 2009, IEEE publisher).

For the overall consideration of compatibility and short-channel immunity, the ultimate CMOS structure may resort to an ultrathin body or multi-gate device on an insulator with a combination of a III–V semiconductor nMOS and Ge pMOS,[84] as shown in Fig. 35.

CONCLUSIONS

Mobility enhancement technologies are facing enormous challenges when scaling down MOSFET dimensions. As device dimensions shrink, the performance improvement resulting from SiC and SiGe source/drain stressors and capping stress memorized films is rapidly reduced. The strain may be released in the form of dislocations at high temperature and may thus form new interface states. These interface states will, in turn, limit the processing window of the thermal budget. The increased effective electric field and quantum confinement effects in MOSFETs with shrunken dimension offset the strain effects and lower hole mobility. Consequently, co-optimizing the performance of nMOS and pMOS devices becomes difficult. Interface engineering is the most critical concern for Ge or III–V channel materials. Many issues, such as parasitic effects, must be carefully addressed for future implementation of new channel materials.

Due to the deficiencies of individual mobility enhancement technologies in improving device performance, the combination of different technologies will be required to further improve device performance with the promise of processing compatibility. Combination of CESLs with SiGe stressors as well as with other technologies that offer strain of different polarities has been carried out. The combination of other mobility enhancement technologies may also work, although the feasibility of these combinations must be explored. Properly characterized and implemented strain engineering does not compromise or render long-term reliability. CESL strain and SiC stressors with low concentrations of defects are suitable for nMOS devices, and SiGe stressors are suitable for pMOS devices in terms of reliability issues. New processes with new substrates either based on hybrid orientation or composed of group III–V materials need to be simplified.

The improved mobility offered by mobility enhancement technologies continues to make these technologies a promising and active area when the device dimension is scaled down to 21 nm and beyond. Further efforts to understand the fundamental issues associated with the enhancement of device performance, such as defect evolution and definitive metrology, optimization of various strain techniques in shrunken geometries, and reducing the costs of new channel materials, are required before the ultimate potential of strain engineering is applied in the state-of-the-art transistor.

ACKNOWLEDGEMENT

This project was supported by the State Key Development Program for Basic Research of China (Contract No. 2006CB302704). The authors would like to express their thanks to Dr. Abigail Lubow from Yale University for valuable help.

REFERENCES

1. International Technology Roadmap for Semiconductor (2009) available online at: www.itrs.net.
2. J. Lusakowski, W. Knap, Y. Meziani, J.P. Cesso, A. El Fatimy, R. Tauk, N. Dyakonova, G. Ghibaudo, F. Boeuf, and T. Skotnicki, *Solid-State Electron.* 50, 632 (2006). doi:10.1016/j.sse.2006.03.017.
3. D.A. Antoniadis, I. Aberg, C. Ni Chleirigh, O.M. Nayfeh, A. Khakifirooz, and J.L. Hoyt, *IBM J. Res. Dev.* 50, 363 (2006).
4. S.S. Chung, Y.J. Tsai, C.H. Tsai, P.W. Liu, Y.H. Lin, C.T. Tsai, G.H. Ma, S.C. Chien, and S.W. Sun, *2007 IEEE Conference on Electron Devices and Solid-State Circuits—EDSSC '07* (2007), pp. 23–26.
5. Z.Y. Cheng, M.T. Currie, C.W. Leitz, G. Taraschi, E.A. Fitzgerald, J.L. Hoyt, and D.A. Antoniadas, *IEEE Electron Device Lett.* 22, 321 (2001).
6. T.S. Drake, C. Ni Chleirigh, M.L. Lee, A.J. Pitera, E.A. Fitzgerald, D.A. Antoniadis, D.H. Anjum, J. Li, R. Hull, N. Klymko, and J.L. Hoyt, *J. Electron. Mater.* 32, 972 (2003).
7. F. Driussi, D. Esseni, L. Selmi, P.E. Hellstrom, G. Malm, J. Hallstedt, M. Ostling, T.J. Grasby, D.R. Leadley, and X. Mescot, *Solid-State Electron.* 52, 498 (2008). doi:10.1016/j.sse.2007.10.033.
8. T.A. Langdo, A. Lochtefeld, M.T. Currie, R. Hammond, V.K. Yang, J.A. Carlin, C.J. Vineis, G. Braithwaite, H. Badawi, M.T. Bulsara, and E.A. Fitzgerald, *IEEE International SOI Conference*, Williamsburg, VA, Oct 07–10 2002 (2002), pp. 211–212.
9. I. Lauer, T.A. Langdo, Z.Y. Cheng, J.G. Fiorenza, G. Braithwaite, A.T. Currie, C.W. Leitz, A. Lochtefeld, H. Badawi, M.T. Bulsara, M. Somerville, and D.A. Antoniadis, *IEEE Electron Device Lett.* 25, 83 (2004). doi:10.1109/led.2003.822686.
10. T.A. Langdo, M.T. Currie, Z.Y. Cheng, J.G. Fiorenza, M. Erdtmann, G. Braithwaite, C.W. Leitz, C. Vineis, J.A. Carlin, A. Lochtefeld, M.T. Bulsara, I. Lauer, D.A. Antoniadis, and M. Somerville, *Solid-State Electron.* 48, 1357 (2004). doi:10.1016/j.sse.2004.02.013.
11. J.L. Hoyt, H.M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E.A. Fitzgerald, and D.A. Antoniadis, *International Electron Devices 2002 Meeting, Technical Digest* (2002), pp. 23–26.
12. M.V. Fischetti, Z. Ren, P.M. Solomon, M. Yang, and K. Rim, *J. Appl. Phys.* 94, 1079 (2003). doi:10.1063/1.1585120.
13. S.E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, *IEEE International Electron Devices Meeting 2004, Technical Digest* (2004), pp. 221–224.
14. S.E. Thompson, G.Y. Sun, *International Symposium on VLSI Technology, Systems and Applications*, Hsinchu, Taiwan, Apr. 24–26 2006 (2006), pp. 46–47.
15. J.S. Lim, S.E. Thompson, and J.G. Fossum, *IEEE Electron Device Lett.* 25, 731 (2004). doi:10.1109/led.2004.837581.
16. S.E. Thompson, G.Y. Sun, Y.S. Choi, and T. Nishida, *IEEE Trans. Electron Devices* 53, 1010 (2006). doi:10.1109/ted.2006.872088.
17. S.S. Chung, E.R. Hsieh, D.C. Huang, C.S. Lai, C.H. Tsai, P.W. Liu, Y.H. Lin, C.T. Tsai, G.H. Ma, S.C. Chien, and S.W. Sun, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 435–438.
18. Y.C. Yeo, *3rd International SiGe Technology and Device Meeting*, Princeton, NJ, May 15–17 2006, pp. S177–S182. doi:10.1088/0268-1242/22/1/s42.
19. M. Saitoh, N. Yasutake, Y. Nakabayashi, T. Numata, and K. Uchida, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 573–576.

20. V. Chan, R. Rengarajan, N. Rovedo, W. Jin, T. Hook, P. Nguyen, J. Chen, E. Nowak, X.D. Chen, D. Lea, A. Chakravarti, V. Ku, S. Yang, A. Steegen, C. Baiocco, P. Shafer, H. Ng, S.F. Huang, and C. Wann, *2003 IEEE International Electron Devices Meeting, Technical Digest* (2003), pp. 77–80.
21. G. Scott, J. Lutze, M. Rubin, F. Nouri, and M. Manley, *International Electron Devices Meeting 1999 Technical Digest (Cat No99CH36318). International Electron Devices Meeting 1999 Technical Digest (Cat No99CH36318)* (1999). doi:10.1109/IEDM.1999.824277.
22. C.Y. Hsu, C.C. Lee, Y.T. Lin, C.Y. Hsieh, and M.J. Chen, *IEEE Trans. Electron Devices* 56, 1667 (2009). doi:10.1109/ted.2009.2024024.
23. M. Ishibashi, K. Horita, M. Sawada, M. Kitazawa, M. Igarashi, T. Kuroi, T. Eimori, K. Kobayashi, M. Inuishi, and Y. Ohji, *Jpn. J. Appl. Phys. 1* 44, 2152 (2005). doi:10.1143/jjap.44.2152.
24. A. Steegen, A. Lauwers, M. de Potter, G. Badenes, R. Rooyackers, and K. Maex, *2000 Symposium on VLSI Technology, Digest of Technical Papers* (2000), pp. 180–181.
25. X. Chen, S. Samavedam, V. Narayanan, K. Stein, C. Hobbs, C. Baiocco, W. Li, D. Jaeger, M. Zaleski, H.S. Yang, N. Kim, Y. Lee, D. Zhang, L. Kang, J. Chen, H. Zhuang, A. Sheikh, J. Wallner, M. Aquilino, J. Han, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kirshnan, X. Wang, M. Chudzik, M. Chowdhury, D. Nair, C. Reddy, Y.W. Teh, C. Kothandaraman, D. Coolbaugh, S. Pandey, D. Tekleab, A. Thean, M. Sherony, C. Lage, J. Sudijono, R. Lindsay, J.H. Ku, M. Khare, and A. Steegen, *VLSI Technology, 2008 Symposium on* June (2008), pp. 88–89.
26. C.-H. Ge, C.-C. Lin, C.-H. Ko, C.-C. Huang, Y.-C. Huang, B.-W. Chan, B.-C. Perng, C.-C. Sheu, P.-Y. Tsai, L.-G. Yao, C.-L. Wu, T.-L. Lee, C.-J. Chen, C.-T. Wang, S.-C. Lin, Y.-C. Yeo, and C. Hu, *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International* (2003), pp. 3.7.1–3.7.4.
27. C.C. Auth, A. Chun, J.-S. Dalis, A. Davis, A. Ghani, T. Glass, G. Glassman, T. Harper, M. Hattendorf, M. Hentges, P. Jaloviar, S. Joshi, S. Klaus, J. Kuhn, K. Lavric, D. Lu, M. Mariappan, H. Mistry, K. Norris, B. Rahhal-orabi, N. Ranade, P. Sandford, J. Shifren, L. Souw, V. Tone, K. Tambwe, F. Thompson, A. Towner, D. Troeger, T. Vandervoorn, P. Wallace, C. Wiedemer, J. Wiegand, and C. Wiegand, *VLSI Technology, 2008 Symposium on* June (2008), pp. 128–129.
28. S.Y. Wu, C.W. Chou, C.Y. Lin, M.C. Chiang, C.K. Yang, M.Y. Liu, L.C. Hu, C.H. Chang, P.H. Wu, C.I. Lin, H.F. Chen, S.Y. Chang, S.H. Wang, P.Y. Tong, Y.L. Hsieh, J.J. Liaw, K.H. Pan, C.H. Hsieh, C.H. Chen, J.Y. Cheng, C.H. Yao, W.K. Wan, T.L. Lee, K.T. Huang, C.C. Chen, K.C. Lin, L.Y. Yeh, K.C. Ku, S.C. Chen, C.W. Chang, H.J. Lin, S.M. Jang, Y.C. Lu, J.H. Shieh, M.H. Tsai, J.Y. Song, K.S. Chen, V. Chang, S.M. Cheng, S.H. Yang, C.H. Diaz, Y.C. See, and M.S. Liang, *2007 IEEE International Electron Devices Meeting, Vols 1 and 2* (2007), pp. 263–266.
29. F. Arnaud, J. Liu, Y.M. Lee, K.Y. Lim, S. Kohler, J. Chen, B.K. Moon, C.W. Lai, M. Lipinski, L. Sang, F. Guarin, C. Hobbs, P. Ferreira, K. Ohuchi, J. Li, H. Zhuang, P. Mora, Q. Zhang, D.R. Nair, D.H. Lee, K.K. Chan, S. Satadru, S. Yang, J. Koshy, W. Hayter, M. Zaleski, D.V. Coolbaugh, H.W. Kim, Y.C. Ee, J. Sudijono, A. Thean, M. Sherony, S. Samavedam, M. Khare, C. Goldberg, and A. Steegen, *Electron Devices Meeting, 2008 IEDM 2008 IEEE International* (2008).
30. P.R. Chidambaram, B.A. Smith, L.H. Hall, H. Bu, S. Chakravarthi, Y. Kim, A.V. Samoilov, A.T. Kim, P.J. Jones, R.B. Irwin, M.J. Kim, A.L.P. Rotondaro, C.F. Machala, and D.T. Grider, *Symposium on VLSI Technology*, Honolulu, HI, Jun. 15–17 2004 (2004), pp. 48–49.
31. K.W. Ang, K.J. Chui, A. Madan, L.Y. Wong, C.H. Tung, N. Balasubramanian, M.F. Li, G.S. Samudra, and Y.C. Yeo, *IEEE Electron Device Lett.* 28, 509 (2007). doi:10.1109/led.2007.896802.
32. A. Madan, G. Samudra, and Y.C. Yeo, *J. Appl. Phys.* 104 (2008). doi:10.1063/1.3000481.
33. K. Chui, K.W. Ang, A. Madan, H. Wang, C. Tung, L. Wong, Y. Wang, S. Choy, N. Balasubramanian, M.F. Li, G. Samudra, and Y. Yeo, *51th IEEE* International Electron Devices Meeting, Washington, DC, Dec. 4–7 2005 (2005), pp. 493–496.
34. F. Nouri, P. Verheyen, L. Washington, V. Moroz, I. De Wolf, M. Kawaguchi, S. Biesemans, R. Schreutelkamp, Y. Kim, M. Shen, X. Xu, R. Rooyackers, M. Jurczak, G. Eneman, K. De Meyer, L. Smith, D. Pramanik, H. Forstner, S. Thirupapuliyur, and G.S. Higashi, *50th IEEE International Electron Devices Meeting*, San Francisco, CA, Dec. 13–15 2004 (2004), pp. 1055–1058.
35. L. Smith, V. Moroz, G. Eneman, P. Verheyen, F. Nouri, L. Washington, M. Jurczak, O. Penzin, D. Pramanik, and K. De Meyer, *IEEE Electron Device Lett.* 26, 652 (2005). doi:10.1109/led.2005.853668.
36. K.W. Ang, K.J. Chui, V. Bliznetsov, Y.H. Wang, L.Y. Wong, C.H. Tung, N. Balasubramanian, M.F. Li, G. Samudra, and Y.C. Yeo, *IEEE International Electron Devices Meeting*, Washington, DC, Dec. 05–07 2005 (2005), pp. 503–506.
37. Z.B. Ren, G. Pei, J. Li, B. Yang, R. Takalkar, K. Chan, G. Xia, Z. Zhu, A. Madan, T. Pinto, T. Adam, J. Miller, A. Dube, L. Black, J.W. Weijtmans, E. Harley, A. Chakravarti, T. Kanarsky, R. Pal, I. Lauer, D.G. Park, and D. Sadana, *Symposium on VLSI Technology*, Honolulu, HI, Jun. 17–19 2008 (2008), pp. 172–173.
38. B. Yang, R. Takalkar, Z. Ren, L. Black, A. Dube, J.W. Weijtmans, J. Li, J.B. Johnson, J. Faltermeier, A. Madan, Z. Zhu, A. Turansky, G. Xia, A. Chakravarti, R. Pal, K. Chan, A. Reznicek, T.N. Adam, J.P. de Souza, E.C.T. Harley, B. Greene, A. Gehring, M. Cai, D. Aime, S. Sun, H. Meer, J. Holt, D. Theodore, S. Zollner, P. Grudowski, D. Sadana, D.G. Park, D. Mocuta, D. Schepis, E. Maciejewski, S. Luning, J. Pellerin, and E. Leobandung, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 51–54.
39. Y. Liu, O. Gluschenkov, J. Li, A. Madan, A. Ozcan, B. Kim, T. Dyer, A. Chakravarti, K. Chan, C. Lavoie, I. Popova, T. Pinto, N. Rovedo, Z. Luo, R. Loesing, W. Henson, and K. Rim, *Symposium on VLSI Technology 2007*, Kyoto, Japan, 2007 (2007), pp. 44–45.
40. Q.X. Xu, X.F. Duan, H. Qian, H.H. Liu, H.O. Li, Z.S. Han, M. Liu, and W.F. Gao, *IEEE Electron Device Lett.* 27, 179 (2006). doi:10.1109/led.2006.870248.
41. Q.X. Xu, X.F. Duan, H.H. Liu, Z.S. Han, and T.C. Ye, *IEEE Trans. Electron Devices* 54, 1394 (2007). doi:10.1109/TED.2007.895871.
42. C.H. Chen, T.L. Lee, T.H. Hou, C.L. Chen, C.C. Chen, J.W. Hsu, K.L. Cheng, Y.H. Chiu, H.J. Tao, Y. Jin, C.H. Diaz, S.C. Chen, and M.S. Liang, *2004 Symposium on VLSI Technology, Digest of Technical Papers* (2004), pp. 56–57.
43. T. Miyashita, T. Owada, A. Hatada, Y. Hayami, K. Ookoshi, T. Mori, H. Kurata, and T. Futatsugi, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 55–58.
44. A. Eiho, T. Sanuki, E. Morifuji, T. Iwamoto, G. Sudo, K. Fukasaku, K. Ota, T. Sawada, O. Fuji, H. Nii, M. Togo, K. Ohno, K. Yoshida, H. Tsuda, T. Ito, Y. Shiozaki, N. Fuji, H. Yamazaki, M. Nakazawa, S. Iwasa, S. Muramatsu, K. Nagaoka, M. Iwai, M. Ikeda, M. Saito, H. Naruse, Y. Enomoto, T. Kitano, S. Yamada, K. Imai, N. Nagashima, T. Kuwata, and F. Matsuoka, *2007 Symposium on VLSI Technology, Digest of Technical Papers* (2007), pp. 218–219.
45. E. Morifuji, A. Eiho, T. Sanuki, M. Iwai, and F. Matsuoka, *Jpn. J. Appl. Phys.* 48 (2009). doi:03120310.1143/jjap.48.031203.
46. C. Ortolland, P. Morin, C. Chaton, E. Mastromatteo, C. Populaire, S. Orain, F. Leverd, P. Stolk, F. Boeuf, and F. Arnaud, *2006 Symposium on VLSI Technology (IEEE Cat No 06CH37743C)*, 2 pp, CD-ROM (2006).
47. C. Ortolland, Y. Okuno, P. Verheyen, C. Kerner, C. Stapelmann, M. Aoulaiche, N. Horiguchi, and T. Hoffmann, *IEEE Trans. Electron Devices* 56, 1690 (2009). doi:10.1109/ted.2009.2024021.

48. G. Eneman, P. Verheyen, A. De Keersgieter, M. Jurczak, and K. De Meyer, *IEEE Trans. Electron Devices* 54, 1446 (2007). doi:10.1109/ted.2007.896367.
49. K.M. Tan, M.C. Yang, T.Y. Liow, R.T.P. Lee, and Y.C. Yeo, *IEEE Trans. Electron Devices* 56, 1277 (2009). doi:10.1109/ted.2009.2019388.
50. F. Andrieu, T. Ernst, C. Ravit, M. Jurczak, G. Ghibaudo, and S. Deleonibus, *IEEE Electron Device Lett.* 26, 755 (2005). doi:10.1109/led.2005.855413.
51. C. Gallon, C. Fenouillet-Beranger, S. Denorme, F. Boeuf, V. Fiori, N. Loubet, A. Vandooren, T. Kormann, M. Broekaart, P. Gouraud, F. Leverd, G. Imbert, C. Chaton, C. Laviron, L. Gabette, F. Vigilant, P. Garnier, H. Bernard, A. Tarnowka, R. Pantel, F. Pionnier, S. Jullian, S. Cristoloveanu, and T. Skotnicki, *International Conference on Solid State Devices and Materials*, Kobe, Japan, Sep 13–15 2005 (2006), pp. 3058–3063. doi:10.1143/jjap.45.30581.
52. S. Pidin, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, K. Ohkoshi, R. Nakamura, K. Kobayashi, K. Kawamura, T. Saiki, S. Fukuyama, S. Satoh, M. Kase, and K Hashimoto, *IEEE International Electron Devices Meeting 2004, Technical Digest* (2004), pp. 213–216.
53. Y.C. Liu, J.W. Pan, T.Y. Chang, P.W. Liu, B.C. Lan, C.H. Tung, C.H. Tsai, T.F. Chen, C.J. Lee, W.M. Wang, Y.A. Chen, H.L. Shih, L.Y. Tung, L.W. Cheng, T.M. Shen, S.C. Chiang, M.F. Lu, W.T. Chang, Y.H. Luo, D. Nayak, D. Gitlin, H.L. Meng, and C.T. Tsai, *IEEE International Electron Devices Meeting*, Washington, DC, Dec. 05–07 2005 (2005), pp. 855–858.
54. P. Verheyen, G. Eneman, R. Rooyackers, R. Loo, L. Eeckhout, D. Rondas, F. Leys, J. Snow, D. Shamiryan, M. Demand, and T.Y. Hoffman, *IEEE International Electron Devices Meeting*, Washington, DC, Dec. 05–07 2005 (2005), pp. 907–910.
55. L. Washington, F. Nouri, S. Thirupapuliyur, G. Eneman, P. Verheyen, V. Moroz, L. Smith, X.P. Xu, M. Kawaguchi, T. Huang, K. Ahmed, M. Balseanu, L.Q. Xia, M.H. Shen, Y. Kim, R. Rooyackers, K. De Meyer, and R. Schreutelkamp, *IEEE Electron Device Lett.* 27, 511 (2006). doi:10.1109/led.2006.875766.
56. R. Arghavani, L. Xia, H. M'Saad, M. Balseanu, G. Karunasiri, A. Mascarenhas, and S.E. Thompson, *IEEE Electron Device Lett.* 27, 114 (2006). doi:10.1109/led.2005.862277.
57. S. Mayuzumi, S. Yamakawa, D. Kosemura, M. Takei, K. Nagata, H. Akamatsu, K. Aamari, Y. Tateshita, H. Wakabayashi, M. Tsukamoto, T. Ohno, M. Saitoh, A. Ogura, and N. Nagashima, *2009 Symposium on VLSI Technology, Digest of Technical Papers* (2009), pp. 14–15.
58. N. Yasutake, T. Ishida, K. Ohuchi, N. Aoki, N. Kusunoki, S. Mori, I. Mizushima, T. Morooka, K. Yahashi, S. Kawanaka, K. Ishimaru, and H. Tshiuchi, *Solid-State Device Research Conference, 2006 ESSDERC 2006 Proceeding of the 36th European* (2006), pp. 77–80.
59. N. Yasutake, A. Azuma, T. Ishida, N. Kusunoki, S. Mori, H. Itokawa, L. Mizushima, S. Okamoto, T. Morooka, N. Aoki, S. Kawanaka, S. Inaba, and Y. Toyoshima, *2007 Symposium on VLSI Technology, Digest of Technical Papers* (2007), pp. 48–49.
60. S.E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z.Y. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, *IEEE Electron Device Lett.* 25, 191 (2004). doi:10.1109/led.2004.825195.
61. G. Giusi, F. Crupi, E. Simoen, G. Eneman, and M. Jurczak, *IEEE Trans. Electron Devices* 54, 78 (2007). doi:10.1109/ted.2006.887198.
62. A. Shickova, P. Verheyen, G. Eneman, R. Degraeve, E. Simoen, P. Favia, D.O. Klenov, E.S. Andres, B. Kaczer, M. Jurczak, P. Absil, H.E. Maes, and G. Groeseneken, *IEEE Trans. Electron Devices* 55, 3432 (2008). doi:10.1109/7ed.2008.2006919.
63. K.T. Lee, C.Y. Kang, M.S. Park, B.H. Lee, H.K. Park, H.S. Hwang, H.H. Tseng, R. Jammy, and Y.H. Jeong, *IEEE Electron Device Lett.* 30, 760 (2009). doi:10.1109/led.2009.2021007.
64. C.Y. Lu, H.C. Lin, and T.Y. Huang, *Electrochem Solid State Lett.* 9, G138 (2006). doi:10.1149/1.2173189.
65. C.S. Lu, H.C. Lin, Y.J. Lee, and T.Y. Huang, *2007 IEEE International Reliability Physics Symposium Proceedings—45th Annual* (2007), pp. 670–671.
66. S. Dey, M. Agostinelli, C. Prasad, X. Wang, and L. Shifren, *2006 IEEE International Reliability Physics Symposium Proceedings—44th Annual* (2006), pp. 461–464.
67. M.V. Fischetti and S.E. Laux, *J. Appl. Phys.* 80, 2234 (1996).
68. P. Su and J.J.Y. Kuo, *IEEE Electron Device Lett.* 28, 649 (2007). doi:10.1109/led.2007.900297.
69. S. Maeda, Y.S. Jin, J.A. Choi, S.Y. Oh, H.W. Lee, J.Y. Yoo, M.C. Sun, J.H. Ku, K. Lee, S.G. Bae, S.G. Kang, J.H. Yang, Y.W. Kim, and K.P. Suh, *2004 Symposium on VLSI Technology, Digest of Technical Papers* (2004), pp. 102–103.
70. G. Giusi, E. Simoen, G. Eneman, P. Verheyen, F. Crupi, K. De Meyer, C. Claeys, and C. Ciofi, *IEEE Electron Device Lett.* 27, 508 (2006). doi:10.1109/led.2006.875758.
71. E. Simoen, P. Verheyen, A. Shickova, R. Loo, and C. Claeys, *IEEE Electron Device Lett.* 28, 987 (2007). doi:10.1109/led.2007.906437.
72. C. Claeys, E. Simoen, S. Put, G. Giusi, and F. Crupi, *Solid-State Electron.* 52, 1115 (2008). doi:10.1016/j.sse.2008.04.035.
73. M. Yang, V.W.C. Chan, K.K. Chan, L. Shi, D.M. Fried, J.H. Stathis, A.I. Chou, E. Gusev, J.A. Ott, L.E. Burns, M.V. Fischetti, and M. Ieong, *IEEE Trans. Electron Devices* 53, 965 (2006). doi:10.1109/ted.2006.872693.
74. B. Yang, Y.M. Yang, D.A. Fried, C.D. Sheraw, A. Waite, K. Nummy, L. Black, S.D. Kim, H. Yin, B. Kim, S. Narasimha, X. Chen, M. Khare, S. Luning, and P. Agnello, *2007 International Workshop on Electron Devices and Semiconductor Technology* (2007), pp. 8–13.
75. K.L. Saenger, J.P. de Souza, K.E. Fogel, J.A. Ott, A. Reznicek, C.Y. Sung, D.K. Sadana, and H. Yin, *Appl. Phys. Lett.* 87 (2005). doi:10.1063/1.2138795.
76. K.L. Saenger, J.P. de Souza, K. Fogel, J.A. Ott, A. Reznicek, H. Yin, C.Y. Sung, and D.K. Sadana, *J. Electrochem. Soc.* 155, H80 (2008). doi:10.1149/1.2811908.
77. P. Batude, M. Vinet, A. Pouydebasque, C. Le Royer, B. Previtali, C. Tabone, J. Hartmann, L. Sanchez, L. Baud, V. Carron, A. Toffoli, F. Allain, V. Mazzocchi, D. Lafond, O. Thomas, O. Cueto, N. Bouzaida, D. Fleury, A. Amara, S. Deleonibus, and O. Faynot, *IEEE International Electron Devices Meeting*, Baltimore, MD, Dec. 7–9 2009 (2009), pp. 14.1.1–14.1.4. doi:10.1109/iedm.2009.5424352.
78. M. Yang, V. Chan, S.H. Ku, M. Ieong, L. Shi, K.K. Chan, C.S. Murthy, R.T. Mo, H.S. Yang, E.A. Lehner, Y. Surpris, F.F. Jamin, P. Oldiges, Y. Zhang, B.N. To, J.R. Holt, S.E. Steen, M.P. Chudzik, D.M. Fried, K. Bernstein, H. Zhu, C.Y. Sung, J.A. Ott, D.C. Boyd, and N Rovedo, *2004 Symposium on VLSI Technology, Digest of Technical Papers* (2004), pp. 160–161.
79. C.Y. Sung, H.Z. Yin, H.Y. Ng, K.L. Saenger, V. Chan, S.W. Crowder, J.H. Li, J.A. Ott, R. Bendernagel, J.J. Kempisty, V. Ku, H.K. Lee, Z.J. Luo, A. Madan, R.T. Mo, P.Y. Nguyen, G. Pfeiffer, M. Raccioppo, N. Rovedo, D. Sadana, J.P. de Souza, R. Zhang, Z.B. Ren, and C.H. Wann, *IEEE International Electron Devices Meeting 2005, Technical Digest* (2005), pp. 235–238.
80. S.-H. Lee, J. Huang, P. Majhi, P.D. Kirsch, B.-G. Min, C.-S. Park, J. Oh, W.-Y. Loh, C.-Y. Kang, B. Sassman, P.Y. Hung, S. McCoy, J. Chen, B. Wu, G. Moori, D. Heh, and C. Young, *2009 Symposium on VLSI Technology, Digest of Technical Papers* 4b (1) (2009), pp. 74–75 .
81. M.L. Lee, E.A. Fitzgerald, M.T. Bulsara, M.T. Currie, and A. Lochtefeld, *J. Appl. Phys.* 97 (2005). doi:01110110.1063/1.1819976.
82. T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama, and S. Takagi, *IEEE Electron Device Lett.* 26, 243 (2005). doi:10.1109/led.2005.844699.

83. S. Takagi, T. Tezuka, T. Irisawa, S. Nakaharai, T. Maeda, T. Numata, K. Ikeda, and N. Sugiyama, *Mater. Sci. Eng. B* 135, 250 (2006). doi:10.1016/j.mseb.2006.08.015.
84. S. Takagi, T. Tezuka, T. Irisawa, S. Nakaharai, T. Numata, K. Usuda, N. Sugiyama, M. Shichijo, R. Nakane, and S. Sugahara, *7th International Conference on Ultimate Integration on Silicon, Grenoble*, France, Apr. 20–21, 2006 (2007), pp. 526–536. doi:10.1016/j.ssc.2007.02.017.
85. S. Takagi, T. Mizuno, T. Tezuka, N. Sugiyama, S. Nakaharai, T. Numata, J. Koga, and K. Uchida, *5th European International Workshop on the Ultimate Integration of Silicon*, Leuven, Belgium, 2004, May 2005 (2005), pp. 684–694 doi: 10.1016/j.sse.2004.08.020.
86. S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, *IEEE Trans. Electron Devices* 55, 21 (2008). doi:10.1109/ted.2007.911034.
87. T. Low, Y.T. Hou, M.F. Li, C.X. Zhu, A. Chin, G. Samudra, L. Chan, and D.L. Kwong, *IEEE International Electron Devices Meeting*, Washington, D.C., Dec. 08–10 2003 (2003), pp. 691–694.
88. T. Irisawa, T. Numata, T. Tezuka, K. Usuda, N. Hirashita, N. Sugiyama, E. Toyoda, and S.L. Takagi, *IEEE Trans. Electron Devices* 53, 2809 (2006). doi:10.1109/ted.2006.884078.
89. J. Oh, P. Majhi, C.Y. Kang, R. Jammy, R. Joe, T. Sugawara, Y. Akasaka, T. Kaitsuka, T. Arikado, and M. Tomoyasu, *International Conference on Solid State Devices and Materials*, Tsukuba, Japan, Sep. 24–26 2008 (2009). doi:04c05510.1143/jjap.48.04c055.
90. T. Krishnamohan, Z. Krivokapic, K. Uchida, Y. Nishi, and K.C. Saraswat, *IEEE Trans. Electron Devices* 53, 990 (2006). doi:10.1109/ted.2006.872362.
91. L. Gomez, M. Canonico, M. Kim, P. Hashemi, and J.L. Hoyt, *J. Electron. Mater.* 37, 240 (2008). doi:10.1007/s11664-007-0337-8.
92. S. Joshi, S. Dey, M. Chaumont, A. Campion, and S.K. Banerjee, *J. Electron. Mater.* 36, 641 (2007). doi:10.1007/s11664-007-0137-1.
93. S. Dey, S. Joshi, D. Garcia-Gutierrez, M. Chaumont, A. Campion, M. Jose-Yacaman, and S.K. Banerjee, *J. Electron. Mater.* 35, 1607 (2006).
94. F.A. Trumbore, *Bell Syst. Tech. J.* 39, 205 (1960).
95. S.M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
96. A. Ritenour, A. Khakifirooz, D.A. Antoniadis, R.Z. Lei, W. Tsai, A. Dimoulas, G. Mavrou, and Y. Panayiotatos, *Appl. Phys. Lett.* 88, 3 (2006). doi:13210710.1063/1.2189456.
97. M. Kobayashi, T. Irisawa, B.M. Kope, Y. Sun, K. Saraswat, H. Philip Wong, P. Pianetta, and Y. Nishi, *VLSI Technology, 2009 Digest of Technical Papers 2009 Symposium on* 4B (2) (2009), pp. 76–77.
98. N. Taoka, W. Mizubayashi, Y. Morita, S. Migita, H. Ota, and S. Takagi, *VLSI Technology, 2009 Digest of Technical Papers 2009 Symposium on* T4B (4) (2009), pp. 80–81.
99. J. Mitard, B. De Jaeger, F.E. Leys, G. Hellings, K. Martens, G. Eneman, D.P. Brunco, R. Loo, J.C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C.H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M.M. Heyns, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 873–876.
100. J. Mitard, C. Shea, B. DeJaeger, A. Pristera, G. Wang, M. Houssa, G. Eneman, G. Hellings, W.-E. Wang, J.C. Lin, and F.E. Leys, *VLSI Technology, 2009 Digest of Technical Papers 2009 Symposium on* T4B (5) (2009), pp. 82–83.
101. N. Taoka, M. Harada, Y. Yamashita, T. Yamamoto, N. Sugiyama, and S.I. Takagi, *Appl. Phys. Lett.* 92 (2008). doi:10.1063/1.2899631.
102. D. Reinking, M. Kammler, N. Hoffmann, M. Horn von Hoegen, and K.R. Hofmann, *Solid State Device Research Conference, 1999 ESSDERC 1999 29th European* (1999), pp. 300–303.
103. C.O. Chui, H. Kim, D. Chi, B.B. Triplett, P.C. McIntyre, and K.C. Saraswat, *International Electron Devices 2002 Meeting, Technical Digest* (2002), pp. 437–440.
104. J.J.H. Chen, N.A. Bojarczuk, H.L. Shang, M. Copel, J.B. Hannon, J. Karasinski, E. Preisler, S.K. Banerjee, and S. Guha, *IEEE Trans. Electron Devices* 51, 1441 (2004). doi:10.1109/ted.2004.833593.
105. Y. Kamata, A. Takashima, Y. Kamimuta, and T. Tezuka, *VLSI Technology, 2009 Digest of Technical Papers 2009 Symposium on* 4B (3) (2009), pp. 78–79.
106. H. Shang, H. Okorn-Schimdt, J. Ott, P. Kozlowski, S. Steen, E.C. Jones, H.S.P. Wong, and W. Hanesch, *IEEE Electron Device Lett.* 24, 242 (2003). doi:10.1109/led.2003.810879.
107. H.L. Shang, H. Okorn-Schmidt, K.K. Chan, M. Copel, J.A. Ott, P.M. Kozlowski, S.E. Steen, S.A. Cordes, H.S.P. Wong, E.C. Jones, and W.E. Haensch, *International Electron Devices 2002 Meeting, Technical Digest* (2002), pp. 441–444.
108. T. Maeda, K. Ikeda, S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, *IEEE Electron Device Lett.* 26, 102 (2005). doi:10.1109/led.2004.841442.
109. S. Monfray, M.P. Samson, and D. Dutartre, *Electron Devices Meeting, 2007 IEDM 2007 IEEE International* (2007), pp. 693–696.
110. E. Batail, S. Monfray, C. Tabone, O. Kermarrec, J.F. Damlencourt, P. Gautier, G. Rabille, C. Arvet, N. Loubet, Y. Campidelli, J.M. Hartmann, A. Pouydebasque, V. Delaye, C. Le Royer, G. Ghibaudo, T. Skotnicki, and S. Deleonibus, *IEDM 2008 IEEE International Electron Devices Meeting Technical Digest* (2008), 4 pp. doi:10.1109/iedm.2008.4796704.
111. J. Oh, I. Ok, C.Y. Kang, M. Jamil, S.H. Lee, W.Y. Loh, J. Huang, B. Sassman, L. Smith, S. Parthasarathy, B.E. Coss, W.H. Choi, H.D. Lee, M. Cho, S.K. Banerjee, P. Majhi, P.D. Kirsch, H.H. Tseng, and R. Jammy, *2009 Symposium on VLSI Technology* (2009), pp. 238–239.
112. H.L. Shang, K.L. Lee, P. Kozlowski, C. D'Emic, I. Babich, E. Sikorski, M.K. Ieong, H.S.P. Wong, K. Guarini, and N. Haensch, *IEEE Electron Device Lett.* 25, 135 (2004). doi:10.1109/led.2003.823060.
113. D. Kuzum, K. Martens, T. Krishnamohan, and K.C. Saraswat, *Appl. Phys. Lett.* 95 (2009). doi:10.1063/1.3270529.
114. A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E.K. Evangelou, *Appl. Phys. Lett.* 89 (2006). doi:10.1063/1.2410241.
115. P. Tsipas and A. Dimoulas, *Appl. Phys. Lett.* 94 (2009). doi:10.1063/1.3068497.
116. D. Kuzum, T. Krishnamohan, A.J. Pethe, A.K. Okyay, Y. Oshima, Y. Sun, J.P. McVittie, P.A. Pianetta, P.C. McIntyre, and K.C. Saraswat, *IEEE Electron Device Lett.* 29, 328 (2008). doi:10.1109/led.2008.918272.
117. D. Kuzum, T. Krishnamohan, A. Nainani, S. Yun, P.A. Pianetta, H.S.P. Wong, and K.C. Saraswat, *2009 IEEE International Electron Devices Meeting (IEDM 2009)*. (2009), 4 pp. doi:10.1109/iedm.2009.5424322.
118. C.H. Lee, T. Nishimura, N. Saido, K. Nagashio, K. Kita, and A. Toriumi, *2009 IEEE International Electron Devices Meeting (IEDM 2009)* (2009), 4 pp. doi:10.1109/iedm.2009.5424323.
119. K. Kita, S.K. Wang, M. Yoshida, C.H. Lee, K. Nagashio, T. Nishimura, and A. Toriumi, *2009 IEEE International Electron Devices Meeting (IEDM 2009)* (2009), 4 pp. doi:10.1109/iedm.2009.5424243.
120. K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, *2009 IEEE International Electron Devices Meeting (IEDM 2009)* (2009), 4 pp. doi:10.1109/iedm.2009.5424248.
121. J.H. Park, M. Tada, D. Kuzum, P. Kapur, H.Y. Yu, H.S.P. Wong, and K.C. Saraswat, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 389–392.
122. K. Sawano, Y. Hoshi, K. Kasahara, K. Yamane, K. Hamaya, M. Miyao, and Y. Shiraki, *Appl. Phys. Lett.* 97, 162103 (2010). doi:10.1063/1.3503587.
123. J. Robertson and L. Lin, *2009 IEEE International Electron Devices Meeting* (2009), pp. 107–110.

124. K. Yamane, K. Hamaya, Y. Ando, Y. Enomoto, K. Yamamoto, T. Sadoh, and M. Miyao, *Appl. Phys. Lett.* 96 (2010). doi:10.1063/1.3368701.
125. K. Martens A. Firrinciel, R. Rooyackers, B. Vincent, R. Loo, S. Locorotondo, E. Rosseel, T. Vandeweyer, G. Hellings, B. De Jaeger, M. Meuris, P. Favia, H. Bender, B. Douhard, J. Delmotte, W. Vandervorst, E. Simoen, G. Jurczak, D. Wouters, and J.A. Kittl, *IEEE Electron Device Meeting* (2010), pp. 18.14.11–18.14.14.
126. T. Tezuka, S. Nakaharai, Y. Moriyama, N. Hirashita, E. Toyoda, N. Sugiyama, T. Mizuno, and S.I. Takagi, *25th Symposium on VLSI Technology, Kyoto*, Japan, Jun 14–16, 2005 (2005), pp. 80–81.
127. B. Vincent, J.F. Damlencourt, Y. Morand, A. Pouydebasque, C. Le Royer, L. Clavelier, N. Dechoux, P. Rivallin, T. Nguyen, S. Cristoloveanu, Y. Campidelli, D. Rouchon, M. Mermoux, S. Deleonibus, D. Bensahel, and T. Billon, *Mater. Sci. Semicond. Process.* 11, 205 (2008). doi:10.1016/j.mssp.2008.10.005.
128. C. Le Royer, B. Vincent, L. Clavelier, J.F. Damlencourt, C. Tabone, P. Batude, D. Blachier, R. Truche, Y. Campidelli, Q.T. Nguyen, S. Cristoloveanu, S. Soliveres, G. Le Carval, F. Boulanger, T. Billon, D. Bensahel, and S. Deleonibus, *IEEE Electron Device Lett.* 29, 635 (2008). doi:10.1109/led.2008.923539.
129. W. Van Den Daele, E. Augendre, C. Le Royer, J.F. Damlencourt, B. Grandchamp, and S. Cristoloveanu, *Solid-State Electron.* 205 (2010). doi:10.1016/j.sse.2009.12.020.
130. K. Romanjek, E. Augendre, W. Van Den Daele, B. Grandchamp, L. Sanchez, C. Le Royer, J.M. Hartmann, B. Ghyselen, E. Guiot, K. Bourdelle, S. Cristoloveanu, F. Boulanger, and L. Clavelier, *Microelectron. Eng.* 86, 1585 (2009). doi:10.1016/j.mee.2009.03.069.
131. J.Q. Lin, S. Lee, H.J. Oh, W.F. Yang, G.Q. Lo, D.L. Kwong, and D.Z. Chi, *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec. 15–17 2008 (2008), pp. 401–404.
132. H.C. Chin, M. Zhu, C.H. Tung, G.S. Samudra, and Y.C. Yeo, *IEEE Electron Device Lett.* 29, 553 (2008). doi:10.1109/led.2008.921393.
133. N. Li, E.S. Harmon, J. Hyland, D.B. Salzman, T.P. Ma, Y. Xuan, and P.D. Ye, *Appl. Phys. Lett.* 92 (2008). doi:10.1063/1.2908926.
134. M. Yokoyama, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, *2009 Symposium on VLSI Technology* (2009), pp. 242–243.
135. N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C.K. Gaspe, M.B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 363–366.
136. Y.N. Sun, E.W. Kiewra, J.P. de Souza, J.J. Bucchignano, K.E. Fogel, D.K. Sadana, and G.G. Shahidi, *IEEE Electron Device Lett.* 30, 5 (2009). doi:10.1109/led.2008.2008827.
137. M. Kobayashi, P.T. Chen, Y. Sun, N. Goel, P. Majhi, M. Garner, W. Tsai, P. Pianetta, and Y. Nishi, *Appl. Phys. Lett.* 93 (2008). doi:18210310.1063/1.3020298.
138. H. Matsuzaki, T. Maruyama, T. Kosugi, H. Takahashi, M. Tokumitsu, and T. Enoki, *IEEE International Electron Devices Meeting 2005, Technical Digest* (2005), pp. 795–798.
139. Z. Zhen, F. Pagette, C. D'Emic, B. Yang, C. Lavoie, A. Ray, Y. Zhu, M. Hopstaken, S. Maurer, C. Murray, M. Guillorn, D. Klaus, J.J. Bucchignano, J. Bruley, J. Ott, A. Pyzyna, J. Newbury, W. Song, G. Zuo, K.L. Lee, A. Ozcan, J. Silverman, Q. Ouyang, and D.G. Park, W. Haensch, and P.M. Solomon, *2010 International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA 2010)* (2010), pp. 154–155. doi:10.1109/vtsa.2010.5488908.
140. T. Kim, D. Kim, J.A. del Alamo, *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec. 6–8 (2010), pp. 30.37.31–30.37.34.
141. A.K. Baraskar, M.A. Wistey, V. Jain, U. Singisetti, G. Burek, B.J. Thibeault, Y.J. Lee, A.C. Gossard, and M.J.W. Rodwell, *J. Vac. Sci. Technol. B* 27, 2036 (2009). doi:10.1116/1.3182737.
142. A. Baraskar, M.A. Wistey, V. Jain, E. Lobisser, U. Singisetti, G. Burek, Y.J. Lee, B. Thibeault, A. Gossard, and M. Rodwell, *J. Vac. Sci. Technol. B* 28, C5I7 (2010). doi:10.1116/1.3454372.
143. S.H. Kim, M. Yokoyama, N. Taoka, R. Iida, S. Lee, R. Nakane, Y. Urabe, N. Miyata, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec. 6–8 2010 (2010), pp. 26.26.21–26.26.24.
144. L. Di, A.W. Fang, J.E. Bowers, *58th Electronic Components & Technology Conference, Proceedings* (2008), pp. 979–984.
145. C. Hock-Chun, G. Xiao, L. Xinke, L. Zhe, and Y. Yee-Chia, *2009 Symposium on VLSI Technology* (2009), pp. 244–245.
146. S. Oktyabrsky and P. Ye, *Fundamentals of III–IV Semiconductor MOSFETs (Springer US 2010)*, pp. 349–378. doi:10.1007/978-1-4419-1547-4.
147. R. Mohammad, S. Katircioglu, and M. El-Hasan, *J. Mater. Sci.* 43, 2935 (2008). doi:10.1007/s10853-007-1794-4.
148. M. Radosavljevic, T. Ashley, A. Andreev, S.D. Coomber, G. Dewey, M.T. Emeny, M. Fearn, D.G. Hayes, K.P. Hilton, M.K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S.J. Smith, M.J. Uren, D.J. Wallis, P.J. Wilding, and R. Chau, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 727–730.
149. D. Varghese, Y. Xuan, Y.Q. Wu, T. Shen, P.D. Ye, and M.A. Alam, *IEEE International Electron Devices Meeting 2008, Technical Digest* (2008), pp. 379–382.
150. A. Nainani, S. Raghunathan, D. Witte, M. Kobayashi, T. Irisawa, T. Krishnamohan, K. Saraswat, B.R. Bennett, M.G. Ancona, and J.B. Boos, *2009 IEEE International Electron Devices Meeting* (2009), pp. 801–804.
151. A Nainani, D Kim, T Krishnamohan, K Saraswat, *2009 International Conference on Simulation of Semiconductor Processes and Devices* (2009), pp. 47–50.
152. T.I. Aneesh Nainani, Z. Yuan, Y. Sun, T. Krishnamohan, M. Reason, B.R. Bennett, J.B. Boos, M.G. Ancona, Y. Nishi, and K.C. Saraswat, *2010 IEEE International Electron Devices Meeting* (2010), pp. 6.4.1–6.4.4.
153. S. Suthram, Y. Sun, P. Majhi, I. Ok, H. Kim, H.R. Harris, N. Goel, S. Parthasarathy, A. Koehler, T. Acosta, T. Nishida, H.H. Tseng, W. Tsai, J. Lee, R. Jammy, and S.E. Thompson, *2008 Symposium on VLSI Technology* (2008), pp. 143–144.
154. M.K. Hudait, G. Dewey, S. Datta, J.M. Fastenau, J. Kavalieros, W.K. Liu, D. Lubyshev, R. Pillarisetty, W. Rachmady, M .Radosavljevic, T. Rakshit, and R. Chau, *2007 IEEE International Electron Devices Meeting, Vols 1 and 2* (2007), pp. 625–628.
155. M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M.K. Hudait, J.M. Fastenau, J. Kavalieros, W.K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, *2009 IEEE International Electron Devices Meeting* (2009), pp. 292–295.
156. M. Yokoyama R. Iida, S.H. Kim, N. Taoka, Y. Urabe, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, *2010 IEEE International Electron Devices Meeting* (2010), pp. 3.1.1–3.1.2.
157. R.J.W. Hill, C. Park, J. Barnett, J. Price, J. Huang, N. Goel, W.Y. Loh, J. Oh, C.E. Smith, P. Kirsch, P. Majhi, and R. Jammy, *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec. 6–8 2010 (2010), pp. 6.2.1–6.2.4.
158. J. Fiorenza, M. Carroll, and A. Lochtefeld, *Compound Semiconductor* (2009), pp. 21–23.
159. J.S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochtefeld, *Appl. Phys. Lett.* 90 (2007). doi:10.1063/1.2435603.
160. R. Loo, G. Wang, L. Souriau, J.C. Lin, S. Takeuchi, G. Brammertz, and M. Caymax, *J. Electrochem. Soc.* 157, H13 (2010). doi:10.1149/1.3244564.
161. J.S. Park, M. Curtin, J.M. Hydrick, J. Bai, J.T. Li, Z. Cheng, M. Carroll, J.G. Fiorenza, and A. Lochtefeld, *Electrochem. Solid State Lett.* 12, H142 (2009). doi:10.1149/1.3077178.

162. J.Z. Li, J. Bai, J.M. Hydrick, J.G. Fiorenza, C. Major, M. Carroll, Z. Shellenbarger, and A. Lochtefeld, *ECS Trans.* 18, 887 (2009). doi:10.1149/1.3096551.
163. J.Z. Li, J. Bai, C. Major, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, *J. Appl. Phys.* 103 (2008). doi:10.1063/1.2924410.
164. J.Z. Li, J.M. Hydrick, J.S. Park, J. Li, J. Bai, Z.Y. Cheng, M. Carroll, J.G. Fiorenza, A. Lochtefeld, W. Chan, and Z. Shellenbarger, *J. Electrochem. Soc.* 156, H574 (2009). doi:10.1149/1.3129463.
165. A. Lubow, S. Ismail-Beigi, and T.P. Ma, *Appl. Phys. Lett.* 96 (2010). doi:10.1063/1.3367708.