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The Distribution Tail of LWIR HgCdTe-on-Si FPAs: a Hypothetical Physical Mechanism

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A model is proposed to explain disparities found in the operability values and histograms for long-wavelength infrared HgCdTe focal-plane arrays fabricated on Si substrates compared with those fabricated on CdZnTe. The starting point for the model is the close agreement between the aerial density of discrete species (particles, contamination spots, crystalline defects on Si surface) in various interfaces in the HgCdTe/CdTe/Si structure and the density of failed pixels in the array. The density of discrete species is acquired by applying a newly developed variation of the secondary-ion mass spectrometry (SIMS) depth-profiling technique to samples that have been deuterated to enhance detection. A mechanism of selective activation of threading dislocations in a HgCdTe layer on Si is proposed to link discrete species with failed detector pixels.

Key words: HgCdTe, discrete species, Si, FPA, dislocation, enhanced diffusion, diffusion pipes

INTRODUCTION

The industrial baseline process for producing long-wavelength infrared (LWIR) focal-plane arrays (FPAs) involves molecular-beam epitaxy of $Hg_{1-x}Cd_xTe$ on $Cd_{1-y}Zn_yTe$ substrates. The $Cd_{1-y}Zn_yTe$ substrate wafer alloy composition is tuned to effect a nearly perfect lattice-parameter match to the HgCdTe layer. A currently favored alternative technology involves replacement of the expensive, not readily available, and relatively small-area CdZnTe wafers with Si wafers. Si wafers offer thermal matching to the Si readout integrated circuit (ROIC), together with thermal cycling reliability, mechanical strength, and large size over CdZnTe substrates. A potential drawback of Si, however, is the high density of threading dislocations in the HgCdTe epilayer, a result of the 19% lattice-parameter mismatch. Indeed, dislocation density values in state-of-the-art HgCdTe on Si and on CdZnTe are measured to be $\sim 5 \times 10^6$ cm^{-2} and $\sim 5 \times 10^4$ cm^{-2}, respectively. The correlation between dislocation density value and the performance of diode arrays on CdZnTe has been found to be so high that etch pit density (EPD) measurements on smaller pieces of the same layer are often used to screen layers prior to device processing. It was only natural to assume that the higher dislocation density in HgCdTe/Si was responsible for the lower operability values of LWIR FPAs on Si as compared with those on CdZnTe. In this study, we examine this supposition by measuring and comparing layer and device characteristics of both structures. We find little correlation between EPD and device performance and search for an

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explanation of lower performance that is not based entirely on dislocation density.

EXPERIMENTAL PROCEDURES

LWIR HgCdTe layers were deposited by molecular-beam epitaxy on a composite substrate consisting of a (211) Si wafer, ZnTe nucleation layer, and CdTe buffer layer whose thickness was ~10 μm. These structures were examined by a variety of techniques. Atomic force microscopy (AFM) and optical microscopy were used to investigate defects at the HgCdTe surface after submerging a sample in a Benson dislocation-revealing etch.[1]

In a previously reported examination of the impurity content of HgCdTe layers that had been exposed to deuterium,[2,3] the existence of deuterium in the epilayers allowed the detection of defect-related features by a newly developed method using the SIMS technique. This so-called ^{2}H/SIMS/crater technique, first reported in Ref. 4, was used extensively in the current study and is responsible for the main results of this investigation. SIMS imaging was employed to provide additional spatial information on impurities found in the epilayers.

HgCdTe p–n epilayers were deposited and subjected to standard activation anneals before fabrication into 640 × 480 detector arrays. Detector arrays of photodiodes were delineated using conventional lithographic techniques. FPAs were operated at 84 K with f# = 3.5 to simulate tactical conditions. Noise equivalent temperature difference (NEΔT) values were measured for each pixel in the array.

RESULTS AND DISCUSSION

State-of-the-art NEΔT histograms and operability values for a 9.4-μm-cutoff-wavelength HgCdTe on Si-LWIR-FPA measured using tactical conditions (84 K, f# = 3.5) are shown in Fig. 1. Median NEΔT and operability for the Si-based FPA are slightly inferior to those for the CdZnTe FPA.[5] The tail in the distribution at higher NEΔT values is typical of FPAs on Si. The extent of the tail, and the concomitant operability value, vary according to device design, temperature, bias, etc., but the effect is seen in FPAs from a variety of manufacturers.

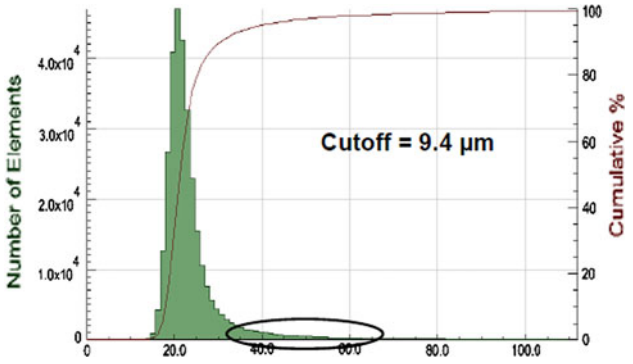

Fig. 1. Histograms of noise equivalent temperature difference values for HgCdTe LWIR FPAs on Si.

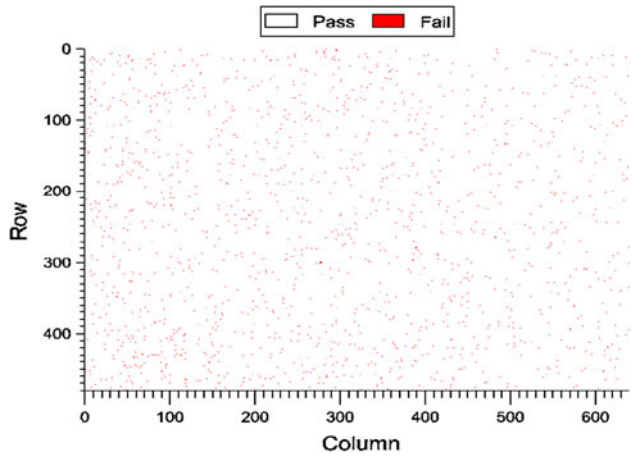

Fig. 2. Spatial distribution of failed pixels for HgCdTe LWIR FPAs on Si.

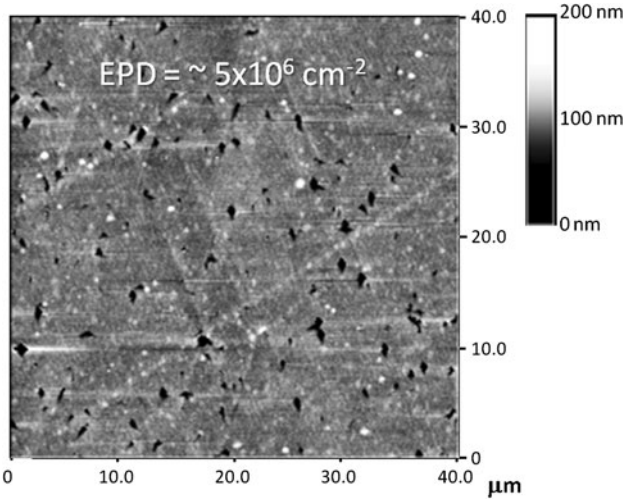

Fig. 3. Atomic force micrograph of etch pits formed in HgCdTe/CdTe/Si using the Benson etch.

In Fig. 2, we show a spatial map of failed pixels, where a failed device is defined as one with a NEΔT value that lies in the tail and outside of a limit set by a particular infrared system's specifications.

It is evident that failed pixels are uniformly distributed. Their density, calculated from the map in Fig. 2, is ~2 × 10^3 cm^{-2}. The origin of failed pixels in the distribution tail is not understood. For reasons stated earlier, the conventional explanation has been that it is linked to the dislocation density resulting from the large lattice mismatch and is therefore fundamental in nature.

In Fig. 3, we show an AFM image of the surface of a HgCdTe layer deposited on Si and subjected to the recently developed Benson etch[1] that decorates a

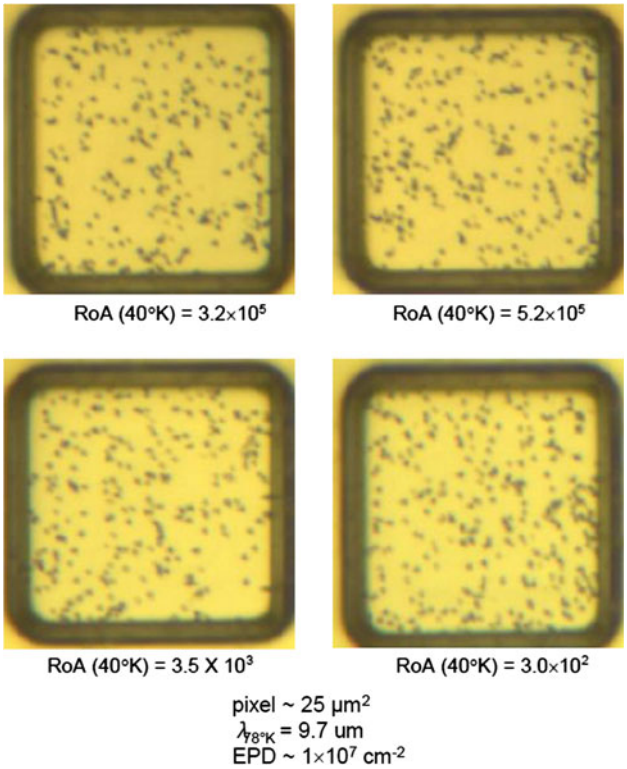

Fig. 4. Optical micrographs of etch pits in individual pixels of the LWIR HgCdTe FPA.

threading dislocation as it emerges from the free surface.

The revealed dislocations are mostly discrete and uniformly distributed with a density of $\sim 5 \times 10^6$ cm^{-2}. This is a state-of-the-art value that has been measured for HgCdTe on Si in many laboratories over the past decade. The discrepancy between the density of failed pixels and threading dislocations is striking.

A more microscopic confirmation of the lack of correspondence between performance and dislocation content of pixels is given in Fig. 4.

An FPA was dismantled after R_0A values were acquired for a large number of devices. Four devices with R_0A values differing by factors of 100 and 1000 were identified. EPD was then measured for these devices. Optical micrographs of etch pits in the devices, along with their R_0A values, are given in Fig. 4. EPD values were the same for the four pixels: $\sim 1 \times 10^7$ cm^{-2}. A conclusion from this data is that some factor other than dislocation density must be sought to explain the tail of failed pixels for LWIR HgCdTe devices on Si.

As part of a search for an alternative explanation for failed pixels, we applied the new version of the SIMS technique[4] to HgCdTe/CdTe/Si structures. Discrete species in the CdTe/Si interfacial region were detected that had not been previously reported. The technique consists of hydrogenation of a sample with ^{2}H and subsequent sputtering in a SIMS system with an ion beam optimized for revealing defects, in conjunction with compositional monitoring utilizing the depth profile of the Te sublattice.[6,7] Because the concentration of Te species in this technique is continuously monitored, sputtering can be stopped at any desired location in the heteroepitaxial structure. This ability permits investigation of the different interfaces including HgCdTe/CdTe, CdTe/ZnTe, and ZnTe/Si. In particular, microscopic plan-view analysis of an interface can be obtained by observing the floor of the sputtered crater. In Fig. 5 we show examples of these images for two HgCdTe/CdTe/Si structures.

In these examples, the sputtering was stopped in the ZnTe nucleation layer. We speculate that the

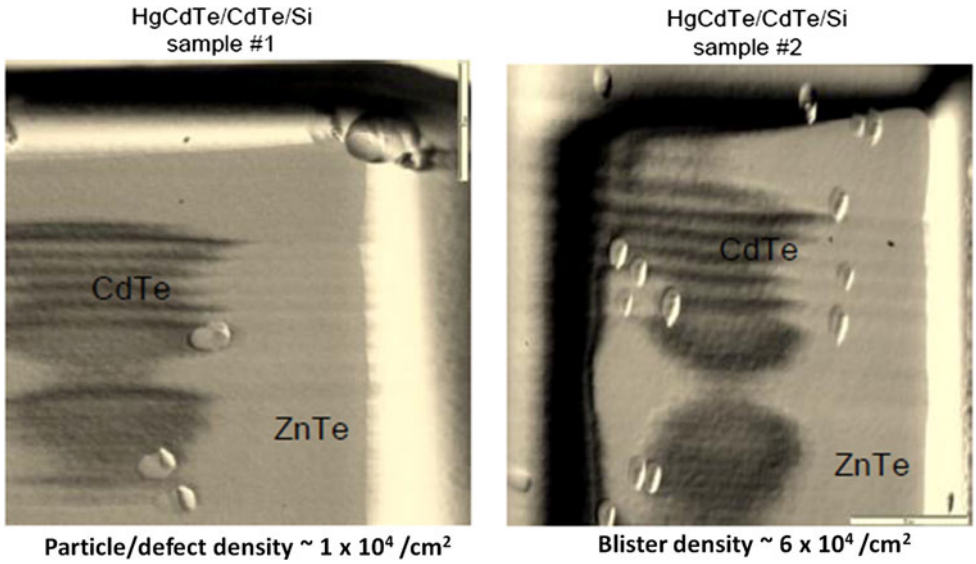

Fig. 5. Optical micrographs of features in the floor of SIMS craters in HgCdTe/CdTe/Si. These floors are located in the CdTe/Si interfacial region.

blisters shown in the images are associated with discrete species, such as particles and/or contamination spots and crystalline defects on the Si substrate, that have gettered ^{2}H during hydrogenation and have swollen under the influence of the rastered ion beam. The irregular shape of the blisters suggests clusters of discrete species under the surface of the ZnTe nucleation layer and therefore on the surface of the Si substrate.

The images in Fig. 5 are illustrations of the maximum (6×10^4 cm^{-2}) and minimum (1×10^4 cm^{-2}) density of blisters found in all the craters we examined (~20). The existence of discrete species and their location near the ZnTe/Si interface were confirmed by scanning Auger microscopy (SAM) measurements.[8] Additional information on the discrete species was obtained using a combination of SIMS depth profiling[9] and SIMS imaging.[10] Because of SIMS imaging's low sensitivity, a very high ion count ($>10^{19}$ cm^{-3}) from the respective element is required. SIMS imaging of an element in the floor of the sputtered crater provides information regarding the relative size and density of the discrete species. In Fig. 6, SIMS and SIMS imaging is shown for a sample on which discrete species were previously detected by the ^{2}H/SIMS/crater technique. A SIMS depth profile of carbon shows a stepwise increase in C concentration in the ZnTe/Si interfacial region. At a location estimated to be ~0.65 μm from the Si surface, SIMS imaging of carbon shows two bright spots, suggesting the existence of carbon-rich defects/particles. SIMS imaging of carbon closer to the Si surface (not shown here) exhibits a higher density of irregular spots which suggest defects/contamination on the Si surface. Other types of discrete species with various chemical compositions near the ZnTe/Si interface have been observed by the SAM technique.[8] We note that the density of discrete species in the ZnTe/Si interfacial region is in closer agreement with the density of failed pixels than is the EPD of the HgCdTe epilayer.

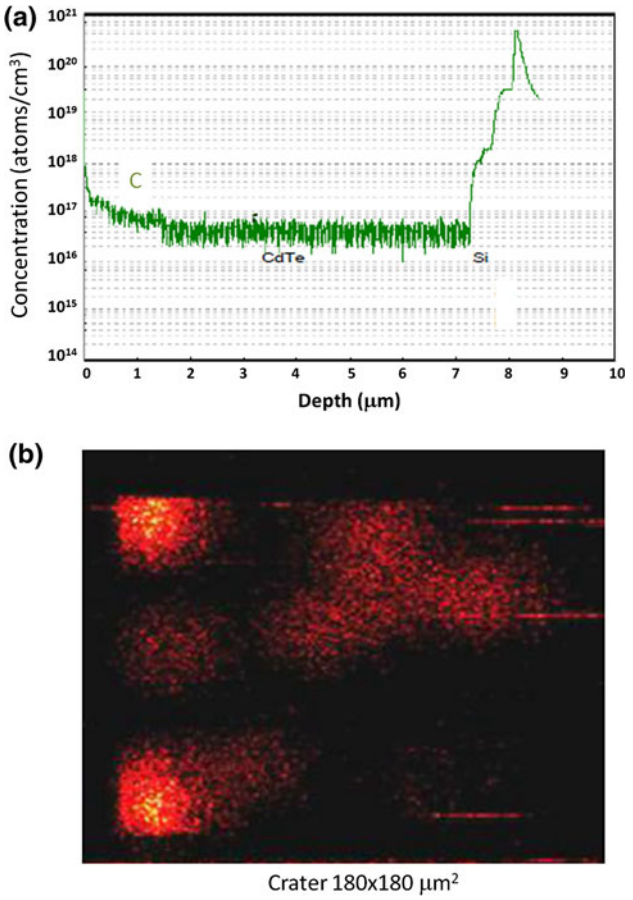

Fig. 6. (a) SIMS depth profile of carbon concentration in an epitaxial layer of CdTe on a Si substrate. (b) SIMS image of C at CdTe/Si interfacial region where C shows the highest concentration.

Model

We now propose a physical mechanism to link the defects and/or impurities present in the CdTe/Si interfacial region, the threading dislocations present in HgCdTe/CdTe/Si structures, and failed pixels in an FPA.

A hypothetical mechanism aimed at explaining the generation of killer dislocations responsible for failed devices emerged from the data on HgCdTe-on-Si materials and arrays. Shown in Fig. 7 is the model, which addresses the factors thought to have the highest probability of generating killer dislocations. These factors are the Si surface, threading dislocations/clusters generated in the interfacial region, discrete species existing at the ZnTe/Si interface, and impurities diffusing from the interfacial region.

The model assumes that dislocations that cause pixels to fail, termed "killer" dislocations, are a small fraction (~1×10^3 cm^{-2}) of the dislocations that thread through the depletion region of the electrical junction. For the threading dislocations to become responsible for device failure they must be activated by feeding deleterious impurities from the CdTe/Si interfacial region to the depletion region of the device electrical junction. Only in this way do threading dislocations become killer dislocations.

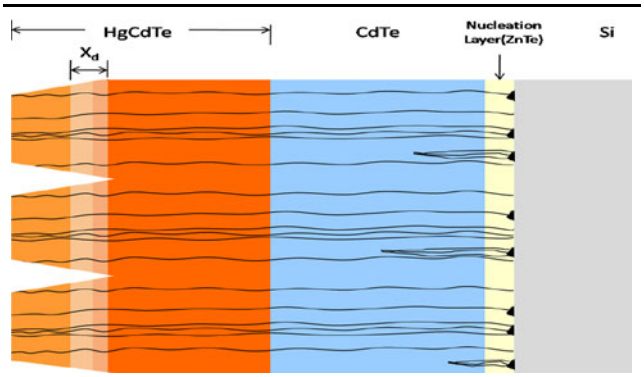

Fig. 7. A simplified model of the hypothetical physical mechanism.

Other factors that may certainly cause failure of devices, such as precipitates, defects in the HgCdTe/CdTe interface, and defects in the CdTe/HgCdTe passivation interface, are not considered.

Parameters Required for the Hypothetical Physical Mechanism

The model is constructed with parameters derived from the data on HgCdTe/CdTe/Si presented earlier. The first parameter includes impurities in the depletion region which may adversely affect device performance. It should be noted that some impurities can be more deleterious than others.

A second parameter is the nucleation layer, which may play a significant role in the generation of killer defects. Nucleation layer characteristics may affect the fraction of dislocations reaching the electrical junction.[11] The characteristics for a good ZnTe nucleation layer include optimized material properties for suppressing dislocations and serving as a barrier for impurity diffusion.

The third parameter includes discrete species (particles and/or contamination, crystalline defects on Si surface) present at the CdTe/Si interfacial region. These species may getter impurities from the surrounding region, thereby becoming discrete diffusion sources with much higher concentration than in the remaining lateral distribution. Such species may also generate pathways for impurity diffusion. Discrete species present in the nucleation layer are key to the conversion of a dislocation channel into an activated channel (killer dislocation).

Both lattice mismatch and discrete species detected in the interfacial layer generate a high number of dislocations and cluster dislocations. Depending on the nucleation layer characteristics, a fraction of these dislocations become threading dislocations of individual and cluster type reaching the electrical junction (observed by EPD). Threading dislocations generated in the CdTe/Si interfacial layer due to the lattice mismatch are likely to be predominantly individual threading dislocations. Threading dislocations generated by the discrete species (particles, contamination, crystalline defects on Si) present in the ZnTe/Si interface are predominantly cluster-type threading dislocations. Both individual and cluster threading dislocations become activated (killer dislocations) when carrying deleterious impurities to the depletion region of the electrical junction. The diffusion of impurities through these threading dislocations occurs with a higher diffusion coefficient than diffusion through the lattice. This process of enhanced diffusion through dislocations leads to the term enhanced diffusion pipe.

Selective Generation of Killer Dislocations

The mechanism whereby threading dislocations become activated is the principle behind the hypothetical physical mechanism.

Generation of killer dislocations will occur by a selection mechanism. The selection condition is proximity or coincidence of pipes with discrete impurity sources. The probability of proximity and/or a coincidence event to occur is key for killer dislocation formation, and it depends as well on the nucleation layer characteristics.

This selective process may result in a much lower density of activated threading dislocations than the density of discrete sources present in the CdTe/Si interfacial layer (1×10^4 cm^{-2} to 6×10^4 cm^{-2}), since only a fraction of the thus activated dislocations will thread through the structure to the depletion region to become killer dislocations. This process depends on the nucleation layer characteristics. Examples of selective generation of killer dislocations are shown schematically in Fig. 8a, b.

The highest probability of killer dislocation generation requires coincidence in location of discrete diffusion sources of any kind with a cluster dislocation. This is the case of cluster dislocations generated by discrete species (particles, contamination or crystalline defects on Si) as shown in Fig. 8a. Included in the figure is a coincidence example which does not result in a threading dislocation (pipe). The proximity of cluster dislocations to a discrete diffusion source (Fig. 8b) may add a small percentage of killer dislocations. Similarly, in this case, not all the proximity cases will result in a threading dislocation, as shown in the figure. The probability of activation of any threading dislocation regardless of the nature of dislocation could be highly dependent on the impurity involved.

The probability of dislocation activation will increase if the nucleation layer is not optimized to be an effective barrier for diffusion and for suppression of dislocation formation, for contamination minimization, and for structural integrity uniformity.

Note that the blister density ($\sim 10^4$ cm^{-2}), measured in Fig. 5, and failed pixel density (Fig. 2), differ by only a factor of 10. Considering the selection criteria for threading dislocation activation, it is more likely that failed pixels are associated with discrete defects in the CdTe/Si interfacial region than with the overall threading dislocation density ($\sim 5 \times 10^6$ cm^{-2}) measured at the HgCdTe surface by EPD.

Therefore, selective criteria in conjunction with the density of discrete species in the ZnTe interfacial layer and with the nucleation layer characteristics could lead to killer dislocation density in much closer agreement with the density of failed pixels.

The Effect of Killer Defects on Devices

Killer defects are, therefore, activated pipes which occur in the process of enhanced diffusion of impurities from discrete sources. These activated pipes could then generate leakage current, severely affecting device performance. Hence, these pipes are electrically active pipes.

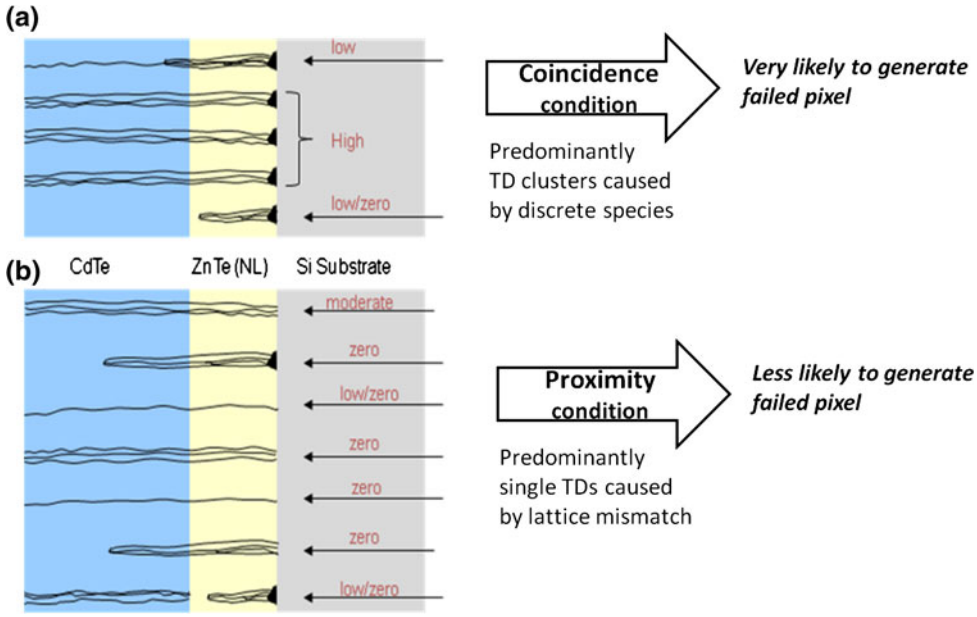

Fig. 8. Examples of the selective generation of killer dislocations in a HgCdTe/CdTe/Si epitaxial structure: (a) coincidence and (b) proximity. Arrows indicate the probability (zero, low, moderate or high) for which situations may lead to a failed pixel. The highest probability for a failed pixel requires the "coincidence condition" (a). The lowest probability for a failed pixed occurs in the case of the "proximity condition" (b).

A shunt component to the *I–V* may be generated by a low-resistivity path across the depletion region created by the Cottrell cloud of impurities or interstitials along the diffusion pipe.[12] Poorly performing HgCdTe/Si diodes (processed by ion implantation) due to shunt leakage currents have been found in Ref. 13. Tunneling components to the HgCdTe/Si *I–V* curve may be generated by the traps existing in the depletion region introduced by impurities traveling through the pipes. The effect of these leakage currents on the electrical junction of the device would depend on the device technology and on the working conditions of the device. As a consequence, the tail distribution measured under various operating conditions may be explained by either different types or behavior of impurities in the killer dislocations.

Link Between the Data and the Model

Examples of various discrete species (particles, contamination spots, crystalline defects on Si substrate) detected by using the ^{2}H/SIMS/crater technique have been reported in Ref. 4. We believe that any of these discrete species may act as the gettering center for impurities present in the surroundings. In our model, these centers become potential sources for impurity diffusion into the depletion region of the device electrical junction in HgCdTe by an enhanced mechanism via threading dislocation channels (pipes).

Experimental evidence of micropipes in HgCdTe-on-Si is shown in Fig. 9. Micropipes in (112) material have been attributed to threading screw dislocations (the screw dislocation is of the form $\{\bar{1}\bar{1}1\}\langle 1\bar{1}0\rangle$).[14] Micropipes can form at the center of screw dislocations during MBE deposition. The spiral pattern observed emanating from the micropipe is due to enhanced growth rate at the step edge. Figure 9a presents a threading screw dislocation, while Fig. 9b presents a detail showing the microchannel. Therefore, from the existing evidence the threading screw dislocations may constitute dislocation channels (pipes) to connect the CdTe/Si interfacial region with the depletion region of the electrical junction.

Deleterious impurities from the CdTe/Si interfacial region can follow a pipe to reach the depletion region of the electrical junction in an enhanced diffusion mechanism. An example of SIMS data on state-of-the-art CdTe/ZnTe/Si is shown in Fig. 10. Figure 10a presents the impurity depth profile. In this case the impurity background is lower than the detection limit. Some impurities might be present in the layer but at levels below the detection limit, and/or gettered at interfaces. Impurities could also be hidden by the low spatial resolution of SIMS analysis, or even gettered to various defects existing in the middle of the layer, as are Li and Cu, shown in Fig. 10a. Deleterious impurities present anywhere in the HgCdTe/CdTe-on-Si structure can follow a channel to reach the depletion region. The hypothetical mechanism from this paper considers only impurities diffusing from the interfacial region. An example of a Na impurity, perhaps gettered by other defects and/or particles such as carbon in the interfacial region, was detected by SIMS imaging at another spot of the same sample, as shown in Fig. 10b. The SAM technique detected other impurities in the CdTe/Si interfacial region, such as F, S, and Cu as discussed in Ref. 8.

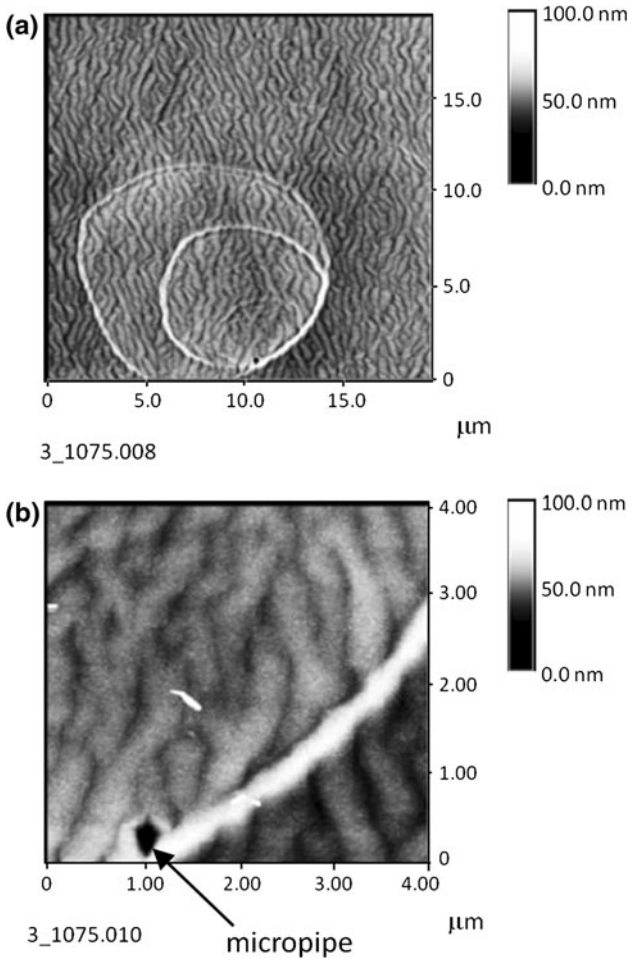

Fig. 9. (a) Atomic force micrographs of an area at the free surface of a HgCdTe/CdTe/Si structure showing the emergence of a screw dislocation at the free surface. Screw dislocation is {111} ⟨110⟩. (b) Detail showing the micropipe.

The nucleation layer, nominally ZnTe, plays a key role in converting the threading dislocations into activated threading dislocations (killer dislocations). ZnTe is chosen for the structure analyzed in this paper, since it has been shown to lock the structure in the (211)B orientation.[11] ZnTe also acts as an efficient barrier for impurity diffusion and for the threading dislocation formation mechanism. While there is no known published data, the SIMS multiple impurity profile (shown in Figs. 10, 11 for HgCdTe-on-Si with a ZnTe nucleation layer) may suggest that ZnTe nucleation serves as an adequate blocking layer. The fact that Li and Na (good decorators in HgCdTe/CdTe)[15] exhibit low impurity levels in Figs. 10 and 11 may support the suggestion that ZnTe acts as a barrier. All the impurities shown in these measurements are below the sample background or below the detection limit. Preliminary data from a SIMS measurement with a high density of points on a thinned sample are shown in Fig. 12. The barrier role of the nucleation layer for the diffusion of Si, in an as-grown sample, is shown in Fig. 12a. However, some problems with the nucleation layer, which might affect the activation of dislocation channels, are observed even in state-of-the-art material. An example is given in Fig. 12b that suggests the presence of Si beyond the interfacial region in an annealed sample. This might be a bulk diffusion process or defect-enhanced diffusion through a nonuniformity in the nucleation layer. More data are needed to confirm these results.

CONCLUSIONS

Discrete species (particles, contamination spots, crystalline defects on Si surface) have been detected in the CdTe/Si interfacial region of HgCdTe/CdTe/Si epitaxial structures. These species getter impurities from the surroundings and thereby constitute discrete impurity diffusion sources.

The similarity in aerial density between these discrete diffusion sources and failed pixels in an LWIR FPA on Si led to a hypothetical physical mechanism to explain the tail distribution in terms of the activation of threading dislocations (killer dislocations).

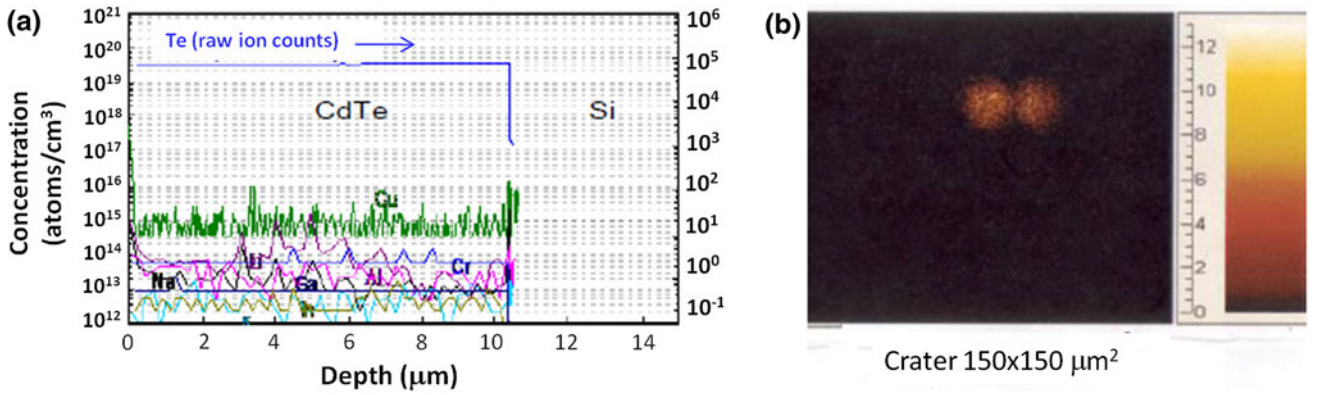

Fig. 10. (a) SIMS depth profile of impurities in the CdTe/ZnTe/Si structure. Te was monitored as a marker to show the layer structure. The impurities shown are below the detection limit. (b) SIMS image of Na at CdTe/Si interfacial region where Na shows the highest concentration (another spot on the same sample).

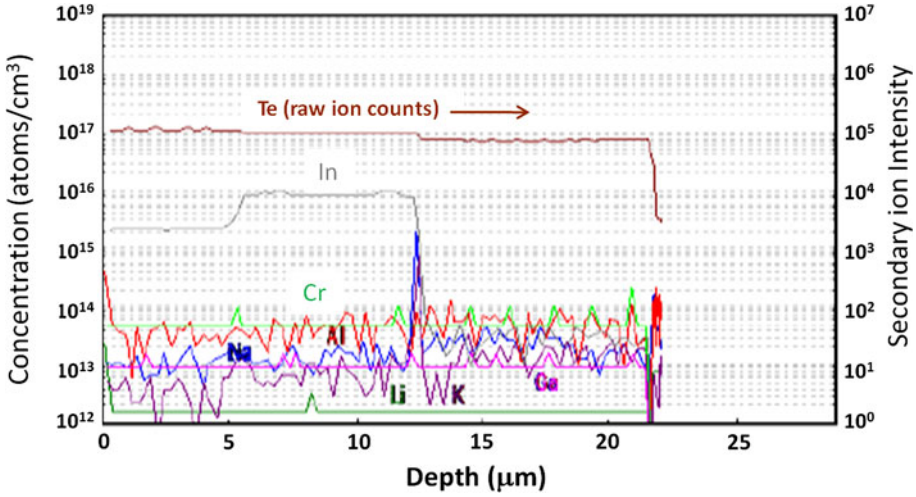

Fig. 11. SIMS depth profile of In and impurities in HgCdTe/CdTe/Si. Te was monitored as a marker to show the layer structure.

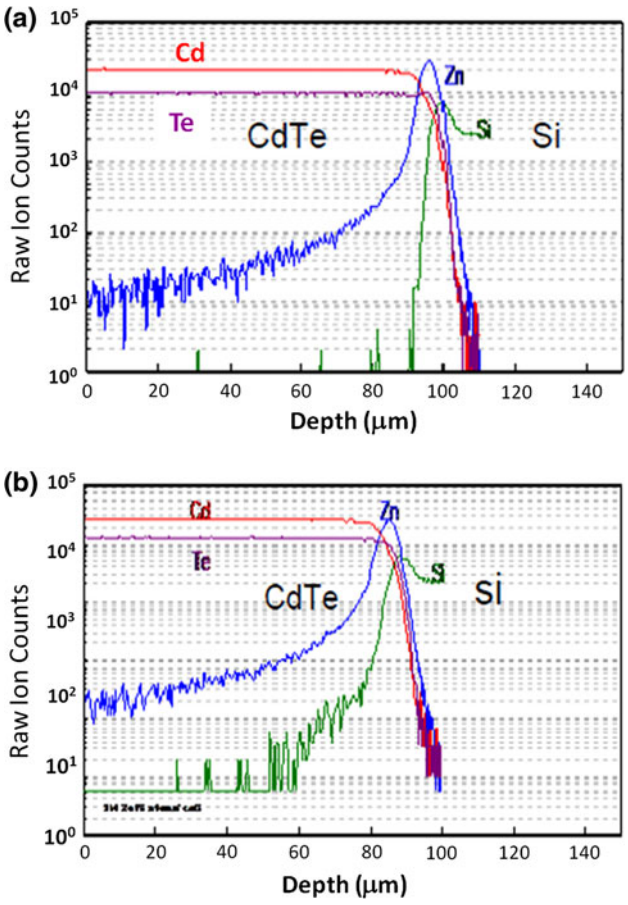

Fig. 12. SIMS profiles with high data point density for CdTe/Si interfacial region study: (a) as grown, and (b) after a high-temperature device anneal.

These killer dislocations allow enhanced diffusion to carry deleterious impurities from the discrete impurity sources in the CdTe/Si interfacial region to the depletion region of the device electrical junction, affecting device performance.

The conversion of a threading dislocation to an activated threading dislocation (killer dislocation) is selective. The selection condition is proximity or coincidence of pipes with discrete impurity sources.

The highest probability for generation of a failed pixel, is the coincidence of threading dislocation clusters with discrete species in the CdTe/Si interfacial region.

The selectivity in conjunction with nucleation layer characteristics lead to a density of failed pixels that is lower than the density of threading dislocations by factors ranging from 100 to 1000.

Further evidence in support of details of the model is presented in the form of preliminary data on HgCdTe/CdTe/Si.

We propose this as an explanation of the observed lack of correlation between EPD and device performance for HgCdTe-on-Si heterostructures.

A prediction of the model would be that reducing the density of the particles and contamination spots and crystalline defects at the surface of (211) Si substrate wafers would lead directly to a reduction in the number of failed pixels in an LWIR HgCdTe FPA. Such a defect and/or particle reduction could be effected by focusing attention on the *ex situ* and *in situ* preparation of the (211) Si substrate.

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