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Interfacial Reaction Effect on Electrical Reliability of Cu Pillar/Sn Bumps

MYEONG-HYEOK JEONG,[1] GI-TAE LIM,[1] BYOUNG-JOON KIM,[2] KI-WOOK LEE,[3] JAE-DONG KIM,[3] YOUNG-CHANG JOO,[2] and YOUNG-BAE PARK[1,4]

1.—School of Materials Science and Engineering, Andong National University, Andong 760-749, Korea. 2.—Department of Materials Science & Engineering, Seoul National University, Seoul 151-744, Korea. 3.—Amkor Technology Korea Inc., Seoul 133-706, Korea. 4.—e-mail: ybpark@andong.ac.kr

Thermal annealing and electromigration (EM) tests were performed with Cu pillar/Sn bumps to understand the growth mechanism of intermetallic compounds (IMCs). Annealing tests were carried out at both 100°C and 150°C. At 150°C, EM tests were performed using a current density of 3.5×10^4 A/cm^2. The electrical failure mechanism of the Cu pillar/Sn bumps was also investigated. Cu_3Sn formed and grew at the Cu pillar/Cu_6Sn_5 interface with increasing annealing and current-stressing times. The growth mechanism of the total (Cu_6Sn_5 + Cu_3Sn) IMC changed when the Sn phase in the Cu pillar/Sn bump was exhausted. The time required for complete consumption of the Sn phase was shorter during the EM test than in the annealing test. Both IMC growth and phase transition from Cu_6Sn_5 to Cu_3Sn had little impact on the electrical resistance of the whole interconnect system during current stressing. Electrical open failure in the Al interconnect near the chip-side Cu pillar edge implies that the Cu pillar/Sn bump has excellent electrical reliability compared with the conventional solder bump.

Key words: Cu pillar/Sn bump, electrical reliability, intermetallic compound, growth kinetics, electromigration

INTRODUCTION

Flip-chip packaging technology assists in the achievement of high performance and miniaturization, because the chip and the substrate are directly connected to flip-chip solder bumps (FCSBs).[1,2] Bump bridging is caused by the shape of the solder in miniaturized electronics. It is limited to applications with fine pitch below 100 μm.[3] As the integration of devices increases, the size of the solder bump becomes smaller with finer pitch. The resulting increase of current density due to miniaturization of the solder bump size with finer pitch causes serious reliability issues. The high current density of FCSBs and the elevated chip temperature relative to the low melting temperature of the solder material can lead to serious electromigration (EM) failure issues.[4] EM is defined as movement of metal atoms in the direction of electron flow due to momentum transfer from conduction electrons to metal atoms. This phenomenon increases with temperature and accelerates when a current is applied. Therefore, a new shape for the bump structure is necessary to address this limitation. Cu pillar bumps are known to be one of the most promising candidate fine-pitch interconnection methods, because they do not cause bump bridging between adjacent bumps and they distribute current uniformly.[5] However, brittle Cu-Sn intermetallic compounds (IMCs) grow and Kirkendall voids form at the joints in Cu pillar bumps because Cu atoms react with Sn atoms in the solder. Additionally, Pb-free solder, due to the

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high concentration of Sn, induces excessive growth of IMCs compared with eutectic Sn-Pb solder. Many researchers have studied IMC formation and growth between Cu and solder, mostly in conventional solder bump structures.[6,7] However, to the best of our knowledge, there have been few systematic studies on the electrical reliability as well as the IMC growth mechanism during current stressing in advanced Cu pillar/thin Sn microbumps. Moreover, under electric current stressing, the growth of IMCs is accelerated by the influence of the electron wind force,[8] which should be systematically investigated. In this work, the IMC growth kinetics in Cu pillar/Sn bumps during both annealing and current-stressing conditions were studied systematically using *in situ* scanning electron microscope (SEM) observations. The electrical failure mechanism and electrical resistance behavior of Cu pillar/Sn bumps were also investigated in detail.

EXPERIMENTAL PROCEDURES

The formation and growth behavior of IMCs due to annealing and EM in Cu pillar/Sn bumps was observed, and the electrical reliability during current stressing was evaluated. The EM test sample structure was designed to facilitate investigation of the EM failure mechanism in Cu pillar/Sn bumps. Overall, the bumps were placed in parallel to distribute the current density, and the center bump was designed to fail by the EM-induced mechanism. Figure 1a shows a schematic diagram of the Cu pillar/Sn bump structure. The pad on the Si chip was sputtered with a 2-μm-thick Al film. An Al line provided the electrical path on the Si chip side. A Cu pillar and pure Sn were formed with a thickness of 40 μm and 3 μm, respectively, on the Al pad, using an electroplating process. The pad on the printed circuit board (PCB) was made using an electroplated 20-μm-thick Cu layer and an electroplated 3-μm-thick pure Sn layer. The thickness and diameter of the Cu pillar/Sn bump were 65 μm and 80 μm, respectively. Pure Sn solders at both the chip and substrate were directly interconnected during the bonding process. The bonding was followed by a reflow process with the peak reflow temperature fixed at 280°C. The bonding time and load were 7 s and 35 N, respectively. Just after bonding, all samples had a similar Sn thickness of 5 μm to 6 μm. The samples were cross-sectioned using sandpaper after the reflow. Figure 1b shows an SEM image of a cross-sectioned Cu pillar/Sn bump. To investigate the interfacial microstructure evolution and IMC growth in Cu pillar/Sn bumps, *in situ* annealing tests were performed via SEM at temperatures of 100°C and 150°C. EM tests to determine the effect of current stressing were performed with a current density of 3.5×10^4 A/cm^2 at 150°C. IMC growth while applying the stressing current density was also observed *in situ*.

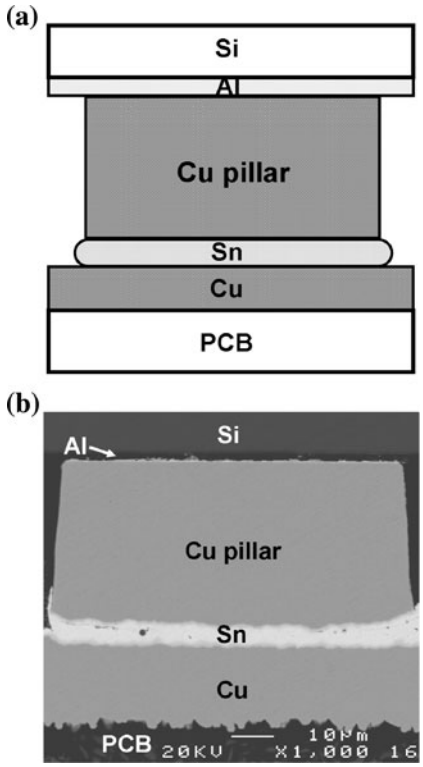

Fig. 1. (a) Schematic diagram and (b) SEM image of Cu pillar/Sn bump structure.

The IMC growth kinetics was investigated by an *in situ* method; that is, the cross-sectioned Cu pillar/Sn bump samples were annealed or current-stressed in an SEM chamber. Similar experimental methods are reported in detail elsewhere.[9–12] The evolution of each interfacial microstructure and the IMC growth in the Cu pillar/Sn bumps was analyzed using SEM in backscattered electron (BSE) mode and using energy-dispersive x-ray spectroscopy (EDS). IMC thickness was measured from the IMC layers at both the chip and substrate sides. The Cu-Sn IMC thickness was quantified using an image analyzer, with the IMC thickness defined as the area of the IMC divided by the interface length.

To investigate the effect of electrical reliability according to resistance increases and the correlation between the interfacial microstructure evolution and the growth of IMCs in the Cu pillar/Sn bump system during current stressing, EM testing was performed with a current density of 3.0×10^4 A/cm^2 at 150°C. Changes in the actual chip temperature, including the applied current-induced Joule heating effect, were monitored in real time by attaching a thermocouple to the top surface of the Si chip inside an oven chamber at a fixed temperature around the specimen. In addition, real-time resistance measurements were applied to understand the interfacial microstructure evolution. To investigate the failure mechanism by EM in Cu pillar/Sn bumps, the fracture interface was analyzed using SEM in BSE mode and using EDS.

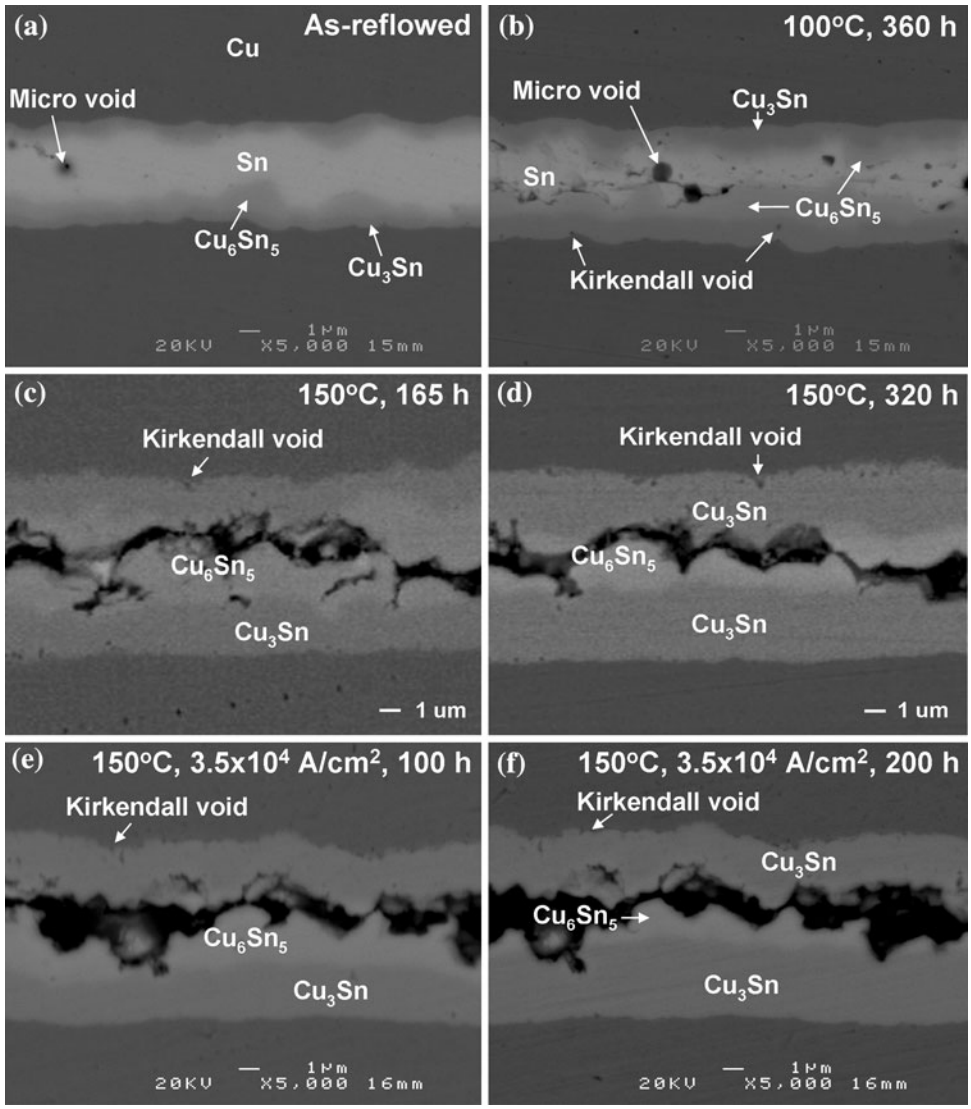

Fig. 2. Enlarged BSE micrographs of the cross-sectioned Cu pillar/Sn interface: (a) as-reflowed, (b) 360 h at 100°C, (c) 165 h at 150°C, (d) 320 h at 150°C, (e) 100 h at 150°C, 3.5 × 10^4 A/cm^2, (f) 200 h at 150°C, 3.5 × 10^4 A/cm^2.

RESULTS AND DISCUSSION

To observe the evolution of the interfacial microstructure and the growth of Cu-Sn IMCs on Cu pillar/Sn bumps with stressing temperature and time, thermal annealing and EM tests were performed at 100°C, 150°C, and 150°C and 3.5 × 10^4 A/cm^2 conditions, respectively. BSE images were taken of cross-sectioned Cu pillar/Sn bumps (Fig. 2). The SEM and EDS results suggested that Cu_6Sn_5 and Cu_3Sn were found at the Cu pillar/Sn interfaces, and that microvoids existed in the Sn phase after reflow. The microvoids seem to originate from the bonding process, also propagated along the original bonding interface. However, the microvoids are an artifact originating not only from process-induced residues but also from surface effects, because our samples were cross-sectioned to perform *in situ* observation in a SEM chamber. After polishing the cross-sectioned samples, bonding interface voids almost disappeared. We also confirmed that the IMC thickness of the half-cut sample was almost identical to that of the polished bump. Similar results are reported elsewhere.[11–13]

Kirkendall voids were observed at the Cu/Cu_3Sn interface as well as within the Cu_3Sn layer. It has been reported that the Kirkendall void formation mechanism can be ascribed to the different diffusivities of Cu and Sn.[6,14] Interestingly, the Kirkendall void density at the substrate side is higher than at the chip side.

The different Cu/Sn electroplating process conditions between the chip side and the PCB side seems to cause this difference in void distribution. At the chip side, successive electroplating of Cu and Sn

layers is performed, while at the substrate side, Cu foil is laminated and then a Sn layer is electroplated after conventional chemical surface treatment. We believe that this difference in process conditions leads to the asymmetry in Kirkendall void density between the chip and substrate sides. Similar results were reported elsewhere.[14–17]

Cu_3Sn formed and grew at the Cu pillar/Cu_6Sn_5 interface with increasing annealing time. It has been reported that the Cu_6Sn_5 and Cu_3Sn phases are generally formed at the Cu/Sn interface during the reaction between Cu and Sn.[6,7,18] Cu_3Sn layers on both interfaces grew to similar thickness. The growth rate of Cu_3Sn in Cu pillar/Sn bumps was also faster than that of Cu_6Sn_5 due to the Sn-limited nature of the Cu-Sn reaction system,[11,19] while in a conventional solder bump the Cu-Sn reaction system is Cu limited. The Sn phase was not observed at the Cu pillar/Sn interface after 165 h at 150°C or after 100 h at 150°C, 3.5×10^4 A/cm^2; on the other hand, the Sn phase was still observed at the Cu pillar/Sn interface after 360 h at 100°C. It appears that higher annealing temperatures and current stressing both accelerate the reaction between Cu and Sn. During current stressing, the electron wind force seems to enhance the IMC formation reaction between Cu and Sn.[19,20] The microvoids, which appeared in the Sn phase after reflow, also propagated along the void, because the Cu-Sn IMC formation constricted the volume.

Figure 3 shows the dependence of the growth mechanism of the total (Cu_6Sn_5 + Cu_3Sn) IMC as a function of annealing and current-stressing time. Figure 3a and b shows the thickness of the total IMC as a function of the square root of annealing time at 100°C and 150°C, respectively. The growth of the total IMC followed a linear relationship with the square root of the annealing time and was faster at higher annealing temperatures.[11] This implies that the growth of the total IMC was controlled by a diffusion mechanism. Figure 3c shows the IMC growth behavior versus current-stressing time. It is noticeable that the total IMC thickness increases linearly with current-stressing time. This is closely related to the different reaction mechanism of EM compared with those of annealing.[8,19,21] Competition between diffusion inside IMCs and chemical reaction at the Cu/Sn interface seems to exist. It has been reported that the IMC thickness in conventional solder bumps under current-stressing conditions is linearly proportional to stressing time,[6,8] which means that the growth of the total IMC is controlled by a reaction mechanism. The IMC growth of the Cu_6Sn_5 and Cu_3Sn phases at 100°C followed linear relationships with the square root of annealing time until 360 h. However, the Cu_6Sn_5 and Cu_3Sn phases linearly increased together before 165 h at 150°C, and then the Cu_6Sn_5 phase rapidly decreased after 165 h at 150°C. During current stressing, the growth slopes of the Cu_6Sn_5 and Cu_3Sn IMCs were altered in a similar way after

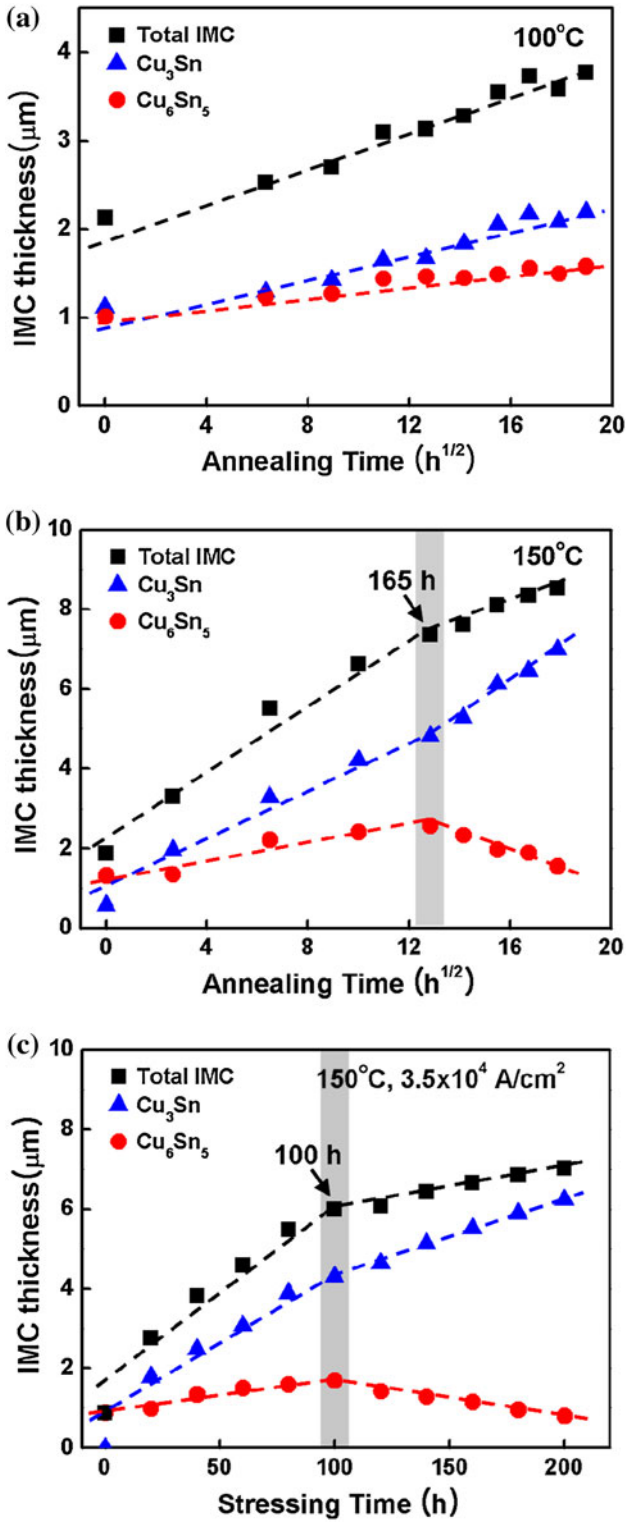

Fig. 3. Thickness variations of each IMC phase with annealing and current-stressing times and temperatures at (a) 100°C, (b) 150°C, and (c) 150°C, 3.5×10^4 A/cm^2.

100 h at 150°C, 3.5×10^4 A/cm^2. Enlarged BSE images of the Cu pillar/Sn bump interface when the Cu_6Sn_5 phases rapidly decreased are shown in

Fig. 2. The Sn phase remained at the Cu pillar/Sn bump interface until 360 h at 100°C, as shown in Fig. 2b. However, the Sn phase was not observed at the Cu pillar/Sn bump interface after 165 h at 150°C and after 100 h at 150°C, 3.5×10^4 A/cm^2, in contrast with the microstructure just after reflow, as shown in Fig. 2c and e. Thus, the decrease in the Cu_6Sn_5 phase results from complete consumption of the Sn phase in the Cu pillar/Sn bumps. The Cu_6Sn_5 phase transforms to the Cu_3Sn phase, because the Cu_6Sn_5 phase reacts with the Cu atoms that are constantly supplied from the Cu pillar, as shown in Eq. 1:

$$Cu_6Sn_5 + 9Cu \rightarrow 5Cu_3Sn. \quad (1)$$

Therefore, the transition times for the Cu_6Sn_5 phase to transform into the Cu_3Sn phase are related to the complete consumption of the Sn phase in the Cu pillar/Sn bumps. The transition time for current stressing at 150°C, 3.5×10^4 A/cm^2 was faster than with annealing alone at 150°C. Under electric current stressing, the growth of IMCs is accelerated by the influence of the electron wind force,[8,19–21] and the transition time became shorter as IMC growth rates increased.[19]

When the specimen undergoes constant current stressing over time, the joints of the FCSBs become a reliability issue due to EM.[9] This damage by EM increases the electrical resistance of the overall Cu pillar/Sn bump system. Therefore, comparing the measured resistance with the microstructure of the specimen can provide information on the electrical failure mechanism. To investigate the effect of electrical reliability according to resistance increases and the correlation between the interfacial microstructure evolution and growth of IMCs in the Cu pillar/Sn bump system during current stressing, Fig. 4 shows typical curves of the change in relative resistance as a function of EM testing time. To characterize the Joule heating under accelerated test conditions, real-time changes in flip-chip package temperature were monitored by attaching a thermocouple to the top surface of the Si chip. Differences between the chip temperature and the ambient oven temperature were measured for current densities of 3.0×10^4 A/cm^2 at a constant oven temperature of 150°C. Joule heating was characterized as 60°C, 75°C, 85°C, and 90°C for resistance increases of 0%, 10%, 20%, and 40%, respectively. The dashed line in the graph represents the failure criterion, defined as a 20% increase in resistance. It is evident that elevated temperatures lead to shorter failure times. Even though sample-to-sample variations are apparent, there seems to be a common resistance–time relationship.[9] Cu pillar/Sn bumps were current-stressed for longer than 560 h before a 20% increase in resistance was reached. Measured resistance changes were correlated with the interfacial microstructure evolution observed during current stressing.

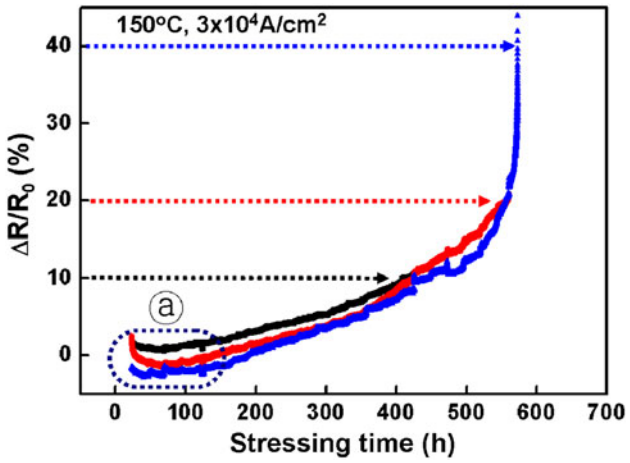

Fig. 4. Resistance increase with stressing time at 150°C, 3×10^4 A/cm^2.

Figure 5 shows the interfacial microstructure during current stressing from the initial reflow of the specimens until 150 h afterward (cf. interval marked "ⓐ" in Fig. 4). Little resistance change occurs due to the formation of IMCs in the Cu pillar/Sn bump, nor does a change occur due to conversion of Cu_6Sn_5 to Cu_3Sn. According to a report by Tanida et al.,[22] no significant difference was confirmed between bonding conditions, and the IMC state has little effect on the resistance of a Cu bump interconnection. As shown in Table I, Cu-Sn IMCs have high resistivity values.[23] However, the IMC layer in the entire daisy-chain interconnect system occupies a very small volume fraction. Therefore, even the phase change of the IMC has little impact on the resistance change of the solder joints.

Figure 6a and b shows the bump microstructure observed for resistance increases of 10% and 20%, respectively. As the resistance increased from 10% to 20%, the Cu_3Sn phase generated in the solder joint thickened. As the resistance increased from 10% to 20%, a notable microstructure change in the Cu pillar/Sn bump was not observed.

As the resistance increased, the Al line of the specimen was observed by SEM in secondary-electron mode (Fig. 7). After a 10% increase in resistance of the specimen, little difference in the features of the Al line was observed. However, when the resistance increased by 20%, accumulation of Al atoms around the location where electrons enter the bumps from the Al lines was observed. As the resistance increased to 40% above the initial value, the atoms were shown to accumulate even more dramatically, as shown in Fig. 7d. The Al line, after a 40% increase in resistance, was about twice as thick as the original line due to this accumulation phenomenon, thought to be caused by EM. The depletion of atoms on the other side of the Al line indicates that the line has been disconnected.[24–26] In Fig. 7c, the atom accumulation region is marked

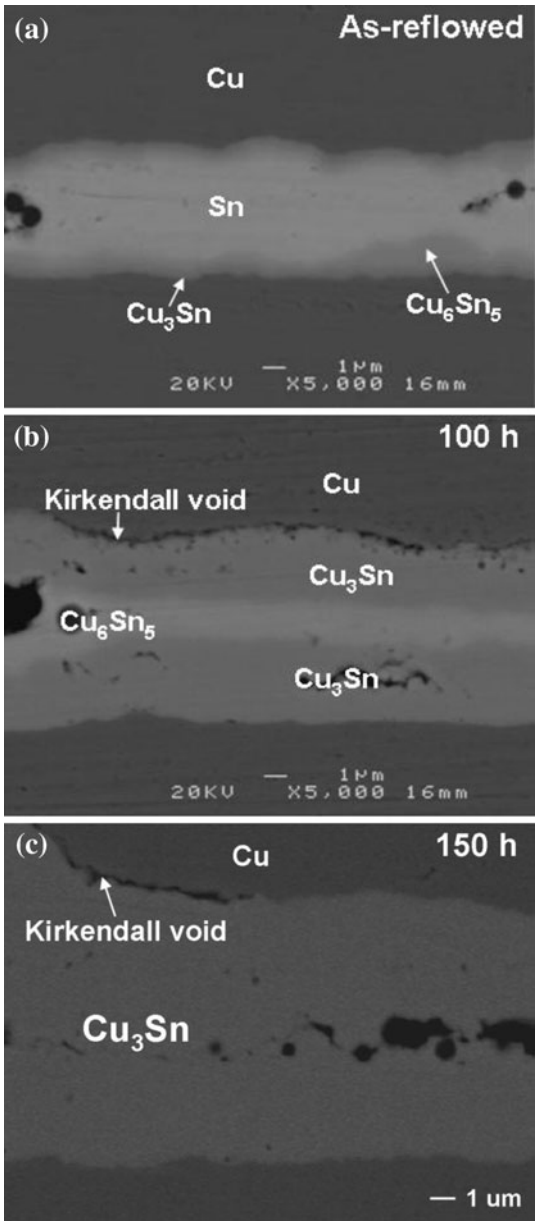

Fig. 5. Enlarged BSE micrographs of the cross-sectioned Cu pillar/Sn interface at 150°C, 3×10^4 A/cm^2: (a) as reflowed, (b) 100 h, and (c) 150 h.

Table I. Electrical resistivity of Cu-Sn systems[23]

Electrical Resistivity (10^{-8} Ω m) at RT			
Cu	**Cu_3Sn**	**Cu_6Sn_5**	**Sn**
1.73	8.93	17.5	10.1

"ⓐ," and the other side marked "ⓑ" is assumed to be the depleted region. The cathode bump current density in the Al line was about 2.0×10^5 A/cm^2, which looks like a high value; however, in the Cu pillar/Sn bump, where EM can occur, the maximum current density was relatively low, about 5.0×10^4 A/cm^2. Because the Cu pillar was sufficiently thick, current crowding in the Al line was alleviated.[27,28] In fact, failure of solder joints by EM at current densities of approximately 1.0×10^5 A/cm^2 has been reported to occur frequently.[28,29] The excellent EM characteristics of Cu pillar/Sn bumps can be compared with the characteristics of solder joints with a diameter similar to the pad. According to the reports by Lee et al.[2,9,10] where Sn-Ag solder joints with diameters of 100 μm were formed on the Cu under bump metallization (UBM), the mean time to failure of those devices was about 30 h to 150 h. In contrast, 600 h passed before EM failure occurred in the Cu pillar/Sn bump structure. Therefore, compared with conventional solder bumps, the Cu pillar/Sn bump structure has excellent electrical reliability.

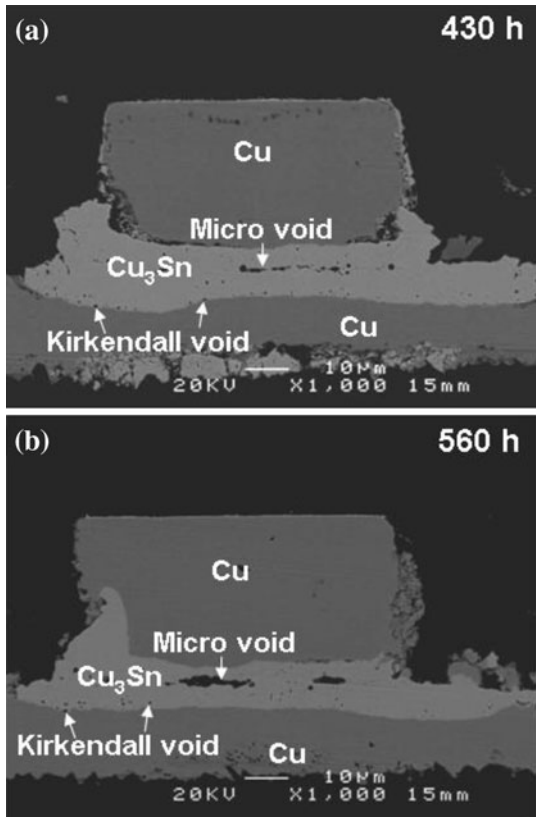

Fig. 6. Micrographs of the bump at different $\Delta R(\Omega)$ ratios: (a) 10% increase (430 h), and (b) 20% increase (560 h).

CONCLUSIONS

The growth behavior of IMCs in Cu pillar/Sn bumps under both annealing and current-stressing conditions was systematically investigated using *in situ* SEM observations. The total (Cu_6Sn_5 + Cu_3Sn) IMC thickness increased linearly with the square root of annealing time, but increased linearly with current-stressing time, which means that

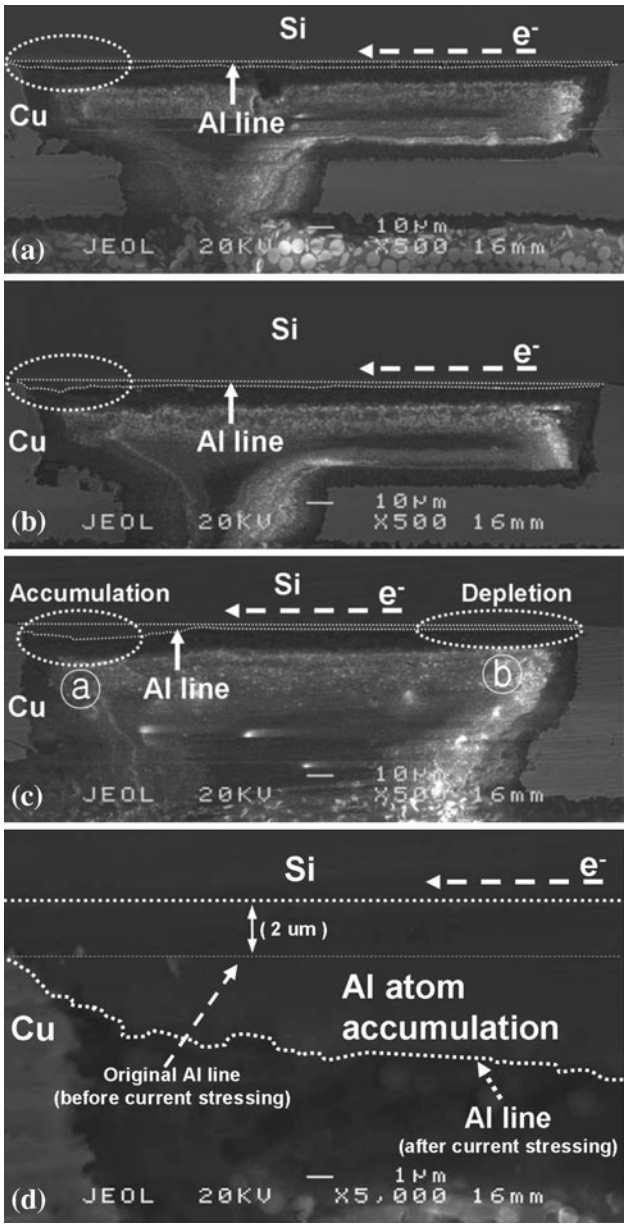

Fig. 7. SE image of Al line with varying $\Delta R(\Omega)$ ratio: (a) 10%, (b) 20%, (c) 40%, and (d) enlarged micrograph of 40% resistance increase.

current stressing, rather than pure annealing, accelerated the interfacial reaction. A change in the IMC growth slopes is closely related to the phase transition from Cu_6Sn_5 to Cu_3Sn phases after complete consumption of the remaining Sn phase due to the limiting amount of Sn phase in the Cu pillar/Sn bump. The characteristic IMC growth mechanism showed little effect on the resistance change in our daisy-chain structure. EM-induced Al line depletion near the Cu pillar edge of the chip side led to electrical failure of the Cu pillar/Sn bump, which suggests that Cu pillar/Sn bumps have better electrical reliability than conventional solder bumps.

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