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# Metalorganic Chemical Vapor Deposition of CdTe(133) Epilayers on Si(211) Substrates

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Single-crystalline CdTe(133) films have been grown by metalorganic chemical vapor deposition on Si(211) substrates. We studied the effect of various growth parameters on the surface morphology and structural quality of CdTe films. Proper oxide removal from the Si substrate is considered to be the principal factor that influences both the morphology and epitaxial quality of the CdTe films. In order to obtain single-crystalline CdTe(133) films, a two-stage growth method was used, i.e., a low-temperature buffer layer step and a high-temperature growth step. Even when the low-temperature buffer layer shows polycrystalline structure, the overgrown layer shows single-crystalline structure. During the subsequent high-temperature growth, two-dimensional crystallites grow faster than other, randomly distributed crystallites in the buffer layer. This is because the capturing of adatoms by steps occurs more easily due to increased adatom mobility. From the viewpoint of crystallographic orientation, it is assumed that the surface structure of Si(211) consists of (111) terrace and (100) step planes with an interplanar angle of 54.8°. This surface structure may provide many preferable nucleation sites for adatoms compared with nominally flat Si(100) or (111) surfaces. The surface morphology of the resulting films shows macroscopic rectangular-shaped terrace—step structures that are considered to be a (111) terrace with two {112} step planes directed toward ⟨110⟩.

**Key words:** Thin film, MOCVD, CdTe/Si, buffer layer, thermal cleaning

## INTRODUCTION

Cadmium telluride (CdTe) is one of the most promising materials for both solar cells and x-ray detectors. Also, its close lattice match and chemical compatibility with mercury cadmium telluride (HgCdTe) make CdTe an ideal substrate for growth of infrared detector material.[1,2] The growth of thick epitaxial layers on large-area substrates such as gallium arsenide (GaAs) or silicon (Si) is a promising route for fabrication of large-area imaging detectors.[3–5] In particular, epitaxial CdTe films on large-area Si substrates offer many well-known advantages, including greater availability of larger sizes at low cost and compatibility that enables integration of focal-plane arrays with Si-based readout electronics. However, their large lattice mismatch, thermal expansion coefficient difference, and the bond valence mismatch impose obstacles to successful growth of epitaxial layers with high crystalline quality.

Several growth techniques, including hot-wall epitaxy,[6,7] metalorganic chemical vapor deposition (MOCVD),[8–10] and molecular-beam epitaxy (MBE),[11,12] have been investigated for growth of epitaxial layers of CdTe on Si substrates. Researchers at the University of Illinois in Chicago have pioneered

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many developments in direct epitaxial growth of CdTe on Si substrates using the MBE technique.[11,12] To obtain epitaxial CdTe films on Si substrates, they used a thermal cleaning method for removal of residual oxides on a chemically cleaned Si substrate. This surface cleaning step is considered to be a decisive factor for achieving high-quality CdTe films on Si.

However, research on MOCVD growth of CdTe on Si has rarely been pursued due to the difficulty of employing proper surface cleaning techniques for Si substrates with conventional MOCVD systems. This is because conventional MOCVD systems are not equipped with an ultrahigh-vacuum (UHV) chamber nor a high-temperature heater with the ability to heat to 900°C.[13] However, Wang and Bhat[10] demonstrated a novel method with an *in situ* Si cleaning step which does not require a high-temperature deoxidation process to grow high-quality CdTe and ZnTe on Si in a single MOCVD reactor.

In this work, we have studied direct growth of CdTe layers on Si substrates in a MOCVD system. One problem with epitaxial growth of CdTe with conventional MOCVD systems is the difficulty of removal of silicon dioxide layers from the Si surface. To resolve this problem, we used Si substrates which had been thermally cleaned in an UHV chamber, followed by arsenic passivation. We will discuss the orientation dependence of CdTe layers grown by MOCVD and their characteristic growth mechanism.

## EXPERIMENTAL PROCEDURES

CdTe films were grown in a horizontal MOCVD reactor at atmospheric pressure under conditions that minimized the gas-phase reactions of cracked Cd with Te precursor by increasing the gas velocity in the reactor above 6 cm/s. Hydrogen was used as the carrier gas. The total gas flow rate through the reactor was 7 slm. Details of the MOCVD system have been described in previous research.[14] Dimethylcadmium (DmCd), and di-iso-propyltelluride (DiPTe) provided by SAFC Hitech were used as precursors for Cd and Te, respectively. The substrate was rotated during the deposition process to improve uniformity of the CdTe film. The precursor ratio into the reactor (DmCd partial pressure/DiPTe partial pressure) was maintained at 1, and the Si substrates used were (211) oriented. The Si substrates were cleaned with solvent, dipped in concentrated HF for 15 s, and rinsed with deionized water before being placed into the UHV chamber for thermal cleaning. Complete deoxidation of the substrate, as confirmed by the observed twofold reflection high-energy electron diffraction pattern, was achieved when the substrate was heated for 20 min at ~840°C, as determined by pyrometric measurement. During the subsequent removal of surface oxides, the background pressure of the chamber was less than $5.0 \times 10^{-9}$ Torr. For the As-coated sample, the substrate temperature was decreased to room temperature with an $As_2$ beam pressure of $3.0 \times 10^{-6}$ Torr for 40 min.

Growth of CdTe films was carried out in two stages: the first stage at 300°C and the second stage at a temperature higher than 400°C, as measured by a K-type thermocouple placed in the graphite susceptor. The first growth stage was carried out for 20 min with a low growth rate of less than 1 $\mu$m/h. In the second growth stage, the growth rate was increased to 5 $\mu$m/h. The crystalline quality of the films was analyzed by x-ray diffraction (XRD) using a Cu $K_\alpha$ source (D8, 60 kW; Bruker). The surface morphology and crystal structure of CdTe films were characterized by Nomarski optical microscopy (BH2-UMA; Olympus) and transmission electron microscopy (TEM; FEI, Tecnai F30 S-Twin), respectively.

## RESULTS AND DISCUSSION

Growth of CdTe films on Si substrates was attempted under a wide range of growth conditions. MOCVD of CdTe layers performed with Si substrates which had not undergone the thermal cleaning process resulted in polycrystalline layers with very poor substrate adhesion. It is thought that this result is mainly due to the thin oxide layer on the substrate surface. If a Si substrate is loaded quickly into a MOCVD reactor after chemical etching, the presence of a submonolayer oxide cannot be ruled out because of variations in the processing conditions. The resulting CdTe surface did not change when we added the low-temperature buffer layer onto these substrates.

Thermal cleaning and arsenic passivation of the Si surface were found to be important factors for obtaining single-crystalline CdTe films by MOCVD. Also, the buffer layer growth of CdTe at low temperature (~300°C) was necessary for smooth surface morphology. In this work, thermal cleaning of the Si substrate and As passivation were carried out sequentially in the UHV chamber. Afterward, the substrates were vacuum-packed and preserved to retain an oxide-free surface and then transported to the MOCVD reactor. It is thought that the As passivation plays a major role in protecting the heat-cleaned Si surface. All of the following results were obtained using arsenic-passivated Si(211) substrates.

The typical surface morphology of the CdTe buffer layer on Si(211), which was grown at 300°C and has a thickness of 200 nm, and its XRD pattern are shown in Fig. 1. The XRD pattern indicates that the CdTe layer is polycrystalline with preferred growth orientation of [331]. These results can be explained by three-dimensional nucleation at the initial growth stage. Although the Si(211) surface provides a periodic step array where nucleation can be initiated favorably, the limited lateral mobility due to the low deposition temperature prevents adatoms from moving to stable sites on the substrate surface. Therefore, nucleation occurs two-dimensionally at

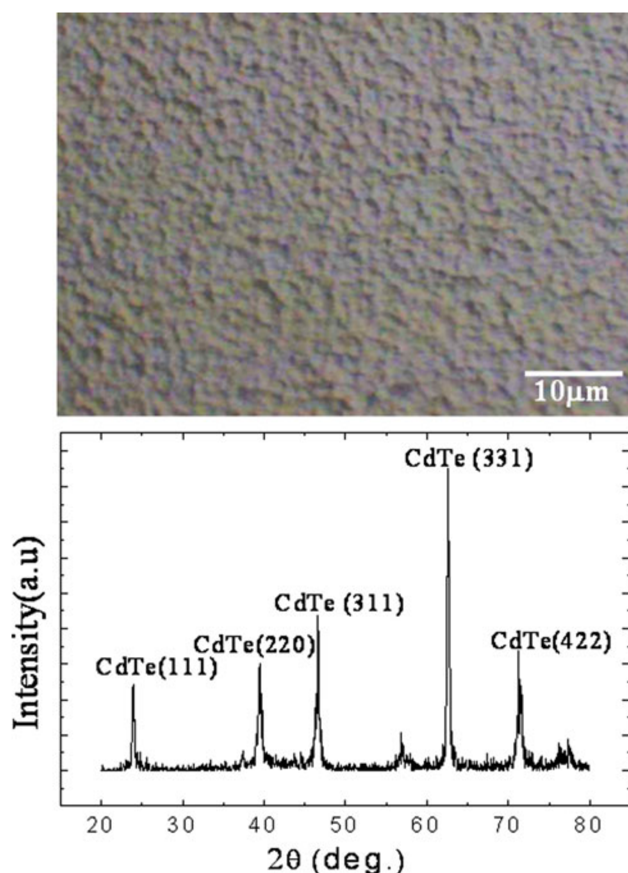


Fig. 1. Optical Nomarski image of a 200-nm-thick CdTe buffer layer on a Si(211) substrate, which was grown at 300°C, and its XRD pattern.

the step edge as well as three-dimensionally in the close vicinity of the incident site. This would result in polycrystalline structure of the film.

The surface morphology changes with the addition of the second stage at a different growth temperature. Figure 2 shows the surface morphology of CdTe layers grown under different temperatures and their XRD patterns. When the growth temperature was less than 450°C, the layers tended to be polycrystalline. The intensity of the CdTe(133) peak increased with increasing growth temperature. It is noteworthy that no peaks other than that of CdTe(133) were observed when the growth temperature was 500°C, indicating a single-crystalline layer. Also the surfaces consist of a regular array of crystallographic terrace and step structures which is parallel to the [110] axis.

The low-temperature CdTe buffer layer has been shown to directly affect the surface morphology and crystalline structure of subsequently grown CdTe films. The effect of buffer layer thickness on surface morphology is shown in Fig. 3. The buffer layer was grown at 300°C for different times, and the growth conditions of the second stage were 500°C for 1 h. The surface images become coarse when the buffer layer thickness is thicker than 1 $\mu$m. Our results show that the optimum thickness for the low-temperature buffer layer is about 200 nm to 400 nm. The critical thickness of CdTe on Si had been calculated to be less than 1 nm, providing 19% lattice mismatch between CdTe and Si.[15] The conventional lattice-matching and accommodation mechanism based on critical thickness cannot be applied to our results because our low-temperature buffer layer does not have a single-crystalline structure. A high-resolution TEM image of the CdTe in the buffer layer region is shown in Fig. 4. The buffer layer results in randomly distributed, fine CdTe domains without extended defects in the region near the Si substrate, as indicated by the circle in Fig. 4. Interestingly, a

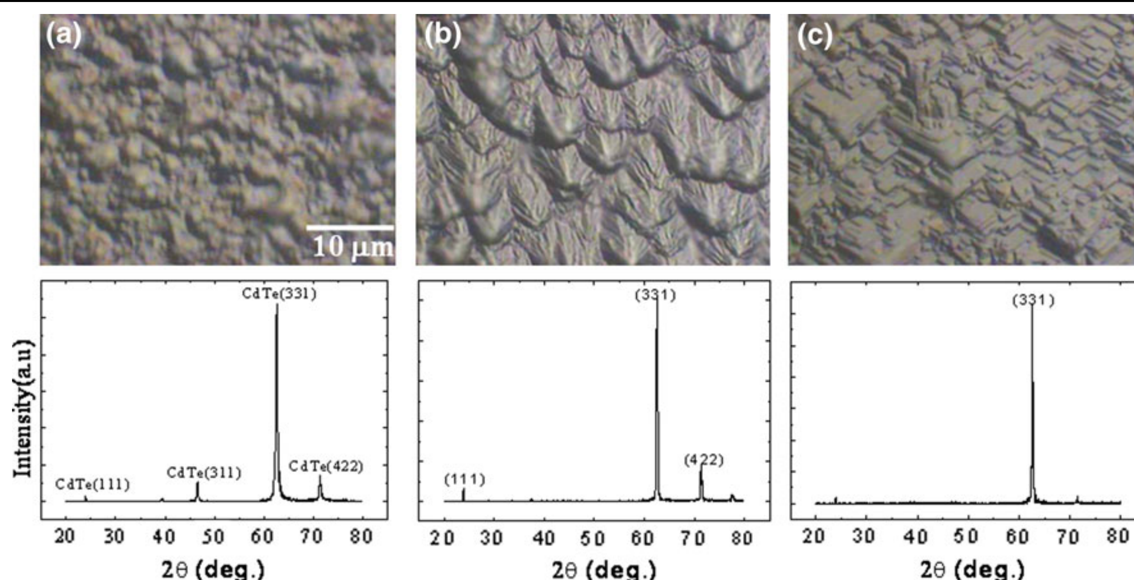


Fig. 2. Surface morphology of CdTe/Si(211), and corresponding XRD patterns, grown under various CdTe deposition temperatures: (a) 360°C, (b) 450°C, and (c) 500°C. In all samples, low-temperature buffer layer thicknesses are 300 nm and total layer thicknesses are 1.2 $\mu$m.

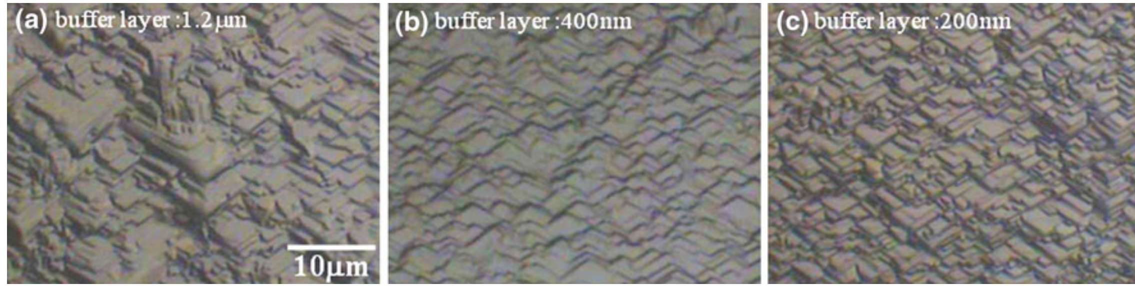


Fig. 3. Surface morphology of CdTe grown on various buffer layer thicknesses. In all samples, the buffer layer was grown at 300°C, for (a) 3 h, (b) 1 h, or (c) 30 min. The second stage of growth was performed at 500°C for 1 h. Total layer thicknesses were 5.0 $\mu$m, 4.2 $\mu$m, and 4.0 $\mu$m, respectively.

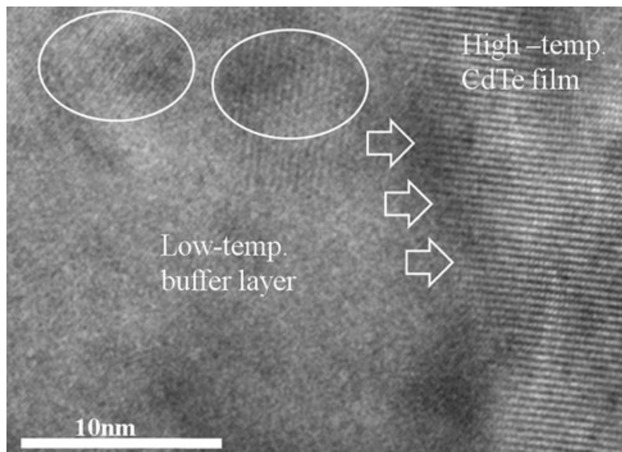


Fig. 4. High-resolution TEM image showing randomly distributed polycrystalline structure of buffer layer and overgrown single crystal.

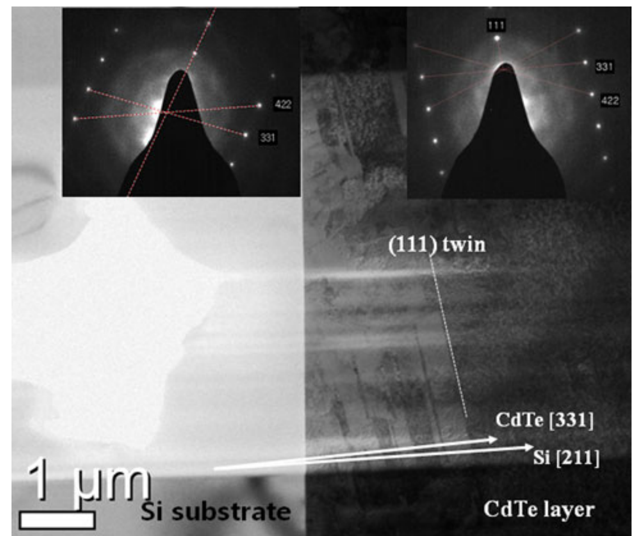


Fig. 5. Cross-sectional TEM image of Si/CdTe interface and electron diffraction patterns.

CdTe layer, subsequently grown at 500°C, exhibited single-crystalline structure.

Figure 5 shows a cross-sectional high-resolution TEM image of the CdTe/Si interface. Although the buffer layers had been grown in expectation of 1.2 $\mu$m thickness, the interface between the buffer layer and overgrown CdTe layer was not clear. The low-temperature CdTe buffer layer had a high density of lamellar twins. It is reported that [255] is the exact twin of [211], with [111] as the mirror plane.[16] At the initial growth stage, it is speculated that nucleation was initiated with the CdTe[211] direction, the same as the Si substrate orientation. The subsequent growth induces CdTe(255), with [111] as the mirror plane. The insets to Fig. 5 show electron diffraction patterns of the CdTe layer and the Si(211) substrates. From Fig. 5, the CdTe(133) pattern was found to be tilted away from Si(211) by 2.5°, as indicated by the white arrow. This tilt is assumed to be the interplanar angle between (133) and (255), which is calculated to be 2.5°.

The Si(211) surface consists of a periodic array of (111) terrace planes and (100) step planes. At the buffer layer growth temperature, nucleation is assumed to be initiated at two different sites: the step edge site and the terrace site. If the surface diffusion length of incident atoms could be increased by increasing the deposition temperature or decreasing the growth rate, adatoms would have a better chance of arranging favorably at the step site. Under this growth condition, three-dimensionally nucleated islands on the terrace surface would have a random orientation and two-dimensionally nucleated crystallites on the step edge would have the same crystallographic orientation as the substrate. Our buffer layer results in polycrystalline growth with CdTe(133) preferred, as confirmed by the XRD pattern and TEM image. As growth proceeds, CdTe(211) crystallites will preferentially develop from larger-sized grains, and twins may nucleate and propagate inside these domains to accommodate strain induced by lattice mismatch or polarity. This will probably result in preferable CdTe(133) plane. The CdTe buffer layer surface might consist of a large portion of (133) plane and other random crystallites, even if the layer thickness is greater than 1 $\mu$m. During the subsequent high-temperature growth, the two-dimensional crystallites grow faster

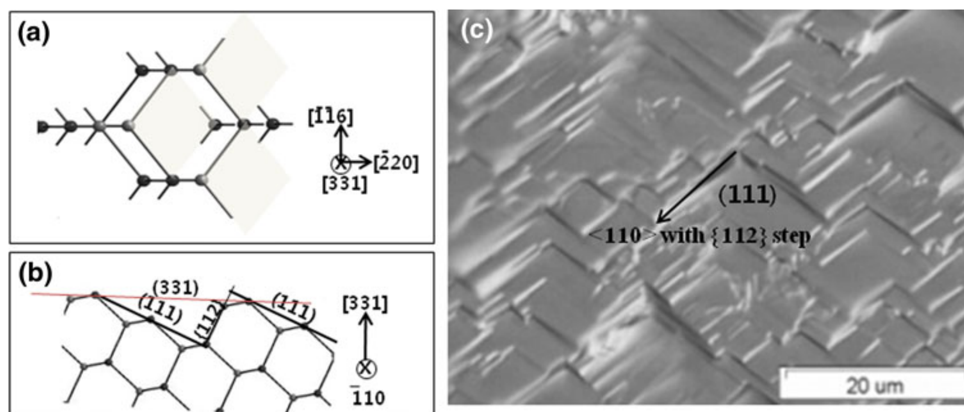


Fig. 6. Atomic arrangement (top view) of: (a) the CdTe(133) surface, and (b) [110] projection of the CdTe(133) plane; (c) optical Nomarski image of CdTe(133) on Si(211).

than the other, randomly distributed crystallites because capturing of adatoms by steps occurs more easily due to increased adatom mobility. This is why the single-crystalline CdTe(133) layer can be overgrown on the polycrystalline CdTe buffer layer.

Rujirawat et al.[12] have reported homo-orientation of CdTe(211) on Si(211) substrates using the MBE technique with a thin ZnTe(211)B buffer layer. Niraula et al.[4] have succeeded in obtaining homo-orientation of CdTe(211) on Si(211) using MOCVD techniques with special pretreatment of the substrates. It is speculated that, in their substrate pretreatment step, a thin buffer layer such as GaAs may be formed and play a crucial role in obtaining homo-orientation of CdTe. It is thought that direct growth of CdTe on Si without heterobuffer layers does not result in homo-orientation of the Si substrate.

Figure 6 illustrates top views of the atomic arrangement of: the CdTe(133) surface (a) and the [110] projection of the CdTe(133) plane (b), and an optical Nomarski image of CdTe(133) on Si(211). The atomic arrangement of CdTe(133) consists of rectangular-shape (111) terrace planes with two step planes of {211} directed toward ⟨110⟩, as indicated in Fig. 6c. The surface morphology of our film is thought to be the result of the step-bunching process during the high-temperature growth. This means that step-flow growth mode occurred during the high-temperature growth stage.

## CONCLUSIONS

We studied the properties of CdTe layers grown on Si substrates by MOCVD from the viewpoint of crystal structure and surface morphology. Proper oxide removal from the Si substrate is likely to be a principal factor that influences both morphology and epitaxial quality of CdTe films grown by MOCVD. Generally, depositions performed with native oxide present on the Si surface produce polycrystalline CdTe films for all substrate temperatures and growth rates. Thermal cleaning in a UHV chamber and As passivation of the Si surface are required for growth of single-crystalline CdTe using a two-stage growth method, which includes a low-temperature buffer layer step and a high-temperature growth step. We explain the CdTe(133) plane formation mechanism on the Si(211) surface based on the crystallographic orientation. The regular array of rectangular-shaped terrace—step structures of the CdTe(133) surface is attributed to the step-bunching process during the high-temperature growth stage.

## REFERENCES

1. T.C. Antony, A.L. Faheubruch, M.G. Peters, and R.H. Bube, *J. Appl. Phys.* 57, 400 (1985).
2. V.P. Singh, O.M. Erickson, and J.H. Chao, *J. Appl. Phys.* 78, 4538 (1995).
3. M.C. Chen and M.J. Bevan, *J. Appl. Phys.* 78, 4787 (1995).
4. M. Niraula, K. Yasuda, K. Takagi, H. Kusama, M. Tominaga, Y. Yamamoto, Y. Agata, and K. Suzuki, *J. Electron. Mater.* 34, 815 (2005).
5. K. Yasuda, M. Niraula, H. Kusama, Y. Yamamoto, M. Tominaga, K. Takagi, Y. Agata, and K. Suzuki, *IEEE Trans. Nucl. Sci.* 52, 1951 (2005).
6. H. Tatsuoka, H. Kuwabara, Y. Nakanishi, and H. Fujiyasu, *J. Cryst. Growth* 129, 686 (1993).
7. S. Seto, S. Yamada, and K. Suzuki, *J. Cryst. Growth* 214–215, 5 (2000).
8. H. Ebe and Y. Nishijima, *Appl. Phys. Lett.* 67, 3138 (1995).
9. K. Yasuda, H. Hatano, M. Minamide, T. Maejima, and K. Kawamoto, *J. Cryst. Growth* 166, 612 (1996).
10. W.-S. Wang and I. Bhat, *J. Electron. Mater.* 24, 451 (1955).
11. L.A. Almeida, Y.P. Chen, J.P. Faurie, S. Sivananthan, D.J. Smith, and S.-C.Y. Tsen, *J. Electron. Mater.* 25, 1402 (1996).
12. S. Rujirawat, L.A. Almeida, Y.P. Chen, S. Sivananthan, and D.J. Smith, *Appl. Phys. Lett.* 71, 1810 (1997).
13. K. Shigenaka, K. Matsushita, L. Sugiura, F. Nakata, and K. Hirahara, *J. Electron. Mater.* 25, 1347 (1996).
14. S.-H. Suh, J.-S. Kim, H.J. Kim, and J.-H. Song, *J. Cryst. Growth* 236, 119 (2002).
15. R. People and J.C. Bean, *Appl. Phys. Lett.* 47, 322 (1985).
16. S. Rujirawat, D.J. Smith, J.P. Faurie, G. Neu, V. Nathan, and S. Sivananthan, *J. Electron. Mater.* 27, 1047 (1998).