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Dislocation Reduction of HgCdTe/Si Through *Ex Situ* Annealing

G. BRILL,[1,5] S. FARRELL,[2] Y.P. CHEN,[1] P.S. WIJEWARNASURIYA,[1] MULPURI V. RAO,[2] J.D. BENSON,[3] and N. DHAR[1,4]

1.—U.S. Army Research Laboratory, Sensors and Electronic Devices Directorate, 2800 Powder Mill Road, Adelphi, MD 20783, USA. 2.—Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030, USA. 3.—U.S. Army RDECOM, CERDEC Night Vision and Electronic Sensors Directorate, Ft. Belvoir, VA 22060, USA. 4.—DARPA, MTO Office, Arlington, VA 22203, USA. 5.—e-mail: gbrill@arl.army.mil

Current growth methods of HgCdTe/Cd(Se)Te/Si by molecular-beam epitaxy (MBE) result in a dislocation density of mid 10^6 cm^{-2} to low 10^7 cm^{-2}. Although the exact mechanism is unknown, it is well accepted that this high level of dislocation density leads to poorer long-wavelength infrared (LWIR) focal-plane array (FPA) performance, especially in terms of operability. We have conducted a detailed study of *ex situ* cycle annealing of HgCdTe/Cd(Se)Te/Si material in order to reduce the total number of dislocations present in as-grown material. We have successfully and consistently shown a reduction of one half to one full order of magnitude in the number of dislocations as counted by etch pit density (EPD) methods. Additionally, we have observed a corresponding decrease in x-ray full-width at half-maximum (FWHM) of *ex situ* annealed HgCdTe/Si layers. Among all parameters studied, the total number of annealing cycles seems to have the greatest impact on dislocation reduction. Currently, we have obtained numerous HgCdTe/Si layers which have EPD values measuring $\sim 1 \times 10^6$ cm^{-2} after completion of thermal cycle annealing. Preliminary Hall measurements indicate that electrical characteristics of the material can be maintained.

Key words: Mercury, cadmium, telluride, HgCdTe, thermal cycle annealing, (112), etch pit density (EPD), dislocations, MBE, silicon, Si, composite substrates

INTRODUCTION

HgCdTe-on-Si material grown by molecular-beam epitaxy has been demonstrated as a viable technology for short-wavelength infrared (SWIR) and mid-wavelength (MWIR) infrared focal-plane arrays.[1–8] However, the goal of advancing this material technology to the long-wavelength (LWIR) regime has been hampered by the one to two orders of magnitude increase in dislocation density with respect to HgCdTe grown on lattice-matched bulk CdZnTe substrates. This deficiency in dislocation density has been shown to limit lifetimes,[9,10] lower mobility of carriers,[11] lead to larger dark currents in long-wavelength detectors,[12,13] and ultimately reduce focal-plane array operability.[9,14] Current growth methods of HgCdTe/Si result in a dislocation density of mid 10^6 cm^{-2} to low 10^7 cm^{-2}. It has been the goal of the HgCdTe community in the past several years to reduce this value significantly.

Recent studies on MBE growth of CdTe/Si have shown that *in situ* thermal cycle annealing, in which annealing is performed intermittently during the MBE growth process itself, is an effective means to reduce etch pit density (EPD) and improve overall crystal quality.[15] It has been observed that subjecting CdTe/Si layers to multiple-cycle *in situ* annealing can result in a reduction of EPD down to a saturation point of mid 10^5 cm^{-2}. Similar *in situ* cycle annealing on HgCdTe/GaAs at 350°C to 490°C resulted in a reported defect density of 2×10^6 cm^{-2} to 4×10^6 cm^{-2} from a baseline growth value of 9×10^6 cm^{-2} to 20×10^6 cm^{-2}.[16] Due to the high

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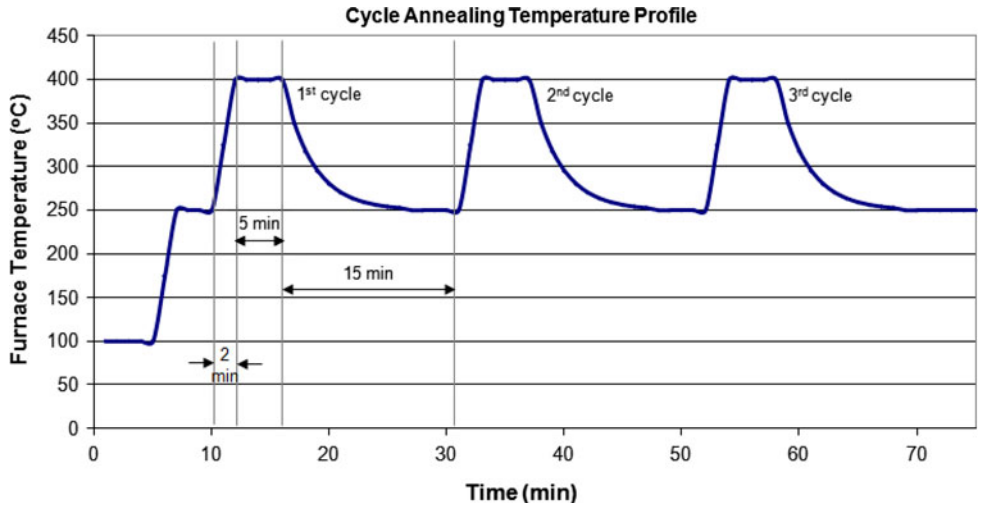

Fig. 1. Temperature profile of a three-cycle *ex situ* annealing experiment conducted with a maximum furnace temperature setpoint of 400°C. Annealing temperature, annealing duration, and number of cycles were variables within this study.

mercury overpressure needed to maintain the surface morphologies and composition of HgCdTe, a cap layer of ZnTe or ZnSe was used for these annealing experiments. Shin et al.[17] reported EPD reduction of HgCdTe/GaAs using *ex situ* cycle annealing, where annealing is performed outside the growth system and the epilayer is not specially capped and is exposed to a heavy mercury overpressure. This method of cycle annealing proved to be effective, with EPD in HgCdTe/GaAs reported as mid 10^5 cm^{-2}.[18,19]

In this paper we present our results of a detailed study on *ex situ* cycle annealing of HgCdTe/Cd(Se)Te/Si. In our study we examined the reduction in the dislocation density and improvement in overall crystalline quality with respect to the annealing temperature setpoint, number of annealing cycles, and total annealing time. Mercury overpressure was also studied in order to ensure that proper surface morphology could be maintained. The cycle annealing process was also compared with our standard device annealing process in terms of both dislocation reduction and electron mobility.

EXPERIMENTAL PROCEDURES

The majority of the HgCdTe samples used in this study were grown by MBE on composite CdTe/Si(112) substrates. A few HgCdTe layers were also grown on a lattice-matched CdSeTe/Si composite substrate for comparison. Details of the CdTe/Si growth process have been described elsewhere.[15,20] In brief, CdTe is nucleated on 3-inch nominal substrates utilizing arsenic passivation of the Si surface followed by growth of a thin ZnTe buffer layer. The final CdTe thickness measured between 8 μm and 10 μm. The subsequent HgCdTe layer was grown to a thickness of approximately 8 μm. The HgCdTe growth was performed at ~185°C with a growth rate of ~2 μm/h. The majority of the $Hg_{1-x}Cd_xTe$ layers were long-wavelength infrared with an x value of ~0.22, but both MWIR ($x \approx 0.33$) and SWIR ($x \approx 0.40$) were used throughout the course of this study. Finally, all as-grown HgCdTe layers were doped n-type using indium and had an as-grown dislocation density measuring between 5×10^6 cm^{-2} and 2×10^7 cm^{-2}.

Larger HgCdTe wafers were cleaved into smaller pieces, nominally sized 7 mm × 7 mm. Closed-ampoule annealing experiments were then conducted under a mercury atmosphere, with the annealed layers characterized by optical microscopy and EPD measurements. Additionally, several annealed layers were characterized using x-ray diffraction and Hall measurement. Figure 1 shows a schematic of a typical cycle annealing experiment. The annealing temperature, annealing duration, and number of cycles incorporated throughout the process were variables investigated in this study. Details of the annealing are described elsewhere.[21]

The dislocation density was measured via a dislocation decoration etch. We employed both a CrO_3/HCl/H_2O etch as well as the etch recently developed by D. Benson at U.S. Army CERDEC Night Vision and Electronic Sensors Directorate.[22] We did not observe any appreciable change in either dislocation size/shape or overall dislocation values with respect to the etching process and consider both etches to have successfully revealed dislocations that thread to the material's surface. A Nomarski optical microscope was used to count the etch pit density of both as-grown and annealed layers.

X-ray rocking curves were also recorded on selected samples using a PANalytical X'Pert Pro MRD to determine the full-width at half-maximum (FWHM) of several Bragg planes of the material under investigation. A dislocation value was then extracted from the x-ray FWHM data using the method described by Benson et al. regarding

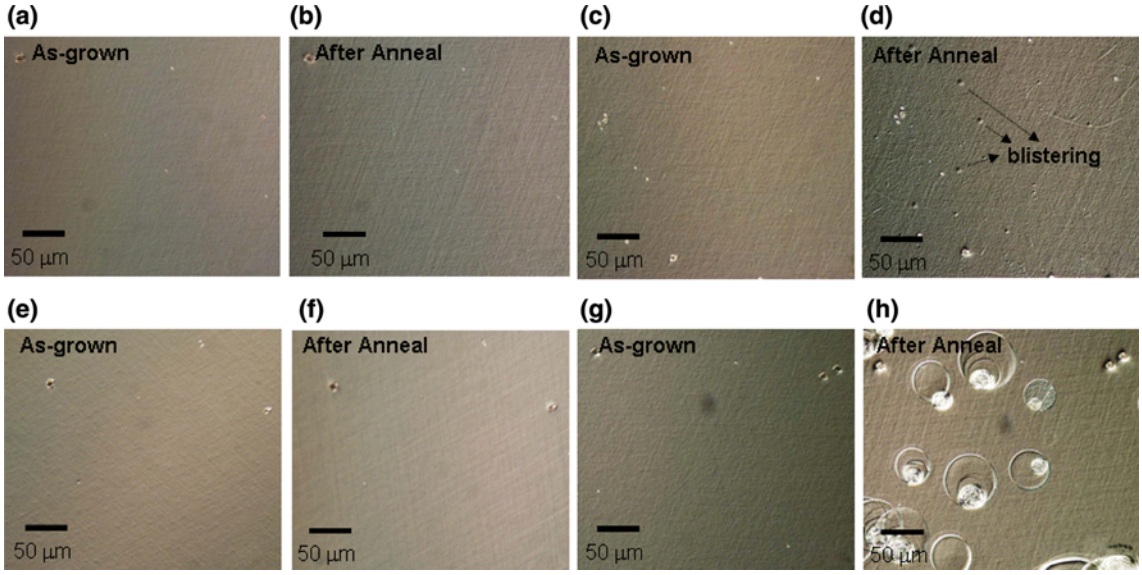

Fig. 2. One-to-one surface images of HgCdTe/Si before and after cycle annealing: (a, b) 400°C/four-cycle anneal using the baseline Hg amount; (c, d) 450°C/four-cycle anneal using the baseline Hg amount; (e, f) 450°C/four-cycle anneal using three times the baseline Hg amount; and (g, h) 450°C/four-cycle anneal using four times the baseline Hg amount.

dislocation density of CdTe/Si layers.[23] All measurements were taken with the Cu K_α wavelength and were performed at room temperature.

Finally, Hall measurements were made at 77 K to determine the electron mobility of select cycle annealed layers with respect to material that underwent a standard mercury saturation anneal. In this case, the cycle annealing process was followed by a 250°C mercury saturation anneal to fill Hg vacancies within the material.

RESULTS AND DISCUSSION

Surface Morphology After Cycle Annealing

Since the samples are heated repeatedly to a high temperature during the cycle annealing process, it was first necessary to investigate the amount of mercury overpressure needed in order to maintain good surface morphology. During our standard device annealing, we incorporate 150 μL of mercury within the closed ampoule. This provides enough overpressure to preserve a high-quality surface while also allowing for mercury vacancy filling during the saturation component of the anneal. Figure 2 shows several images of the HgCdTe surface both before and after annealing. For layers cycle annealed using a setpoint of 400°C, the HgCdTe surface could be maintained by using the baseline mercury overpressure that is used for device annealing, regardless of the number of cycles utilized or the duration of each anneal cycle, as shown in Fig. 2a and b. Note that the maximum temperature used during device annealing is also 400°C. In contrast, if the cycle annealing temperature setpoint was increased to 450°C while still maintaining the baseline mercury overpressure, then signs of surface roughening and blistering appeared. Figure 2c and d clearly shows this effect. In order to obtain proper surface morphology during a 450°C/four-cycle anneal we had to triple the amount of Hg used with respect to our baseline annealing process. Surface images prior to and after a 450°C/four-cycle anneal utilizing this higher mercury amount are shown in Fig. 2e and f. However, if too much mercury was used during the cycle annealing, defects due to mercury condensation on the sample would appear. Figure 2g and h shows before and after images from a HgCdTe/Si sample after undergoing a 450°C/four-cycle anneal with a fourfold increase in the baseline mercury amount. Note that, although the surface morphology in the areas where mercury condensation did not take place is well maintained, the presence of mercury condensation-related defects on the surface would render the sample unsuitable for subsequent device processing. Similar studies were conducted for several 500°C/four-cycle anneals as well, and it was determined that approximately four times the standard mercury overpressure was required to maintain proper surface morphology after an anneal at this temperature. As observed before at lower temperatures, too much mercury during a 500°C cycle anneal led to numerous condensation-related defects. These experiments showed that, although a good surface can be maintained at a higher cycle annealing temperature, the window of suitable mercury overpressures becomes narrower. In other words, at higher annealing temperatures, it was easier to either roughen the surface (too little Hg) or damage the surface through condensation defects (too much Hg). Finally, annealing at 550°C always resulted in a rough surface unsuitable for

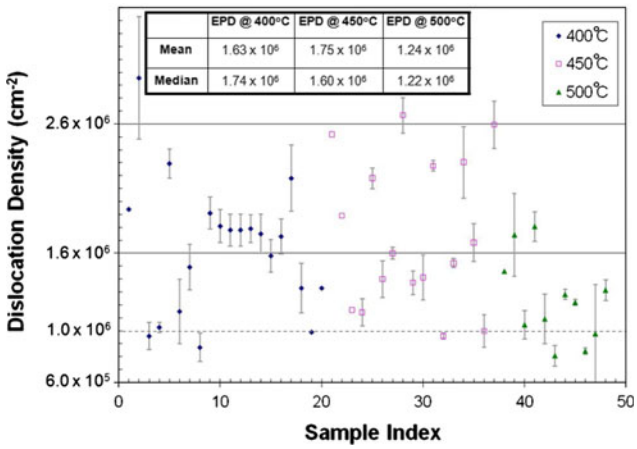

Fig. 3. Dislocation density measurements after cycle annealing experiments at various annealing temperatures. All samples underwent four annealing cycles and were held at the annealing setpoint for 5 min.

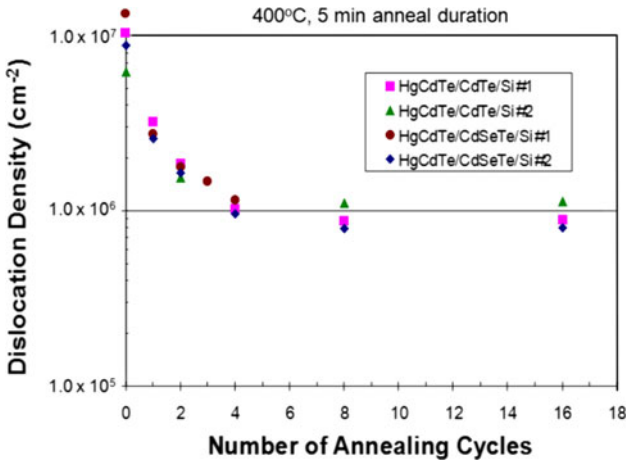

Fig. 4. Dislocation reduction as a function of the number of annealing cycles. Four layers were studied: two grown on CdTe/Si composite substrates and two grown on lattice-matched CdSeTe/Si composite substrates. The data points at zero cycles correspond to the as-grown dislocation density.

further characterization within the limits of the mercury overpressure studied.

Dislocation Measurements After Cycle Annealing

Dislocation density measurements taken from these cycle annealing temperature studies are shown in Fig. 3. For this set of data, the number of cycles was fixed at four and the anneal duration was fixed at 5 min per anneal. No difference is observed in the after-anneal dislocation density between the 400°C and 450°C cycle annealed samples. On average, the after-anneal dislocation density measures 1.7×10^6 cm^{-2} regardless of which temperature was used. At 500°C, a slight improvement in both the average dislocation value (1.2×10^6 cm^{-2}) and the spread of the data is observed. However, even in light of this modest improvement, most of the remaining experiments were conducted using an anneal setpoint of 400°C due to the ease of maintaining proper post-annealed surface morphology.

In contrast to the absolute annealing temperature parameter, strong dependence of the dislocation density reduction on the number of annealing cycles incorporated was observed. Figure 4 shows data taken from four separate HgCdTe/Si layers with respect to the number of cycles. The decrease in dislocation density follows an exponential decay as the number of cycles increases. Somewhere between four and eight cycles, the material reaches a minimum value, with no further reduction obtained as more cycles are added. From these four layers, we observed saturation in dislocation reduction to approximately 1×10^6 cm^{-2}.

To ensure that the dislocation reduction was indeed directly related to the number of annealing cycles rather than the total duration of annealing time, a set of experiments were conducted where the total annealing time was held approximately

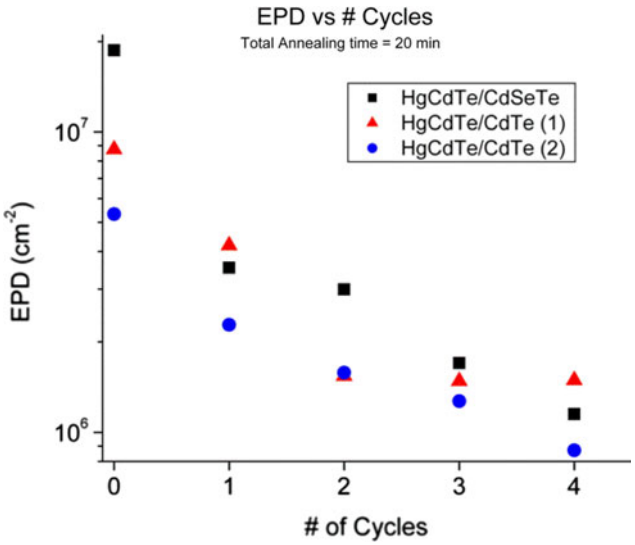

Fig. 5. Variation in dislocation density for fixed total annealing time. The annealing duration was adjusted to maintain a total annealing time of approximately 20 min. The data points at zero cycles correspond to the as-grown dislocation density.

constant but the number of cycles was varied. Four sister HgCdTe/Si pieces were annealed: the first was cycled once to a setpoint of 400°C for 20 min; the second piece was cycled twice to a setpoint of 400°C for 10 min each cycle; the third piece was cycled three times to a setpoint of 400°C for 7 min each cycle; and finally the fourth piece was cycled four times to a setpoint of 400°C for 5 min each cycle. The results are shown in Fig. 5 and clearly indicate that the number of cycles is driving the dislocation reduction not the total annealing time. Additionally, separate experimentation on the anneal duration yielded no improvement in dislocation reduction. Specifically, 400°C/four-cycle

Table I. Dislocation density for as-grown, standard device annealed, and four-cycle annealed HgCdTe/Si layers

Sample	As-Grown EPD (cm^2)	Standard Device Anneal EPD (cm^2)	Four-Cycle Anneal EPD (cm^2)
MCT/Si A	4.7×10^6	3.5×10^6	1.8×10^6
MCT/Si B	8.1×10^6	6.2×10^6	2.0×10^6
MCT/Si C	2.9×10^7	8.6×10^6	1.5×10^6

anneals were carried out using both 10 min and 20 min durations per cycle. Results were similar to those for the shorter duration of 5 min. No duration less than 5 min was studied.

As a final check of the efficacy of our cycle annealing process, we subjected as-grown HgCdTe/Si layers to both 400°C/four-cycle annealing as well as our standard device annealing process. The standard device annealing consists of an initial 400°C anneal for a short period of time (typical duration 6 min) followed by a 250°C saturation anneal using our baseline amount of mercury, 150 μL, within a closed ampoule. Table I shows the results for three different layers. Interestingly, the standard device anneal does reduce the dislocation density with respect to the as-grown material, although not nearly to the level observed with the cycle annealing process. This fits well with our other data, as the standard device anneal can be thought of as a one-cycle anneal (very abrupt heating and one cooling sequence).

To further characterize the cycle annealing process, we measured the x-ray FWHM of the [422] peak before and after annealing. Figure 6 shows data from both a 4-cycle annealed layer and a 16-cycle annealed layer in comparison with the as-grown layer. In both cases, the [422] peak narrows substantially, indicating that the crystallinity

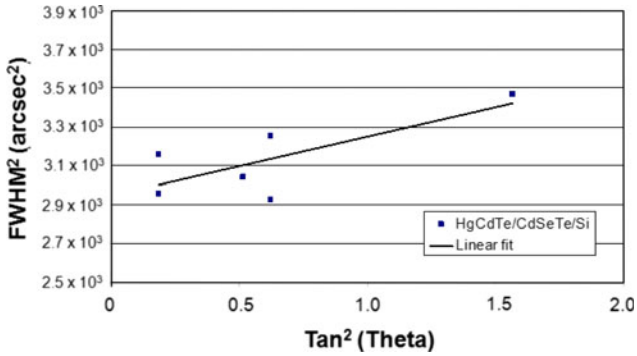

Fig. 7. Plot of the square of the FWHM versus $\tan^2 \theta_B$ for different Bragg angles from a four-cycle annealed layer. From this plot, the dislocation density value was ascertained as 1×10^6 cm^{-2} to 3×10^6 cm^{-2}.

of the material has been improved. Recently, Benson et al. were able to extract dislocation density values of various CdTe/Si(112) layers by measuring the FWHM of several Bragg angles to isolate the peak broadening effect due to dislocations.[23] We conducted a similar analysis for the cycle annealed HgCdTe/Si material and determined a dislocation density value of between 1×10^6 cm^{-2} and 3×10^6 cm^{-2}. The data, shown in Fig. 7, are limited due to the difficulty in measuring higher Bragg angles, but overall this analysis fits well with the dislocation density values that have been obtained through dislocation decoration etches.

From these results, it is clear that the main mechanism for dislocation reduction is the relative change in temperature that the sample experiences during the cycle annealing process. Absolute annealing temperature (above 400°C setpoint) may be argued to have an effect on dislocation reduction, but only as a secondary effect. Similarly, anneal duration has minimal impact upon dislocation reduction. Other factors related to initial material characteristics, such as HgCdTe composition,

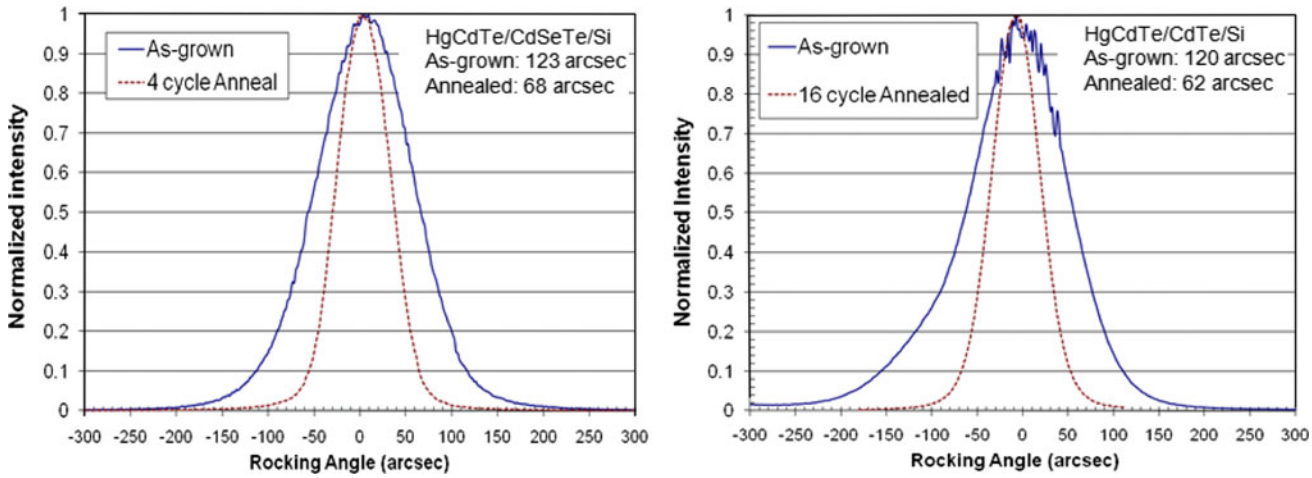

Fig. 6. X-ray FWHM from [422] peaks from a 4-cycle annealed layer and a 16-cycle annealed layer with respect to the as-grown layers.

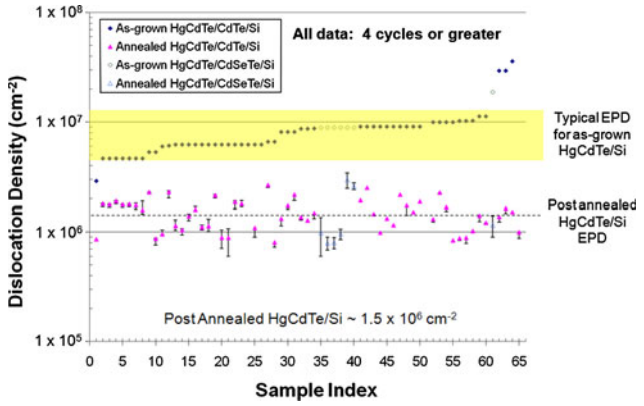

Fig. 8. Before and after dislocation density values for all HgCdTe/Si layers that underwent at least a four-cycle anneal. Average dislocation density after anneal measures 1.5×10^6 cm^{-2}.

CdTe/Si substrate quality (in terms of EPD), and lattice matching of the composite substrate (CdTe/Si versus CdSeTe/Si) have been reported in earlier studies and none appeared to influence final dislocation reduction.[21] More data needs to be gathered with respect to all of these parameters, especially lattice matching of the composite substrate, to conclusively determine their role in dislocation reduction, but to a first order only the number of cycles clearly impacts results.

In summary, the more times the sample is exposed to a temperature change, the more dislocation reduction is observed, down to a saturation point; from our studies, this saturation point is approximately 1×10^6 cm^{-2} for HgCdTe/Si. Figure 8 shows data from all experiments that were conducted with at least four cycles. At this point, it is hypothesized that the temperature change (both positive and negative) induces a strain field within the material, which in turn leads to dislocation movement. Once the dislocations are able to move, the probability that one dislocation can interact with another dislocation becomes nonzero, and hence dislocation annihilation occurs. However, after a certain point, the dislocations become isolated enough that one dislocation can no longer interact with another. At this point, the overall material dislocation value reaches a minimum and the inclusion of more annealing cycles does not further improve material quality.

Electron Mobility After Cycle Annealing

Finally, to truly realize the benefit of dislocation reduction through cycle annealing, the material has to be well behaved electrically as well. Some preliminary Hall studies were carried out to ascertain the impact of cycle annealing on electron mobility. To fill Hg vacancies within the material, a 250°C saturation anneal was performed after the last cycle anneal was completed. A comparison was made with HgCdTe/Si layers that underwent

Table II. Carrier concentration (cc) and mobility (Mob) data from standard device annealed and four-cycle annealed HgCdTe/Si layers

	Activation Anneal + 250°C Saturation Anneal cc at 77 K (cm^3)	Activation Anneal + 250°C Saturation Anneal Mob at 77 K (cm^2/V s)	Four-Cycle + 250°C Saturation Anneal cc at 77 K (cm^{-3})	Four-Cycle + 250°C Saturation Anneal Mob at 77 K (cm^2/V s)
Hall sample A (MCT/CT/Si)	2.9×10^{15}	125,000	2.6×10^{15}	75,200
Hall sample B (MCT/CST/Si)	1.0×10^{16}	73,100	6.1×10^{15}	104,000

our standard device anneal, which was described earlier. It should be noted that, although the device anneal is designed for arsenic activation, the layers used in this study were not doped with arsenic, only doped *in situ* with indium, as the end goal was only to study the electron mobility of the HgCdTe absorber layer. Table II shows the carrier concentration and mobility data from respective LWIR samples taken at 77 K. For the higher-doped sample (sample B), the mobility at 77 K after cycle annealing actually appears better than after the standard device anneal. In contrast, the lower-doped sample (sample A) shows a decrease in mobility after cycle annealing. In either case though, the electron mobility as measured by Hall looks reasonable for LWIR HgCdTe/Si material. However, much more electrical data needs to be gathered with respect to HgCdTe composition, doping density, and alternative substrate utilized (CdTe/Si versus CdSeTe/Si) before a complete understanding of dislocation mitigation in HgCdTe/Si material through cycle annealing can be obtained.

CONCLUSIONS

Thermal cycle annealing using temperature setpoints ranging between 400°C and 500°C has been shown to effectively and reproducibly reduce the dislocation density of HgCdTe/Cd(Se)Te/Si samples to approximately 1×10^6 cm^{-2}. This is the best EPD value found in the literature for HgCdTe/Si material grown by MBE. Additionally, some cycle annealed layers have measured EPD in the high 10^5 cm^{-2} range, although no single or set of parameters has yet been identified to achieve these levels consistently. Among several parameters studied in this work, the number of annealing cycles is the primary factor for decreasing the dislocation density. Comparisons with standard device annealing have been made. While preliminary Hall measurements do not show clear improvement, the observed mobility values are reasonable and suggest that electrical characteristics can be maintained after our *ex situ* cycle annealing procedure.

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