Journal of ELECTRONIC MATERIALS, Vol. 39, No. 4, 2010
DOI: 10.1007/s11664-009-1002-1

Improvement in Performance of Carbon Nanotube Field-Effect Transistors on Patterned SiO_2/Si Substrates

KENZO MAEHASHI,[1,2] SHIN IWASAKI,[1] YASUHIDE OHNO,[1] TAKAOMI KISHIMOTO,[1] KOICHI INOUE,[1] and KAZUHIKO MATSUMOTO[1]

1.—The Institute of Scientific and Industrial Research, Osaka University, 8-1 Mihogaoka, Ibaraki, Osaka 567-0047, Japan. 2.—e-mail: maehashi@sanken.osaka-u.ac.jp

Horizontally aligned single-walled carbon nanotubes (SWNTs) were fabricated on patterned SiO_2/Si substrates with groove-and-terrace structures, which were obtained using electron-beam lithography and reactive ion etching. Scanning electron microscopy observation revealed that SWNTs were aligned in the direction parallel to the groove-and-terrace structures and were preferentially grown along the edges of terraces. Using aligned SWNTs as multichannels, carbon nanotube field-effect transistors (CNTFETs) were fabricated on the patterned SiO_2/Si substrates. This method will be promising to control the direction of SWNTs on SiO_2/Si substrates for fabrication of high-performance CNTFETs with high current outputs.

Key words: CNTFETs, patterned SiO_2/Si substrates, groove-and-terrace structures, horizontally aligned single-walled carbon nanotubes, edge of terraces

INTRODUCTION

Since single-walled carbon nanotubes (SWNTs) have unique mechanical, chemical, and electrical properties, they are one of the most promising materials for fabrication of nanoscale devices such as field-effect transistors (FETs) and single-electron transistors.[1–6] In particular, carbon nanotube FETs (CNTFETs) are one of the promising candidates for application as highly integrated CNT-based circuits and highly sensitive label-free sensors,[7–14] because they have excellent transport properties with high mobility. Thus, CNTFETs with high performance are necessary to realize such devices.

Well-aligned, very dense SWNT arrays are expected to be used as channels for high-performance CNTFETs with high current outputs. In recent years, SWNTs with high density have been aligned in a specific crystallographic direction on sapphire or single-crystal quartz substrates.[15–17] Furthermore, it has been demonstrated that aligned SWNTs on sapphire or single-crystal quartz substrates can be transferred to flexible substrates.[18,19] In previous reports, using conventional photolithography and the metal lift-off process, catalyst particles could be precisely positioned on SiO_2/Si substrates and SWNTs grown from the catalyst particles.[20,21] In general, however, the growth direction of SWNTs on SiO_2/Si substrates is difficult to control since SiO_2 is an amorphous material. Control of the SWNT growth direction on SiO_2/Si substrates is still demanded for the fabrication of nanodevices using conventional silicon processes.

In this work, we synthesized horizontally aligned SWNTs on patterned SiO_2/Si substrates with groove-and-terrace structures using electron-beam (EB) lithography and reactive ion etching (RIE), and then fabricated CNTFETs on the substrates. We demonstrated performance improvement of CNTFETs on the patterned SiO_2/Si substrates.

EXPERIMENTAL PROCEDURES

The fabrication process of the patterned SiO_2/Si substrates with groove-and-terrace structures was as follows: A p^+-type Si wafer with a thermally oxidized SiO_2 (300 nm) layer was used as a

(Received July 23, 2009; accepted November 4, 2009; published online November 24, 2009)

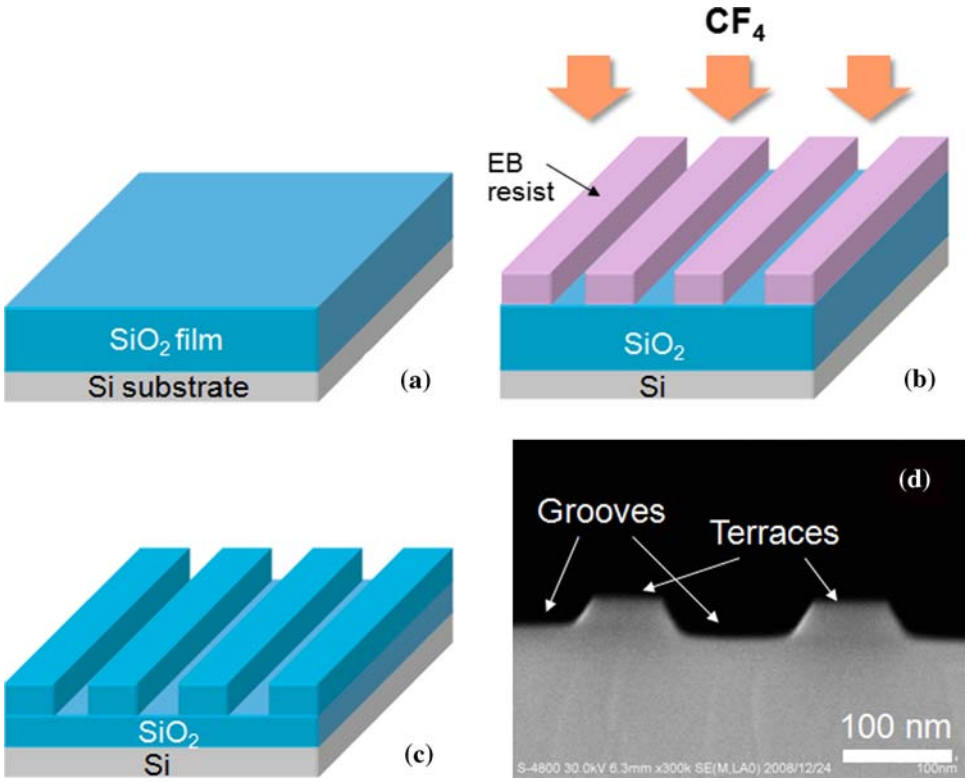

Fig. 1. Fabrication process of the patterned SiO_2/Si substrates with groove-and-terrace structures: (a) formation of SiO_2 film on Si substrate, (b) RIE technique using CF_4 gas after developing the EB resist and (c) groove-and-terrace structures. (d) Cross-sectional SEM image on the SiO_2/Si patterned substrates with groove-and-terrace structures.

substrate, as shown in Fig. 1a. After coating the SiO_2 layer with EB resist (ZEP520A), lines were patterned using EB lithography, as shown in Fig. 1b. The SiO_2 layer was etched by the RIE technique using CF_4 gas after developing the EB resist, as shown in Fig. 1c. Figure 1d shows a cross-sectional scanning electron microscopy (SEM) image of typical patterned substrates with groove-and-terrace structures. The height of the terraces was controlled by the etching time in the RIE process. Subsequently, a 0.5-nm-thick Co catalyst was patterned on the substrates using conventional photolithography. Then, SWNTs were synthesized by thermal chemical vapor deposition at 900°C for 10 min, using C_2H_5OH as a source gas.[20,21]

RESULTS AND DISCUSSION

Figure 2a, b shows SEM images of the SWNTs on the patterned and planar SiO_2/Si substrates, respectively. As shown in the SEM image, the SWNTs started to grow from the patterned catalyst area. The height and width of the terraces in Fig. 2a were estimated to be approximately 40 nm and 100 nm, respectively. As shown in Fig. 2b, on the flat substrate, SWNTs were meandering in random directions, which is due to the amorphous nature of the SiO_2 film. In contrast, the SEM observation in Fig. 2a reveals that the SWNTs were aligned parallel to the groove-and-terrace structures. It is noted that the SWNT growth direction was not affected by the direction of gas flow during SWNT synthesis. Figure 3a and b show typical Raman spectra of the SWNTs at low- and high-frequency regions, respectively, which were synthesized on the patterned SiO_2/Si substrates. Radial breathing modes[22] that are specific to SWNTs were clearly observed, as shown in Fig. 3a. In addition, a strong G-band peak was observed, and the D-band peak, which is related to structural disorder, was quite weak, as shown in Fig. 3b. These results indicate that high-purity high-quality SWNTs were formed on the patterned SiO_2/Si substrates. Therefore, these results indicate that the patterned substrates are useful to control the growth direction of SWNTs. Some SWNTs on the patterned substrates were grown astride a few groove-and-terrace structures; the other SWNTs were oriented in a straight line along one groove-and-terrace structure. In addition, patterned SiO_2/Si substrates with a terrace height of 60 nm were also fabricated, and then SWNTs were synthesized on the substrates. SWNTs were aligned in the direction parallel to the groove-and-terrace structures. It was found that there was little difference in the alignment of SWNT growth between the terraces with heights of 40 nm and

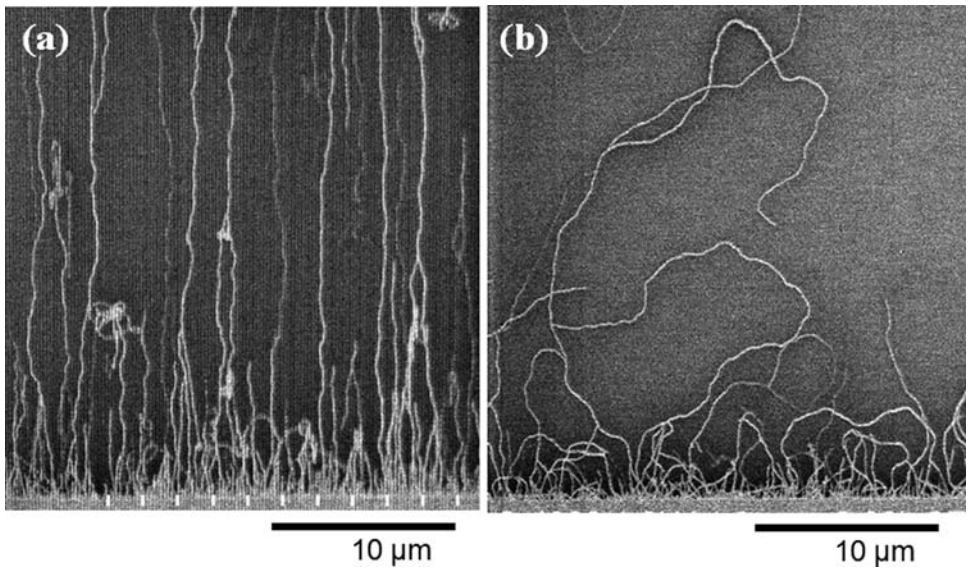

Fig. 2. SEM images of SWNTs on (a) SiO_2/Si patterned substrate with groove-and-terrace structures and (b) flat substrate.

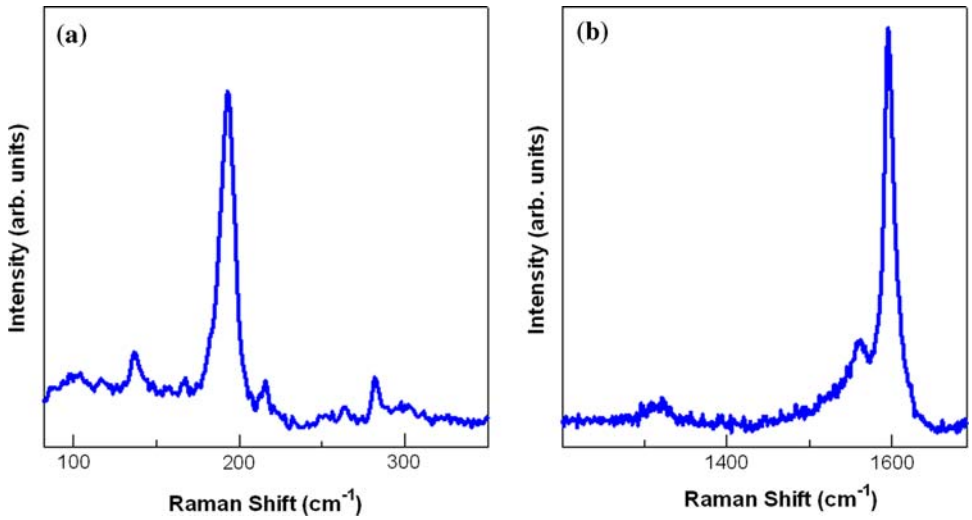

Fig. 3. Raman spectra of SWNTs synthesized on patterned SiO_2/Si substrates: (a) low-frequency region and (b) high-frequency region.

60 nm. We suggest that such terrace height is sufficient for alignment of SWNT growth because it is much larger than the diameter of the SWNTs.

To investigate the exact position of the SWNTs on the patterned SiO_2/Si substrates with groove-and-terrace structures, a bird's-eye-view SEM image was taken, as shown in Fig. 4a. The SEM image reveals that SWNTs were adhered to the edge of the terraces, as shown in Fig. 4b. For this reason, the growth direction of the SWNTs is parallel to the groove-and-terrace structures. The reason why SWNTs adhered to the edge of the terrace can be understood by considering the Casimir-Polder interaction between the SWNTs and the Si substrate.[23,24] The potential energy of a small portion of SWNT located near an infinite flat substrate is proportional to $\sim -1/d^4$, where d is the distance from the substrate surface. The Casimir-Polder potential can decrease as the SWNTs approach the patterned substrates and be modulated by the substrate pattern. In particular, the force lines of the Casimir-Polder potential can be concentrated at the edges of the terraces. As a result, the density of the force lines at the edges of the terraces can become much higher than that on the edges of the grooves. Therefore, the SWNTs are preferentially grown along the edge of the terraces.

Finally, CNTFETs were fabricated on the patterned SiO_2/Si substrates with groove-and-terrace structures. The horizontally aligned SWNTs were used as the channels of the CNTFETs. The inset of Fig. 5 shows an SEM image of a CNTFET fabricated on the patterned SiO_2/Si substrate. Ti/Pd was used for source and drain electrodes. The distance

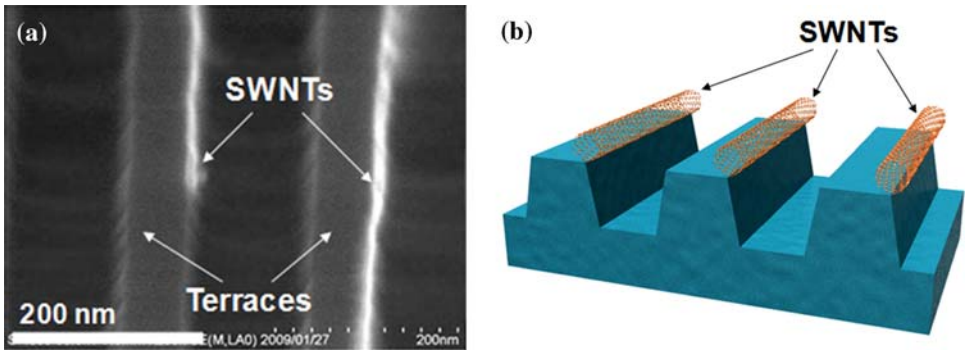

Fig. 4. (a) SEM image of SWNTs on the patterned SiO_2/Si substrate with groove-and-terrace structures, and (b) schematic illustration of SWNTs on the SiO_2/Si patterned substrate with groove-and-terrace structures.

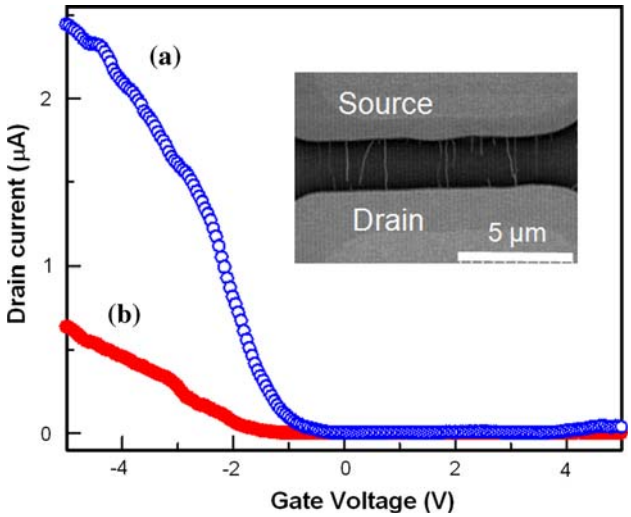

Fig. 5. Transfer characteristics in CNTFETs fabricated on (a) patterned and (b) flat SiO_2/Si substrates. The inset shows an SEM image of the CNTFET fabricated on the patterned SiO_2/Si substrate.

between the source and drain electrodes was estimated to be approximately 3 μm. The SEM image reveals that several SWNTs bridged between the source and drain electrodes. Figure 5a shows the drain current in the CNTFET on the patterned SiO_2/Si substrates with groove-and-terrace structures at room temperature as a function of back-gate voltage. The back-gate voltage was swept from -5 V to 5 V. The source–drain current increased with decreasing back-gate voltage in the positive direction, indicating that the device had *p*-type characteristics. A good pinch-off characteristic with a threshold voltage of 0.5 V and an on/off ratio of 10^4 were obtained. The transconductance was estimated to be 1.7 μS. It is noted that no leakage current between the source and back-gate electrodes was measured. For comparison, transfer characteristics of a CNTFET fabricated on a flat surface are shown in Fig. 5b. The device was formed under the same conditions as that on the patterned SiO_2/Si substrates. Similar transfer characteristics to those in the previous report were obtained.[21] These results indicate that the CNTFET fabricated on the patterned SiO_2/Si substrates had five times higher transconductance and four times larger on-current than that built on the flat surface. For the CNTFET on the flat surface, one SWNT was bridged between the source and drain electrodes. In contrast, several SWNTs were bridged between the source and drain electrodes for the CNTFET on the patterned SiO_2/Si substrates. As a result, a higher-performing CNTFET was obtained. We expect to synthesize more aligned SWNTs with high density using the described method, optimizing the formation condition of the patterned substrate and the growth conditions of the SWNTs. Such CNTFETs on patterned SiO_2/Si substrates will be useful for the formation of highly integrated CNT-based circuits and highly sensitive label-free sensors.

CONCLUSIONS

We synthesized horizontally aligned SWNTs on patterned SiO_2/Si substrates with groove-and-terrace structure using EB lithography and RIE. SEM observation revealed that the SWNTs were preferentially grown along the edges of terraces on the patterned SiO_2/Si substrates. This phenomenon is interpreted based on the Casimir-Polder potential between the SWNTs and the substrate. For this reason, SWNTs were aligned parallel to the groove-and-terrace structures. CNTFETs with multichannels were fabricated on the patterned SiO_2/Si substrates. This method will be promising to control the direction of SWNTs on SiO_2/Si substrates for fabrication of high-performance CNTFETs with high current outputs.

ACKNOWLEDGEMENTS

The authors acknowledge the generous support from the Core Research for Evolutional Science and Technology, the Japan Science and Technology Corporation, Grant-in-Aid for Scientific Research on Priority Area of MEXT, and Scientific Research from the Japan Society for the Promotion of Science, and Special Education, and Research Expenses

(Post-Silicon Materials and Devices Research Alliance) from the Ministry of Education, Culture, Sports, Science, and Technology of Japan.

REFERENCES

1. S. Tans, A. Verschueren, and C. Dekker, *Nature* 393, 49 (1998).
2. Z. Chen, J. Appenzeller, J. Knoch, Y. Lin, and P. Avouris, *Nano Lett.* 5, 1497 (2005).
3. M. Bockrath, D. Cobden, P. McEuen, N. Chopra, A. Zettl, A. Thess, and R. Smalley, *Science* 275, 1922 (1997).
4. D. Mann, A. Javey, J. Kong, Q. Wang, and H. Dai, *Nano Lett.* 3, 1541 (2003).
5. K. Maehashi, H. Ozaki, Y. Ohno, K. Inoue, K. Matsumoto, S. Seki, and S. Tagawa, *Appl. Phys. Lett.* 90, 023103 (2007).
6. Y. Ohno, Y. Asai, K. Maehashi, K. Inoue, and K. Matsumoto, *Appl. Phys. Lett.* 94, 053112 (2009).
7. V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, *Nano Lett.* 1, 453 (2001).
8. A. Javey, Q. Wang, A. Ural, Y. Li, and H. Dai, *Nano Lett.* 2, 929 (2002).
9. K. Maehashi, T. Katsura, K. Karman, Y. Takamura, K. Matsumoto, and E. Tamiya, *Anal. Chem.* 79, 782 (2007).
10. A. Star, J. Gabriel, K. Bradley, and G. Gruner, *Nano Lett.* 3, 459 (2003).
11. K. Maehashi, K. Matsumoto, Y. Takamura, and E. Tamiya, *Electroanalysis* 21, 1285 (2009).
12. T. Katsura, Y. Yamamoto, K. Maehashi, Y. Ohno, and K. Matsumoto, *Jpn. J. Appl. Phys.* 47, 2060 (2008).
13. K. Maehashi and K. Matsumoto, *Sensors* 9, 5368 (2009).
14. K. Besteman, J. Lee, F. Wiertz, H. Heering, and C. Dekker, *Nano Lett.* 3, 727 (2003).
15. S. Han, X. Liu, and C. Zhou, *J. Am. Chem. Soc.* 127, 5294 (2005).
16. C. Kocabas, S. Hur, A. Gaur, M. Meitl, M. Shim, and J. Rogers, *Small* 1, 1110 (2005).
17. S. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. Alam, S. Rotkin, and J. Rogers, *Nat. Nanotechnol.* 2, 230 (2007).
18. X. Liu, S. Han, and C. Zhou, *Nano Lett.* 6, 34 (2006).
19. Q. Cao, H. Kim, N. Pimparkar, J. Kulkarni, C. Wang, M. Shim, K. Roy, M. Alam, and J. Rogers, *Nature* 454, 495 (2008).
20. D. Kaminishi, H. Ozaki, Y. Ohno, K. Maehashi, K. Inoue, K. Matsumoto, Y. Seri, A. Masuda, and H. Matsumura, *Appl. Phys. Lett.* 86, 113115 (2005).
21. K. Maehashi, Y. Ohno, K. Inoue, K. Matsumoto, T. Niki, and H. Matsumura, *Appl. Phys. Lett.* 92, 183111 (2008).
22. K. Maehashi, Y. Ohno, K. Inoue, and K. Matsumoto, *Appl. Phys. Lett.* 85, 858 (2004).
23. H. Casimir and D. Polder, *Phys. Rev.* 73, 360 (1948).
24. K. Milton, P. Parashar, and J. Wagner, *Phys. Rev. Lett.* 101, 160402 (2008).