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Ex Situ Thermal Cycle Annealing of Molecular Beam Epitaxy Grown HgCdTe/Si Layers

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We present the results of *ex situ* thermal cycle annealing (TCA) of molecular beam epitaxy grown mercury cadmium telluride (HgCdTe) on Cd(Se)Te/Si(211) composite substrates. We examined the variation in the etch pit density (EPD) and overall crystalline quality with respect to annealing temperature, number of annealing cycles, total annealing time, pre-annealed EPD/crystal quality, buffer layer quality, and buffer layer lattice constant. Using TCA we observed an order of magnitude reduction in the dislocation density of the HgCdTe layers and a corresponding decrease in x-ray full width at half maximum, when the as-grown layer EPD was on the order of 1×10^7 cm^{-2}. Among all the parameters studied, the one with the greatest influence on reducing EPD was the number of annealing cycles. We also noticed a saturation point where the HgCdTe/Si EPD did not decrease below $\sim 1 \times 10^6$ cm^{-2}, regardless of further TCA treatment or the as-grown EPD value.

Key words: Mercury cadmium telluride (HgCdTe), thermal cycle annealing, etch pit density (EPD), dislocations, molecular beam epitaxy (MBE), silicon (Si), composite substrates

INTRODUCTION

HgCdTe on Si technologies are effective means for producing short wavelength infrared (SWIR) and medium wavelength infrared (MWIR) focal plane arrays.[1–3] However, there remains a problem with defects causing shorter lifetimes and lowering the mobility of minority carriers, and large dark currents in long wavelength infrared (LWIR) detectors.[4,5] Current growth methods of HgCdTe/CdTe/Si result in a dislocation density of mid- to high 10^6 cm^{-2}, which is relatively high in comparison with the HgCdTe growth on lattice-matched bulk CdZnTe substrates.

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Recent work[6] on CdTe/Si has shown that *in situ* thermal cycle annealing (TCA), where annealing is performed intermittently during the growth process itself, is an effective means to reduce etch pit density (EPD) and improve overall crystal quality. Subjecting CdTe/Si layers to multiple cycle *in situ* annealing can result in a reduction of EPD up to a saturation point of mid-10^5 cm^{-2}. Similar *in situ* cycle annealing on HgCdTe/GaAs at 350–490°C has resulted in an EPD of 2–4 $\times$ 10^6 cm^{-2} from the base line growth value of 9–20 $\times$ 10^6 cm^{-2}.[7] Owing to the high mercury over-pressure needed to maintain the surface morphologies and composition of HgCdTe, a cap layer of ZnTe or ZnSe was used in those annealing experiments. Shin et al.[8] reported an EPD reduction of HgCdTe/GaAs using *ex situ* TCA, where annealing was performed outside the growth system and the epilayer was not specially capped

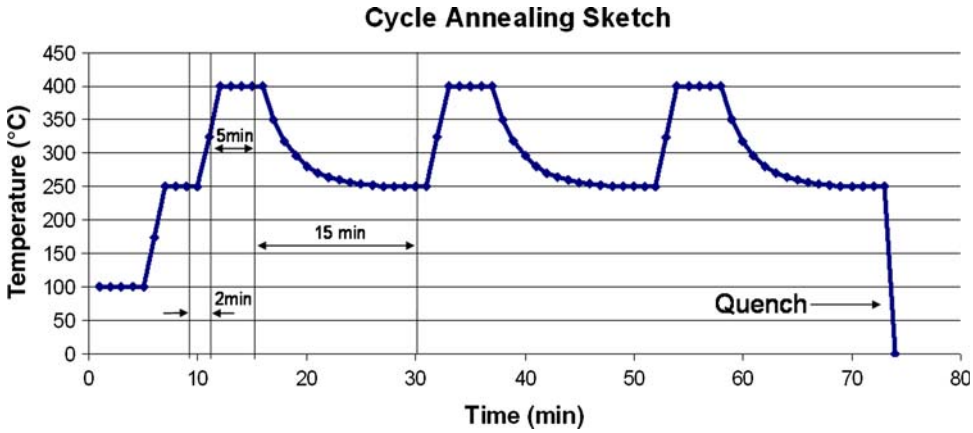

Fig. 1. Temperature versus time schematic of a three-cycle annealing process for a maximum annealing temperature of 400°C.

and was exposed to a heavy mercury over-pressure. This method of cycle annealing was effective in reducing EPD in HgCdTe/GaAs to mid-10^5 cm^{-2}.[8,9]

In this paper we present our results from a detailed study of *ex situ* cycle annealing of HgCdTe/CdTe/Si. In our study we examined the variation in EPD and the overall crystalline quality with respect to annealing temperature, number of annealing cycles, total annealing time, pre-annealed EPD/crystal quality, Cd composition, buffer layer quality, and buffer layer lattice constant. For comparison, we also examined the effects of TCA on the HgCdTe layer grown on lattice-matched ($x \approx 0.04$) $Cd_{1-x}Se_xTe$/Si substrates and on bulk lattice-matched ($x \approx 0.04$) $Cd_{1-x}Zn_xTe$ substrates.

EXPERIMENT

The samples used in this study were grown by molecular beam epitaxy (MBE) on composite CdTe/Si substrates, except where noted. Details of the CdTe/Si growth process have been described elsewhere.[6,10] In brief, CdTe was nucleated on 3-in. nominal substrates using arsenic passivation of the Si surface followed by the growth of a thin ZnTe buffer layer. The subsequent CdTe layer was grown to a thickness of approximately 9 μm. One HgCdTe layer was grown on a lattice-matched CdSeTe/Si composite substrate, while another HgCdTe layer used in this study was grown on a bulk CdZnTe substrate for comparison. The HgCdTe was grown at ~185°C, with a growth rate of ~2 μm/h. The typical HgCdTe layer thicknesses used in these experiments were between 8 μm and 10 μm. The majority of the $Hg_{1-x}Cd_xTe$ layers had an x value of ~0.20 (intended for LWIR application), but both $x \approx 0.33$ (for MWIR) and $x \approx 0.40$ (for SWIR) were also used for comparison.

Samples were cleaved into roughly 7 mm × 7 mm pieces and later were sealed in a quartz ampoule with 100–1000 μl of mercury under a vacuum of ~10^{-5} Torr. The samples were then placed in the center zone of a Lindburg 6 in.-diameter three-zone furnace, which was held at 100°C. Samples were then heated to 250°C. Once the temperature had stabilized (approximately 5 min), the cycle annealing process was initiated. The first step of this process was to heat the samples to the annealing temperature (400–500°C), which was a variable in this study. Generally, this heating time took 2–3 min. The furnace was held at the annealing temperature for another 5 min before being brought back to 250°C. The cooling time from the annealing temperature to 250°C took 10–20 min, depending on the annealing temperature. This cycle was repeated. After the final cycle, the ampoule was held at 250°C before being removed and quenched in a water bath. A schematic of a typical cycle annealing experiment is shown in Fig. 1.

We measured the threading dislocation density using a dislocation decoration etch. This etching process consisted of a quick (2–3 s) 0.5% bromine–methanol etch to clean the surface, followed by a 35 s CrO_3/HCl/H_2O etch, and then another quick bromine–methanol etch to enhance the pit's visibility. The EPD was then counted with an optical Nomarski microscope.

We also recorded the x-ray rocking curves on selective samples using a PANalytical X'Pert Pro materials research diffractometer (MRD) on the (422) crystal plane to determine the full width at half maximum (FWHM), which gives a general assessment of the crystal quality. All measurements were taken with the Cu Kα wavelength and were performed at room temperature.

RESULTS AND DISCUSSION

Since we performed the annealing experiments well above the HgCdTe growth temperature, it was necessary for us to investigate the amount of Hg needed to maintain the surface morphology of the samples. If insufficient Hg was placed in the ampoule, the surface roughened significantly, as shown in Fig. 2. Calculated Hg pressures of approximately 7 atm, 25 atm, and 35 atm were needed to

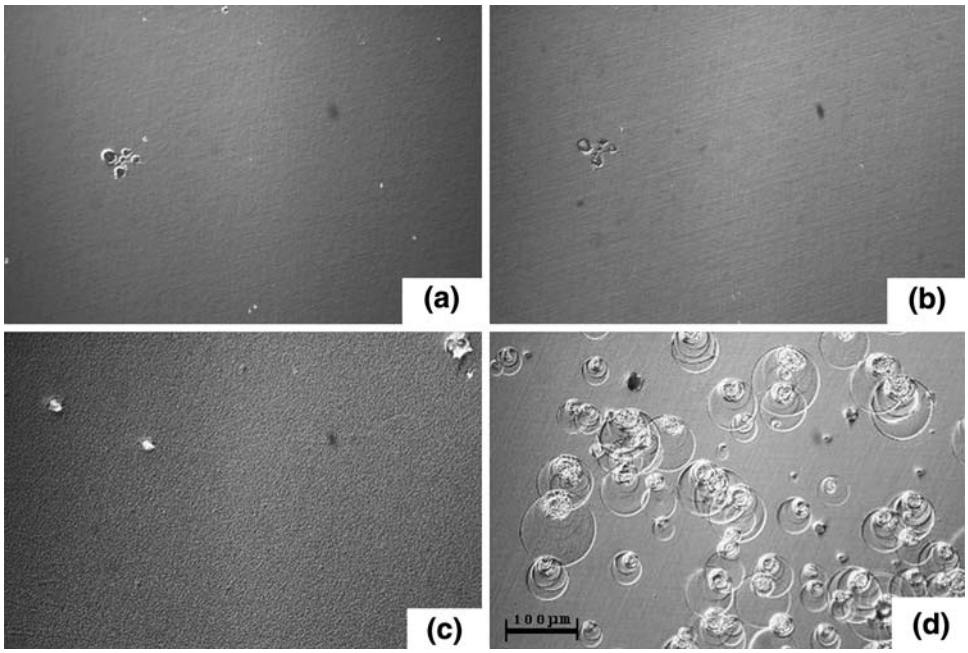

Fig. 2. Surface morphology of HgCdTe/Si samples. (a) As-grown, (b) TCA with correct amount of Hg, (c) TCA with insufficient amount of Hg, and (d) TCA with excessive amount of Hg.

preserve the surface for annealing temperatures of 400°C, 450°C, and 500°C, respectively. For anneals performed at 550°C, the HgCdTe surface morphology could not be preserved, regardless of the amount of Hg used. At all annealing temperatures, there was a problem with Hg condensation on the samples, as shown in Fig. 2d, when an excessive amount of Hg (>10 atm above the required Hg pressure) was used. Condensation could be partially prevented by our placing the sample face down, either directly on the inside bottom surface of the quartz ampoule or onto a clean piece of silicon. These techniques did not have a detrimental effect on the EPD. However, placing the samples face down on the ampoule's inner surface typically resulted in damage to the edges where the HgCdTe layer was in contact with the quartz. We found that putting the sample surface on a piece of silicon, leaving no HgCdTe surface exposed, prevented Hg condensation during cool down and did not show the edge damaging effects that occurred when the sample was placed directly on the ampoule's inner surface. Consequently, we obtained reproducible and better surface morphologies when the samples were placed face down on a piece of silicon. By using proximity annealing techniques, we could anneal the samples at higher temperatures, and the surface could be preserved for characterization, as shown in Fig. 2b.

The main focus of the remainder of the study was to explore the effects of various annealing parameters on the resulting EPD. We examined EPD as a function of annealing temperature for 400°C, 450°C, and 500°C, using four annealing cycles. Experiments at each temperature were repeated several times on different samples. Table I shows the summary of the results for the three annealing temperatures, using samples with an as-grown layer EPD of 6×10^6 cm^{-2} to 1×10^7 cm^{-2}. The results of Table I show that the annealing temperature (for the range we studied) had little role in the reduction of EPD in the samples. While there is evidence to suggest that high temperatures might provide more consistent EPD results, the large amounts of Hg used at high temperatures, to maintain a good surface morphology, could create Hg condensation issues.

Figure 3 shows the variation of EPD as a function of the number of annealing cycles. To limit the Hg condensation, which could be a compounding problem for a larger number of annealing cycles, we performed these anneals at 400°C. As shown in Table I, the results for 400°C closely matched those at higher annealing temperatures. Figure 3 shows an initial exponential decay followed by a saturation of the EPD at $\sim 1 \times 10^6$ cm^{-2} after four cycles. This finding differs from the results by Shin et al.,[8] who saw a further reduction of EPD in HgCdTe/GaAs for eight-cycle annealing as compared to four-cycle annealing. Likely, this difference resulted because the mismatch of the thermal coefficient of expansion and/or the lattice mismatch were much greater for the HgCdTe/Si system than for the HgCdTe/GaAs system. The larger mismatches in the case of HgCdTe/Si when compared with the HgCdTe/GaAs system were expected to play a role in the higher saturation in the EPD value. We measured the EPD values in the 8×10^5 cm^{-2} to 9×10^5 cm^{-2} range for some samples, but the overall EPD saturated at $\sim 1 \times 10^6$ cm^{-2}.

Table I. Etch pit density after four-cycle annealing at different temperatures

Temperature (°C)	Average EPD (cm^2)	Standard Deviation (cm^2)
400	1.2×10^6	5.2×10^5
450	1.6×10^6	7.2×10^5
500	1.4×10^6	3.2×10^5

The as-grown EPD of the samples used for this set of experiments was in the range 6×10^6 cm^{-2} to 1×10^7 cm^{-2}.

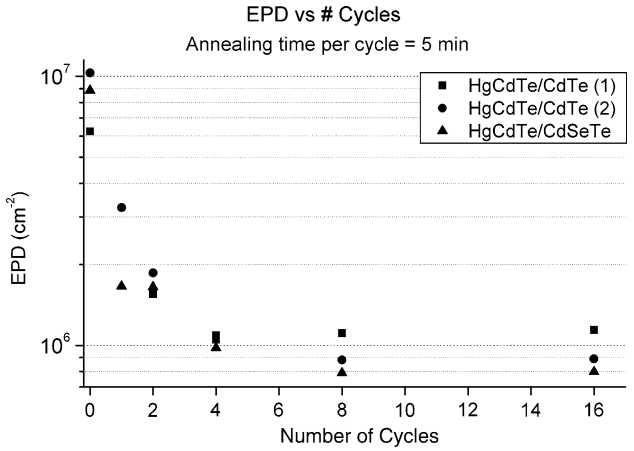

Fig. 3. Variation of EPD with the number of annealing cycles for an annealing time of 5 min per cycle and an annealing temperature of 400°C.

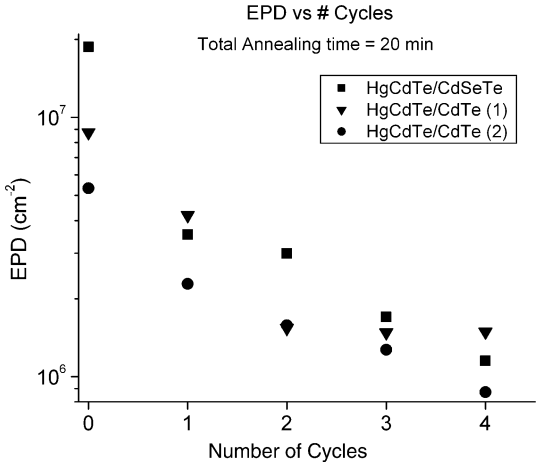

Fig. 4. Variation of EPD with number of annealing cycles, with the total annealing time being kept constant at 20 min for an annealing temperature of 400°C.

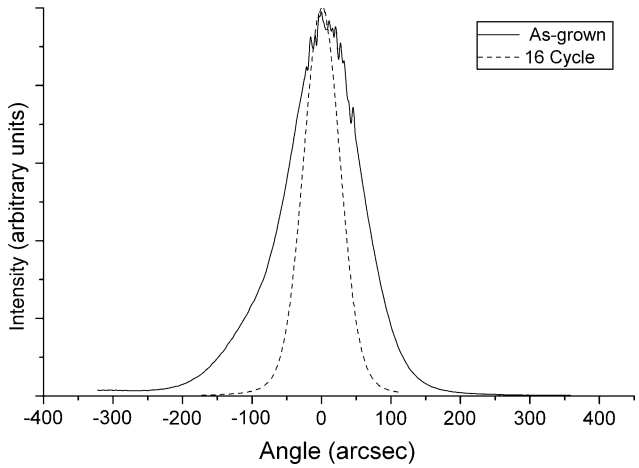

Fig. 5. Comparison between the rocking curves recorded on an as-grown sample having an EPD of 1×10^7 cm^{-2} (solid line) and a 400°C and a 16-cycle annealed sample having an EPD of 8.9×10^5 cm^{-2} (broken line). The FWHM values for the as-grown and the annealed samples are 120 arcsec and 62 arcsec, respectively.

To ensure that the EPD reduction was, indeed, directly related to the number of annealing cycles rather than to the total duration of annealing time, we also conducted experiments where the total annealing time was held constant but the number of cycles was varied. We performed single through four-cycle anneals, while keeping the total annealing time constant at 20 min. Specifically, we held a single-cycle anneal at 400°C for 20 min, a two-cycle anneal for 10 min each cycle, a three-cycle anneal for 7 min each cycle, and a four-cycle anneal for 5 min each cycle. These results are shown in Fig. 4. From the data presented in Figs. 3 and 4, it is clear that the total annealing time was not causing the EPD reduction, but rather the effect was caused by the cyclical nature of the annealing. Additional experimentation of four-cycle annealings with 10-min and 20-min duration for each cycle yielded no advantage over our using 5-min cycles.

Figure 5 shows typical x-ray rocking curves recorded on as-grown and 16-cycle annealed (at 400°C) HgCdTe/Si samples. The crystalline quality has clearly improved, with a reduction in the FWHM from 120 arcsec to 62 arcsec. This result is consistent with those of other studies that show a correlation between x-ray FWHM and defect density.[11] The variation of FWHM with the number of annealing cycles is shown in Fig. 6. The x-ray measurements were performed prior to our performing the EPD etch. Figure 6 also shows an initial exponential decay in FWHM of the x-ray rocking curves as the number of annealing cycles increases, as observed previously in Fig. 3 for EPD as a function of the number of annealing cycles. However, unlike the values of the EPD versus number of annealing cycles in Fig. 3, the values of the x-ray rocking curve FWHM slowly continue to decrease as the number of annealing cycles increases. This result might indicate that the overall quality of the crystal would continue to improve as the number of annealing cycles increases, but at a smaller rate than can be discerned using a defect decoration etch.

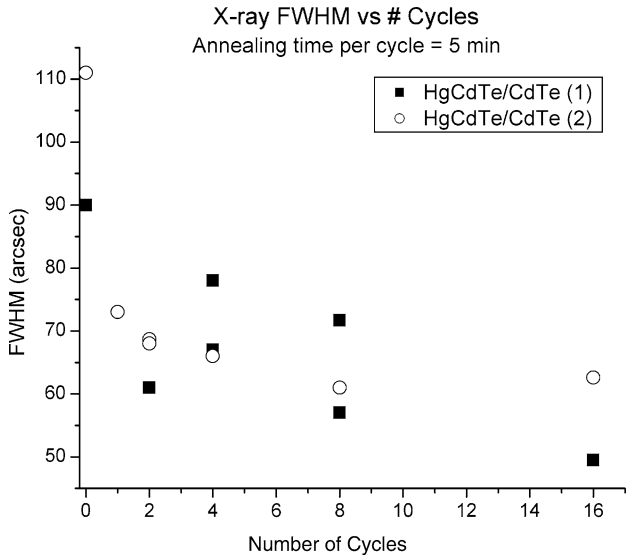

Fig. 6. Variation of x-ray rocking curve FWHM of the (422) crystal plane with number of annealing cycles.

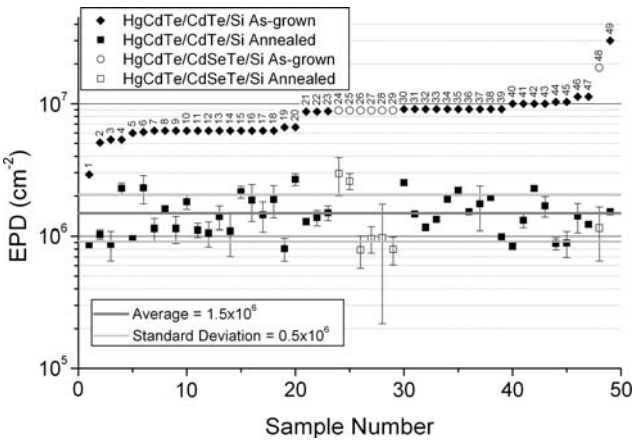

Fig. 7. Depiction of our comprehensive TCA experimental data. For each sample, EPD values before and after TCA are shown.

To understand the 1×10^6 cm^{-2} EPD saturation, we used for the TCA experiments HgCdTe/Si samples with a large variation in as-grown EPD. As stated previously, the results of experiments with variable annealing temperatures indicated that the annealing temperature was not the leading factor in EPD reduction. As a result, the majority of further anneals were carried out at 400°C, although some 450°C and 500°C anneals were also preformed for comparison. The results of this comprehensive annealing study are shown in Fig. 7. The as-grown EPD of the sample had little to no effect on the post-annealed EPD value measured within the as-grown EPD range investigated. The post-anneal EPD of all samples in Fig. 7 had an average value of 1.5×10^6 cm^{-2}, with a standard deviation of 0.5×10^6 cm^{-2}. This result differs from that in the work done by Arias et al.,[12] where a correlation between as-grown EPD and post-annealed EPD was observed. This difference could be due to the absence of multiple annealing cycles employed in their study; hence, their samples did not reach their final EPD saturation points.

While the variation in as-grown HgCdTe EPD ranged from 3×10^6 cm^{-2} to 3×10^7 cm^{-2}, the variation in the as-grown CdTe buffer layer EPD was rather large, ranging from 2.5×10^5 cm^{-2} to 3×10^7 cm^{-2}, as measured using the Everson etch[13] (not shown in Fig. 7). The EPD of a typical as-grown HgCdTe layer showed little correlation with the EPD of the as-grown CdTe buffer layer, except when the as-grown CdTe EPD was greater than mid-10^6 cm^{-2}, at which point the minimum as-grown HgCdTe EPD began to mimic the as-grown CdTe EPD. In spite of two orders of magnitude variation in the as-grown CdTe buffer layer EPD, after TCA, there was no correlation between the final HgCdTe EPD and the as-grown CdTe buffer layer EPD. As seen in Fig. 7, the results of samples such as sample no. 23, with an as-grown CdTe EPD of 1.2×10^7 cm^{-2} (not shown), showed an HgCdTe EPD reduction to the same range as that of other samples [such as 21, 22, 46, and 47, which have an as-grown CdTe buffer layer EPD of 4.6×10^5 cm^{-2} (not shown), and samples 7 through 18, which have an as-grown CdTe buffer layer EPD of 1.1×10^6 cm^{-2} (not shown)]. At this time, it is not clear what effect the TCA has on the buffer layer EPD. Based on the results of our study, it appears that the dislocation reduction by TCA occurs regardless of the origin of the dislocations, whether they nucleate from the CdTe/Si or the HgCdTe/CdTe interface.

In an effort to explore further the effect of the CdTe buffer layer on the HgCdTe EPD, we compared the results of TCA treatment on HgCdTe/CdTe/Si samples with those on HgCdTe/CdSeTe/Si samples, where a lattice-matched CdSeTe buffer layer was used instead of CdTe. The results on these layers are presented in Figs. 3 and 4. In total, five HgCdTe samples with a CdSeTe/Si composite substrate were annealed for four or more cycles and are represented by empty circles in Fig. 7. Though the samples numbered 24 through 29 in Fig. 7 exhibited some of the lowest EPDs of all the samples, the average of these five samples was 1.5×10^6 cm^{-2}, with a deviation of 1×10^6 cm^{-2}. In Fig. 3, the samples with a CdSeTe buffer layer show a trend of reduction and saturation in EPD, with respect to the number of annealing cycles, similar to that of the samples with the CdTe buffer layer. The majority of the $Hg_{1-x}Cd_xTe$ layers used in this experiment had $x \approx 0.20$, but layers with $x \approx 0.33$ and $x \approx 0.40$ were also included in our experiments. Although this was not an exhaustive study, we did not find a correlation between EPD and Cd composition.

The HgCdTe layers grown on bulk CdZnTe samples, which were subjected to annealing conditions similar to those for the HgCdTe layers grown

on the composite substrates, showed a half to one order of magnitude reduction in EPD, from 5×10^5 cm^{-2} to values as low as 5–10 $\times$ 10^4 cm^{-2}. Clearly, the pinning in EPD observed in HgCdTe/Si after TCA is not an intrinsic property of the HgCdTe crystal but is related to the substrate on which it is grown. As with the HgCdTe/Si, the HgCdTe grown on bulk CdZnTe samples showed little to no correlation between the annealing temperature and the resulting EPD. The HgCdTe on bulk CdZnTe also exhibited EPD saturation after undergoing four annealing cycles as in the case of HgCdTe/Si.

CONCLUSIONS

Thermal cycle annealing using temperatures ≥400°C has been shown to reduce effectively and reproducibly the EPD of HgCdTe/CdTe/Si samples to 1×10^6 cm^{-2}. Experimental evidence using a lattice-matched CdSeTe buffer layer on silicon gave evidence that the pinned value is substrate related and not due to an intrinsic property of HgCdTe itself or a product of its growth conditions. The reports by others that have identified a defect reduction down to $\sim 5 \times 10^5$ cm^{-2} in HgCdTe/GaAs is consistent with this hypothesis.[8,9,12] The fact that defect reduction can still be seen when bulk CdZnTe substrates are utilized shows that the defect reduction trend continues as the substrate material becomes more closely lattice matched with HgCdTe. The consistency of minimum dislocation density after TCA across different sets of experiments suggests that there is not a specific annealing parameter that can be tweaked to achieve an EPD lower than $\sim 1 \times 10^6$ cm^{-2} for the HgCdTe/CdTe/Si system. Among several parameters studied in this work, the number of annealing cycles had the greatest influence on decreasing the defect density, but this effectiveness drastically diminished after four annealing cycles.

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