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Abnormal Failure Behavior of Sn-3.5Ag Solder Bumps Under Excessive Electric Current Stressing Conditions

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Abnormal failure behavior of flip chip Sn-3.5Ag solder bumps with a Cu underbump metallurgy under excessive electric current stressing conditions is investigated with regard to electromigration lifetime characteristics and damage evolution morphologies. Abnormal behavior such as abrupt changes in the slope of the resistance versus stressing time curve correlate well with the changes in mean time to failure and the standard deviation with respect to the resistance increase ratio, which seems to be strongly related to highly accelerated electromigration test conditions of 120°C to 160°C and 3×10^4 A/cm^2 to 4.6×10^4 A/cm^2. This is closely related to changes in the damage evolution mechanism with time, even though the activation energy for electrical failure is primarily controlled by Cu diffusion through Cu-Sn intermetallic compound layers.

Key words: Electromigration, flip chip bump, Pb-free solder, Sn-3.5Ag, intermetallic compound

INTRODUCTION

Consumer demand has driven the microelectronics industry to produce products with increased performance, smaller form factor, lower cost, and more functionality, resulting in increasing chip densities and the adoption of flip chip packaging technologies. Smaller flip chip solder bump size, higher current densities, and increasing device temperatures are potential causes for electromigration-induced electrical failure of flip chip solder joints. Electromigration is defined as the movement of metal atoms in the direction of electron flow due to momentum transfer from conduction electrons to migrating metal atoms. This phenomenon has been actively investigated for over 20 years in chip interconnect materials, such as Al, Al(Cu), and Cu.[1–3] Electromigration phenomena in flip chip solder bumps are very different from those in chip interconnects due to their unique geometry and complex material structure. Several failure mechanisms are associated with solder bumps: electromigration, Joule heating, current crowding, intermetallic compound (IMC) evolution, Kirkendall voids,[4] and thermomigration.[5] Pb-free solder materials such as Sn, Sn-Ag, and Sn-Cu have been adopted as flip chip solder bump materials due to the environmental concerns associated with Pb.[6] Electroplated Sn-3.5Ag solder bumps with Cu underbump metallurgy (UBM) is the material system most widely used in the microelectronics industry. Although there are numerous publications that have investigated the electromigration phenomena of flip chip Pb-free solder bumps,[7–10] there has been little study on the relationship between bump electrical lifetime and the characteristics of their microstructural damage evolution. Understanding these two points can provide a clear picture of bump failure mechanisms and a foundation for improving the electromigration reliability of flip chip packaging. In this work, abnormal failure behaviors of flip chip Sn-3.5Ag solder bumps with a Cu UBM are investigated with regard to electromigration lifetime characteristics and damage evolution morphologies under highly accelerated electromigration test conditions.

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EXPERIMENTAL

Eutectic Sn-3.5Ag flip chip solder bumps electroplated with Cu UBM were fabricated by a conventional electroplating, reflow, and underfill flip chip bumping process as described in detail elsewhere.[11] In order to avoid an unwanted contribution of thermal stress and thermomigration effects from differences in thermal expansion coefficients and thermal conductivity, respectively, to the bump failure mechanisms between the Si chip and the plastic substrate, the same Si is used as the chip and substrate, which potentially isolates the electromigration-induced failure mechanism. Figure 1 shows a scanning electron microscope (SEM) image of a cross-sectioned flip chip Sn-3.5Ag solder bump. The interconnect and pad at the chip and substrate sides were electroplated with a Cu film, and the UBM layers were made using a sputter-deposited 0.5-μm-thick Ti/Cu bilayer and an electroplated 4-μm-thick Cu layer. The bump height, pad opening size, and solder bump diameter were 80 μm, 80 μm, and 110 μm, respectively. A scallop-shaped continuous Cu_6Sn_5 IMC was formed along the Cu and solder interfaces at both the chip and substrate sides after the reflow process. An asymmetric flip chip solder bump test structure was introduced, as shown in Fig. 2, to induce premature failure of the single solder bump on the anode side (cf. bump labelled "@" in Fig. 2) compared with three parallel bumps on the cathode side, due to large current density differences. To investigate the failure mechanism under highly accelerated test conditions, electromigration tests were performed in a conventional oven on seven samples at current densities of 3×10^4 A/cm^2, 4×10^4 A/cm^2, and 4.6×10^4 A/cm^2, and temperatures of 120°C, 140°C, and 160°C, respectively, as shown in Table I, which is selected from many other literature reports.[12–14] Here, the current density was defined as the applied current divided by the pad opening area of the Si chip. Log-normal distributions are used to characterize the statistics of electromigration time to failure (TTF), from which the mean time to failure (MTTF) and standard deviation (σ) are derived.

To characterize Joule heating under accelerated test conditions, the real-time changes in flip chip package temperature were monitored by attaching a thermocouple to the top surface of the Si chip. Differences between the chip temperature and the ambient oven temperature were measured for current densities of 3×10^4 A/cm^2, 4×10^4 A/cm^2, and 4.6×10^4 A/cm^2 at a constant oven temperature of 160°C. Joule heating was characterized as 17°C, 28°C, and 44°C for current densities of 3×10^4 A/cm^2, 4×10^4 A/cm^2, and 4.6×10^4 A/cm^2, respectively. Joule heating is proportional to the square of current density due to its proportional relationship with the electric power or the square of the current density. The electrical failure criterion was varied from a 5% to 100% increase in the initial bump resistance to investigate the effect of electromigration-induced failure criteria on the damage evolution mechanisms and lifetime parameters.

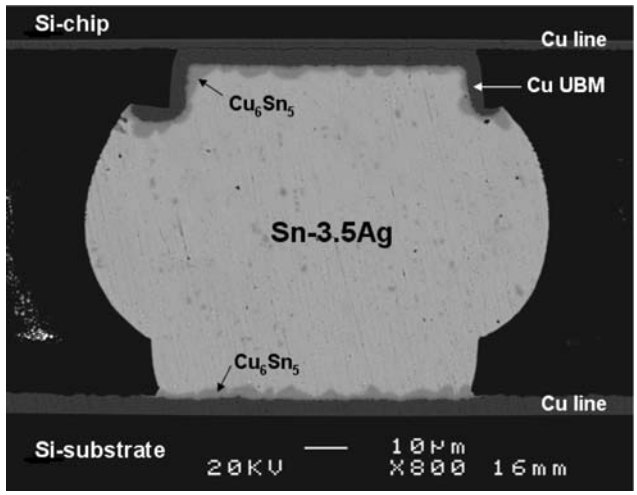

Fig. 1. SEM image of a cross-sectioned Sn-3.5Ag solder bump.

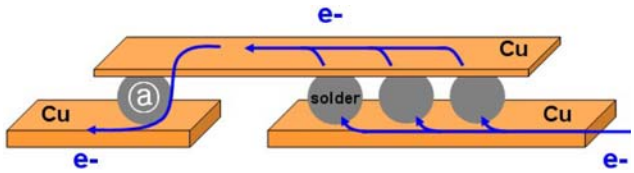

Fig. 2. Schematic diagram of the electromigration test sample structure.

Table I. Electromigration Lifetime Statistics of Sn-3.5Ag Solder Bumps with a 20% Resistance Increase Failure Criterion

Current Density (A/cm^2)	T (°C)	Joule Heating (°C)	Lifetimes (20% Resistance Increase)	
			MTTF (h)	σ
3×10^4	160	17	166.4	0.72
4×10^4	160	28.7	93.5	0.48
4.6×10^4	160	44.4	37.8	0.59
	140	39.4	67	0.44
	120	39.5	286.7	0.14

RESULTS AND DISCUSSION

Electromigration Lifetime Characteristics

The electromigration test was performed at current densities of 3×10^4 A/cm^2 to 4.6×10^4 A/cm^2 and temperatures of 120°C to 160°C. Figure 3 depicts the variation of potential as a function of testing time for seven solder bumps during an electromigration test conducted at 120°C and 4.6×10^4 A/cm^2. These solder bumps exhibit

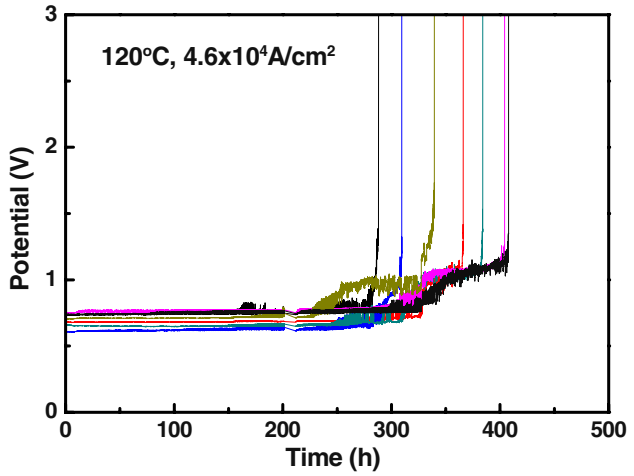

Fig. 3. Variation in potential (V) with stressing time at 120°C and 4.6×10^4 A/cm^2.

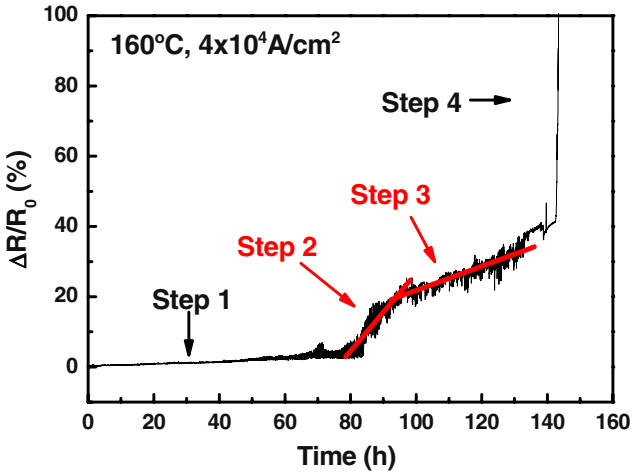

Fig. 4. Resistance change with stressing time at 160°C and 4×10^4 A/cm^2.

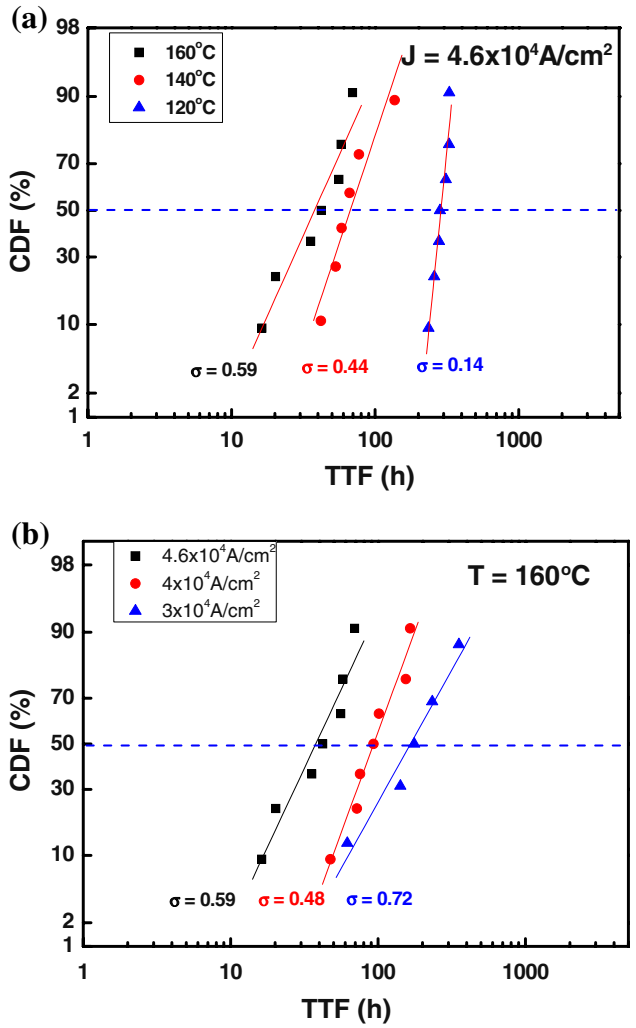

Fig. 5. CDF plots of electromigration for Sn-3.5Ag solder bump: (a) at constant current density of 4.6×10^4 A/cm^2 with varying temperatures, and (b) at constant temperature of 160°C with varying current densities.

common characteristic shapes of resistance versus time curves such as an initial slow increase and unstable increasing fluctuations in resistance, followed by an abrupt increase in resistance indicating electrical open failure of the solder bump. These characteristic behaviors are similarly found for most samples under our test conditions. To investigate these characteristics in more detail, the relative resistance is plotted as a function of testing time. This plot can be divided into four separate steps with different slopes for samples tested at 160°C and 4×10^4 A/cm^2 as shown in Fig. 4. The initial resistance value of this test structure is approximately 0.3 Ω. Step 1 shows a slow increase in resistance up to less than 5% after 80 h of stressing time. In step 2, the resistance fluctuates and increases abruptly to 20% after 100 h. Step 3 is defined as the section with a decreased slope. Steps 2 and 3 can be clearly distinguished due to their abrupt changes in slope even though they have similar fluctuation behaviors. Step 4 represents the abrupt increase in resistance due to electrical open failure of the test structure.

It is important to investigate solder bump microstructure in relation to resistance changes for the selection of a meaningful failure criterion for Pb-free flip chip solder bumps with unique UBM structure since the electromigration lifetime strongly depends on the definition of the failure criterion. Failure criterion is defined by most electromigration lifetime studies as a resistance increase between 10% and 20%. By adopting conventional failure criterion used in chip interconnects, a 20% increase in resistance is arbitrarily selected to characterize electromigration lifetime statistics, as summarized in Table I and Fig. 5. Due to high Joule heating of 17°C to 44°C under our test conditions, the impact of Joule heating should be carefully considered, not only in the electromigration activation energy calculation, but also in the

damage morphology analysis. High Joule heating is a distinctive characteristic of flip chip solder bumps due to their unique geometry,[10,15,16] while conventional chip Al and Cu interconnects show negligibly small Joule heating during typical electromigration conditions due to their simple materials and geometries.[2,3,17] The cumulative distribution function (CDF) of Sn-3.5Ag flip chip solder bump failure time is plotted in Fig. 5 for the different investigated temperatures and current densities. As can be seen from Fig. 5 and Table I, the MTTF of flip chip Sn-3.5Ag solder bump decreases as the temperature and current density increase. With the exception of the test condition of 160°C and 3×10^4 A/cm^2, lower temperature and current density result in a smaller σ, which is typical for conventional electromigration tests.[2,3,17] From the lifetime data summarized in Fig. 5 and Table I, the electromigration activation energy (E_a) and the current density exponent (n) for Sn-3.5Ag solder bump were calculated using Black's equation[18]:

$$t_{50} = Aj^{-n} \exp\left(\frac{E_a}{kT}\right), \quad (1)$$

where t_{50} is the MTTF, A is a constant, j is the current density, n is the current density exponent, E_a is the activation energy, k is the Boltzmann constant, and T is the sample temperature including Joule heating. By applying Eq. 1, the calculated E_a and n of Sn-3.5Ag solder bump are 0.92 eV and 3.2, respectively, as shown in Fig. 6. The temperature values in Fig. 6a include Joule heating to accurately measure E_a, while in Fig. 6b an additional error is included in the n value due to temperature variations between 177°C and 204°C by different Joule heating values for current density variations between 3×10^4 A/cm^2 and 4.6×10^4 A/cm^2. This high n value compared with previously reported values[12,13,19–23] implies that the electromigration test conducted in this study is highly accelerated and leads to changes in failure mode such as excessive local Joule heating inside the flip chip solder bump. Electromigration-induced electrical failure phenomena strongly depend on atomic diffusion kinetics, which is accelerated by both current density and temperature. Due to the unique geometry of flip chip solder bumps, Joule heating of the chip interconnect can be transferred to the contact edge between the conductor line and the solder bump, which generates severe current crowding around the electron-entering contact area.[10,15,16] Temperature increases of solder bump due to Joule heating can quickly approach the melting temperature of Sn-3.5Ag solder, as seen in Table I. These high Joule heating contributions lead to a large current density dependency; that is, the increasing current density accelerates solder atomic diffusion and leads to local melting and a much shorter failure time. The activation energy obtained in this work will be discussed in the following section.

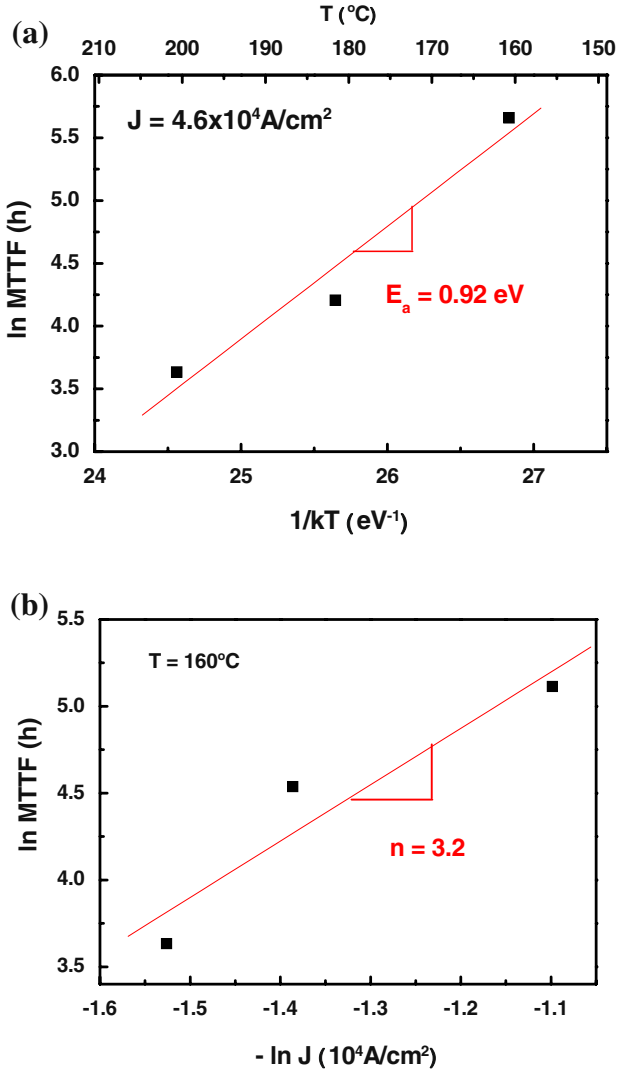

Fig. 6. (a) Activation energy (E_a), and (b) current density exponent (n) of Sn-3.5Ag solder bump electromigration.

Abnormal Electromigration Behaviors

As previously mentioned, electromigration phenomena in flip chip solder bumps are more complex than those in chip interconnects due to their unique geometry and complex material structure. They show several failure mechanisms such as electromigration, Joule heating, current crowding, and IMC evolution or decomposition. Therefore, solder bump failure criteria should be cautiously defined with respect to their complex changes in damaged microstructures. The electrical failure criterion varies from a 5% to 100% increase in the initial electrical resistance in order to investigate its effect on the changes of electromigration lifetime parameters and damage morphologies, as can be seen from Figs. 7–9. The effect of resistance increase ratio on the electromigration failure parameters is shown in Fig. 7 for 160°C and a current density of 4×10^4 A/cm^2. A log-normal distribution fits most

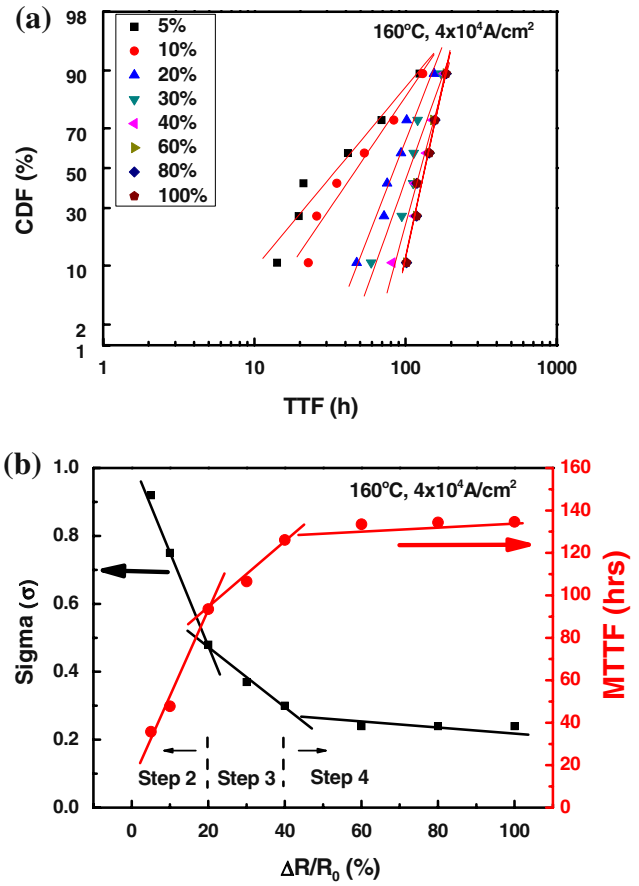

Fig. 7. (a) Electromigration lifetimes distribution, and (b) log-normal standard deviation (σ) and MTTF as a function of resistance increase ratio for 160°C and 4×10^4 A/cm^2.

of the data for different ratios of resistance increase. There are three distinct steps, with different slopes of MTTF versus resistance increase ratio (%), as can be seen in Fig. 7b. These steps consist of an initial stage with a large increasing slope up to 20%, a transition stage with a smaller increasing slope up to 40%, followed by a saturation stage with more than a 40% increase in resistance. Interestingly, the standard deviation distribution shows good correlation with the MTTF distribution, wherein the σ decreases up to 20% in the initial stage, decreases by 40% in the transition stage, followed by a saturation stage with more than a 40% increase in resistance. By comparing Fig. 7b with Fig. 4, the resistance change steps correspond exactly with the steps in MTTF and σ. Steps 2 and 3, with a large fluctuating resistance increase between 40% and 50%, show a large σ, while step 4, with an abrupt 40% increase in resistance, shows a saturated MTTF and σ due to an electrical open failure of the test structure. Overall, the MTTF increases from 36 h to 135 h, while the σ decreases from 0.92 to 0.24, for variations in the resistance increase ratio of 5% to 100%. It is not clear at this moment why these abnormal behaviors such as the existence of four clear different steps and the clear resistance dependence of MTTF and σ are exhibited in our samples. Even though the fundamental mechanism and controlling factors should be clarified in our future work, this result seems to be strongly related to our excessive electrical current stressing conditions.

An increasing MTTF coincident with the resistance increase ratio is logical, since more time is needed to reach a larger resistance value during the electromigration test. An opposite trend for σ implies the change from a multiple to a single failure mode with increasing resistance. A large σ for the initial resistance increase step is most likely a result of sample-to-sample geometry variations and electric-current-induced atomic migration due to Joule heating, current crowding, and IMC evolution or decomposition, which is defined as a multiple mode failure. A single failure mode occurs via an electrical open failure at the chip interconnect near the solder bump when the resistance is increased by over 40%. This is the final stage that results from the previous multiple damage evolution kinetics. This argument supports the saturation behavior of both the MTTF and σ.

In order to understand the effect of electromigration failure criteria on the damage evolution mechanism of flip chip Sn-3.5Ag solder bumps, the cross-sectional microstructures of solder bumps in Fig. 2 were observed at 160°C and 3×10^4 A/cm^2 for each resistance increase ratio when electrons flow from the chip to the substrate, as shown in Fig. 8. Before the test, scallop-shaped Cu_6Sn_5 IMC was formed symmetrically along the Cu/solder interfaces at both the chip and substrate sides after the reflow process, as can be seen in Fig. 1. Figure 8a shows the solder microstructure after a 5% increase in resistance ratio, which is the upper limit of step 1 in Fig. 4. On the chip side, the Cu UBM and Cu-Sn IMCs disappeared and were replaced by Sn. The Cu-Sn IMC thickness doubled at the substrate side. This asymmetric IMC growth seems to result from the well-known IMC polarity effect,[12,13,19–24] which creates an electron pushing force that drives Cu atoms to migrate with the electron flow from the chip, as shown in Fig. 8a. Step 1 is related to the dissolution of the chip-side Cu UBM and Cu-Sn IMC and the thickening of the substrate-side Cu-Sn IMC due to a polarity effect. The Cu pad regions on both sides remain unreacted. These microstructural changes are responsible for the slow and small increase in electrical resistance up to 5%. Figure 8b and c show the cross-sectioned solder microstructures when the resistance increase ratios reached 10% and 20%, corresponding to stage 2 in Fig. 4. Before the increase in resistance reached 10%, half of the solder area at the substrate side was transformed to Cu_6Sn_5 IMC with little IMC formation on the remaining area of the chip side. Further, the Cu substrate pad slightly dissolves while a large number of the Cu atoms in the chip pad around the solder bump are exchanged for Sn atoms.

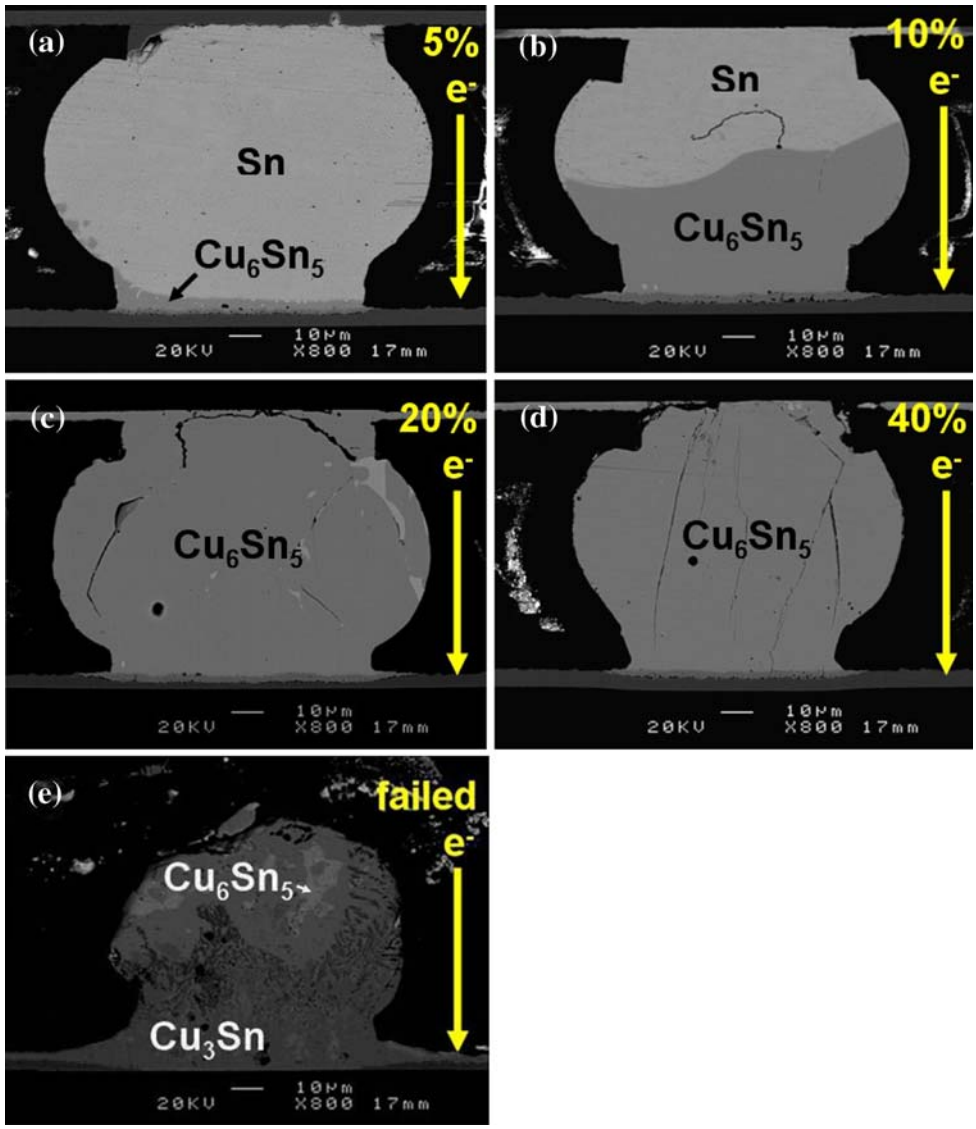

Fig. 8. SEM image of cross-sectioned solder bump in Fig. 2 for 160°C and 4 × 10^4 A/cm^2 with resistance increase ratio of: (a) 5%, (b) 10%, (c) 20%, (d) 40%, and (e) failure.

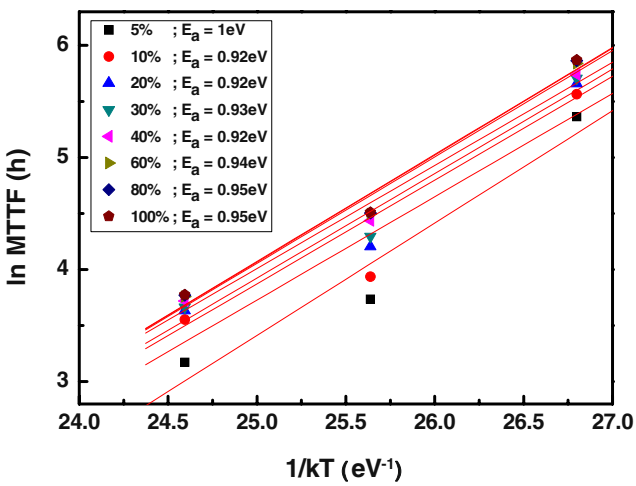

Fig. 9. Activation energy (E_a) as a function of resistance increase ratio.

The highly accelerated stressing condition used in this work generates a large amount of Joule heating, which accelerates the diffusion of Cu atoms in the Sn matrix to form large amounts of Cu_6Sn_5 IMC on the substrate side. It is interesting to note that the IMC polarity effect still dominates at stage 2, as can be seen in Fig. 8b, while longer test times lead to the complete transformation of solder volume into Cu_6Sn_5 IMC with a subsequent 20% increase in resistance, as shown in Fig. 8c. The substrate Cu pad is still resistive to IMC formation, but the chip pad near the solder bump is also converted to Cu-Sn IMC. Therefore, intermediate steps 2 and 3 represent multiple mode failures, wherein several reactions such as Cu dissolution at the chip pad, Sn diffusion to the chip pad, and IMC formation at the solder bulk and chip pad area occur compatibly without dominance of any specific mechanism.

These multiple mode failures could be responsible for the large σ and resistance fluctuations depicted in Figs. 7b and 4, respectively. Figure 8d shows critical voids at the contact region between the solder bump and the chip-side Cu line for a resistance increase of 40% with little change to the substrate pad side. This led to an abrupt resistance increase, as shown in step 4 in Fig. 4. Finally, local melting occurs on the chip side of the solder bump due to severe current crowding and Joule heating, as shown in Fig. 8e. A high temperature at the solder bump itself seems to be responsible for the phase transformation of Cu_6Sn_5 into Cu_3Sn, which should be clarified in further work. Some reports in the literature demonstrate a minor increase in resistance prior to the abrupt resistance increase at open failure for eutectic solder bump, which can be considered a dominant, void nucleation mechanism.[16,19,20]

Figure 9 shows the change in activation energy as a function of the increasing resistance ratio. Although there are significant resistance ratio variations from 5% to 100%, the activation energy maintains a constant value of 0.94 eV, with the exception of when the resistance ratio is 5%. Reported values for activation energy of IMC growth in Cu-Sn systems are 0.9 eV to 1 eV,[12,13,19–23] which are comparable to the activation energy obtained in this study. Even if various reaction and diffusion mechanisms occur simultaneously during current stressing, the dominant mechanism is identified as interfacial void formation after excessive Cu-Sn IMC growth in the solder joint accelerated by severe Joule heating.[9,10,14–16] Thus, a more developed understanding of electromigration characteristics of Pb-free flip chip solder bumps can be obtained by correlating the microstructural evolution with electrical characteristics during electromigration studies, which can help to define meaningful failure criteria of new interconnect systems to more accurately and reliably assess electromigration lifetimes.

CONCLUSIONS

Abnormal electromigration characteristics of Sn-3.5Ag flip chip solder bumps using Cu UBM were investigated under highly accelerated test conditions in order to understand the relationship between the electrical resistance behaviors and the electromigration lifetime parameters and bump microstructural evolution.

Abnormal changes in the slope of the resistance versus stressing time curve correlate well with the changes in mean time to failure and the standard deviation with respect to the resistance increase ratio at highly accelerated electromigration test conditions, which are closely related to the changes in the dominant damage evolution mechanism with time. In spite of various reaction and diffusion mechanisms being competitively involved, such as Cu UBM and pad dissolution into the solder, Sn diffusion into chip pad, and extensive Cu-Sn IMC growth, the dominant failure mechanism seems to be interfacial void formation after excessive Cu-Sn IMC growth in the solder joint under excessive electric current stressing conditions.

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