Journal of ELECTRONIC MATERIALS, Vol. 37, No. 10, 2008
DOI: 10.1007/s11664-008-0515-3

Regular Issue Paper

Electromigration Reliability and Morphologies of Cu Pillar Flip-Chip Solder Joints with Cu Substrate Pad Metallization

YI-SHAO LAI,[1,2] YING-TA CHIU,[1] and JIUNN CHEN[1]

1.—Central Labs, Advanced Semiconductor Engineering, Inc., 26 Chin 3rd Road, Nantze Export Processing Zone, Kaohsiung 811, Taiwan. 2.—e-mail: yishao_lai@aseglobal.com

The Cu pillar is a thick underbump metallurgy (UBM) structure developed to alleviate current crowding in a flip-chip solder joint under operating conditions. We present in this work an examination of the electromigration reliability and morphologies of Cu pillar flip-chip solder joints formed by joining Ti/Cu/Ni UBM with largely elongated ~62 μm Cu onto Cu substrate pad metallization using the Sn-3Ag-0.5Cu solder alloy. Three test conditions that controlled average current densities in solder joints and ambient temperatures were considered: 10 kA/cm^2 at 150°C, 10 kA/cm^2 at 160°C, and 15 kA/cm^2 at 125°C. Electromigration reliability of this particular solder joint turns out to be greatly enhanced compared to a conventional solder joint with a thin-film-stack UBM. Cross-sectional examinations of solder joints upon failure indicate that cracks formed in $(Cu,Ni)_6Sn_5$ or Cu_6Sn_5 intermetallic compounds (IMCs) near the cathode side of the solder joint. Moreover, the ~52-μm-thick Sn-Ag-Cu solder after long-term current stressing has turned into a combination of ~80% Cu-Ni-Sn IMC and ~20% Sn-rich phases, which appeared in the form of large aggregates that in general were distributed on the cathode side of the solder joint.

Key words: Flip chip, Cu pillar, electromigration, solder joint, reliability

INTRODUCTION

The implementation of Pb-free solder alloys in a flip-chip package has recently become a topic of interest in the electronic packaging industry, for which the durability of these solder joints under high-current stressing represents one of the major reliability concerns.[1] Favorable Pb-free solder alloys fall into two categories, namely, the Sn-Ag and Sn-Ag-Cu families. Both show the advantages of good processability and high reliability. The Sn-Ag-Cu family in particular has become the most favored as a substitute for conventional Sn-Pb solders in recent years.

Several studies have addressed the electromigration issue of Sn-Ag-Cu flip-chip solder joints (e.g., Refs. 2–7). Similar to Sn-Pb solder joints, the high current density induced by current crowding (e.g., Refs. 8–11) around the thin-film-stack underbump metallurgy (UBM) at the chip side has been identified as a crucial driving force responsible for the failure of these solder joints.[5–7] In response to this critical and general electromigration-induced failure in flip-chip solder joints, the thick Cu pillar UBM has been proposed to alleviate current crowding and consumption of UBM as well.[12,13] The Cu pillar UBM structure also allows fine-pitch and high-density input/outputs (I/Os); nevertheless, the thermomechanical and mechanical reliability of solder joints with this particular UBM structure still remains an open issue.

In this work, we present electromigration reliability and morphologies of flip-chip solder joints formed by joining Ti/Cu/Ni UBM with largely elongated ~62 μm Cu onto Cu substrate pad metallization using the Sn-3Ag-0.5Cu solder alloy. Three test conditions that controlled average current densities in solder joints and ambient temperatures were considered: 10 kA/cm^2 at 150°C, 10 kA/cm^2 at

(Received February 29, 2008; accepted June 10, 2008; published online July 2, 2008)

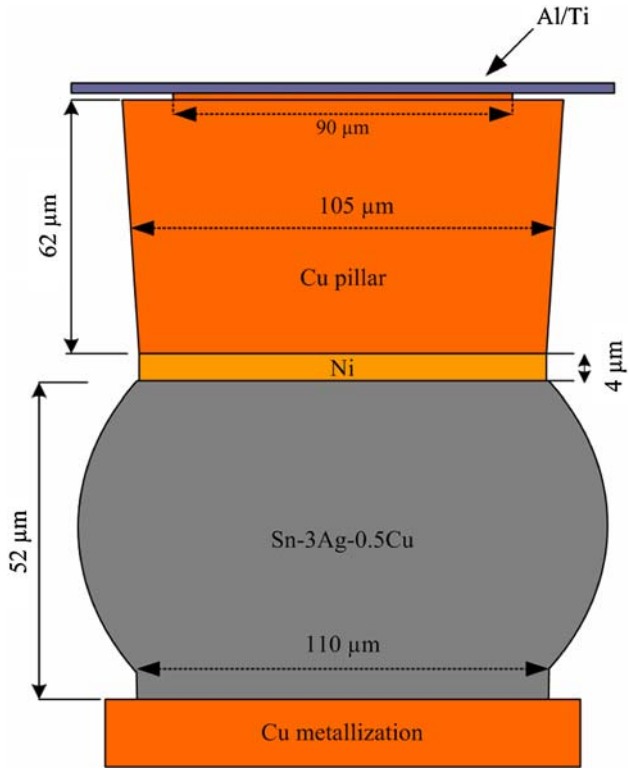

Fig. 1. Schematic of a Cu pillar solder joint.

160°C, and 15 kA/cm^2 at 125°C. Energy-dispersive x-ray spectroscopy (EDS) was employed to identify microstructural compositions on cross-sectioned solder joints upon failure.

ELECTROMIGRATION EXPERIMENTS

The test vehicle employed in electromigration experiments was a 27 mm × 27 mm × 1.39 mm flip-chip package, which involves a 7.62 mm × 7.62 mm × 0.73 mm silicon chip interconnected to a 0.56-mm-thick substrate with 720 solder joints in the soldermask-defined configuration. The pitch between adjacent solder joints is 270 μm. In the present case, the Cu pillar UBM is a Ti/Cu/Ni tri-layer metallization stack with a largely elongated Cu layer. As shown schematically in Fig. 1, the diameter and passivation opening of the Cu pillar UBM were 105 μm and 90 μm, respectively. The tip of the ~62-μm-thick plated Cu pillar was coated subsequently with a ~4-μm-thick Ni layer and the Sn-3Ag-0.5Cu solder alloy, which was then reflowed to form a solder bump. The solder joint was formed by joining the Cu pillar UBM along with the solder bump onto a ~25-μm-thick Cu substrate pad metallization with a soldermask opening of ~110 μm. The substrate pad metallization features the solder on pad (SOP) surface treatment, i.e., with printed Sn-3Ag-0.5Cu presolder on the pad surface. The Sn-Ag-Cu solder in the Cu pillar solder joint was ~52 μm thick.

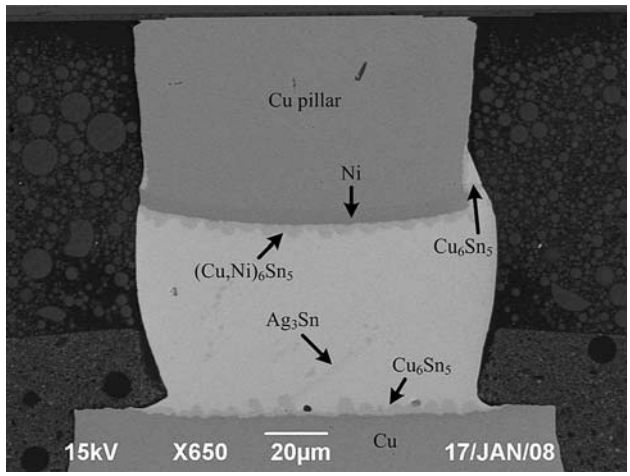

Fig. 2. Cross-sectional view of an as-assembled Cu pillar solder joint.

The cross-sectional view of an as-assembled Cu pillar solder joint is shown in Fig. 2. Microstructures within the solder joint included $(Cu,Ni)_6Sn_5$ intermetallic compound (IMC), Cu_6Sn_5 IMC, Ag_3Sn IMC, and the nearly pure Sn matrix. Due to the presence of the Ni diffusion-barrier layer, $(Cu,Ni)_6Sn_5$ was formed on the interface between Ni and the solder on the UBM side. Plate-type Ag_3Sn and scallop-type Cu_6Sn_5 were observed near the interface between the solder and Cu substrate pad metallization. A few Cu_6Sn_5 phases formed near the brim of the Cu pillar in contact with the solder. From the figure, it is apparent that the presence of Ag_3Sn depressed the formation of Cu_6Sn_5,[14] and therefore the structure of $(Cu,Ni)_6Sn_5$ on the UBM side was more compact than that of Cu_6Sn_5 on the substrate side, in particular at the location beneath the Ag_3Sn plate. Moreover, we have observed that the Ag_3Sn plate formed exclusively near the substrate side whereas none was observed near the UBM side. This may be attributed to the different cooling rates around the UBM and substrate sides of the solder joint upon solidification, but at present we are unable to identify the cause with certainty.

Figure 3 shows the layout of circuits and joints on the flip-chip test vehicle. Only a single daisy chain at the edge of the chip on the encompassed region shown in Fig. 3 was electrified with a constant direct-current (DC) electric current. Figure 4 shows the configuration of this particular electrified daisy chain and the directions of DC current and electron flow, which are opposite from each other. Note that in V1+ and V2+ joints, electrons flow from the UBM to the substrate while in V1− and V3− joints they flow from the substrate to the UBM. The current bypasses the V2−/V3+ joint on the chip side. Individual electrical resistances on the three sections labeled R_1, R_2, and R_3 were monitored *in situ*, and the experiments were terminated once the resistance of each of these three sections exceeded

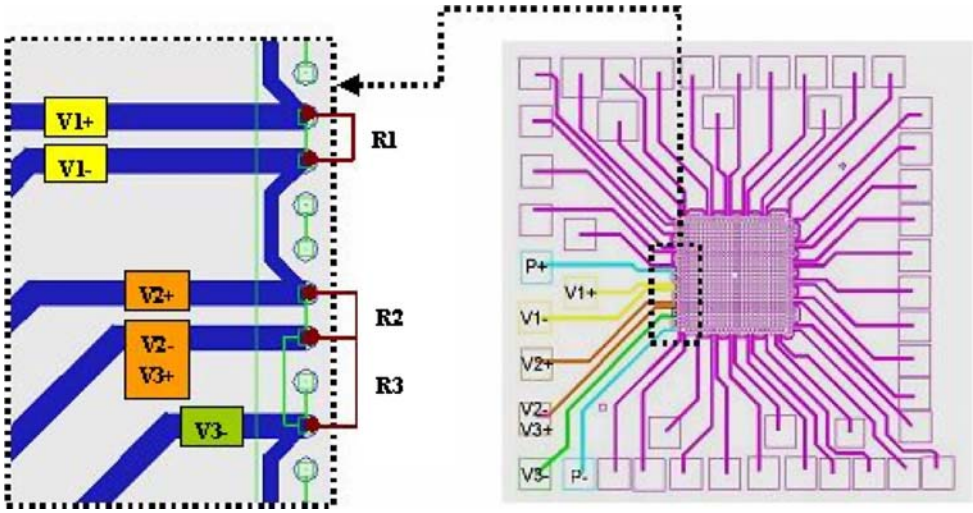

Fig. 3. Layout of circuits and joints.

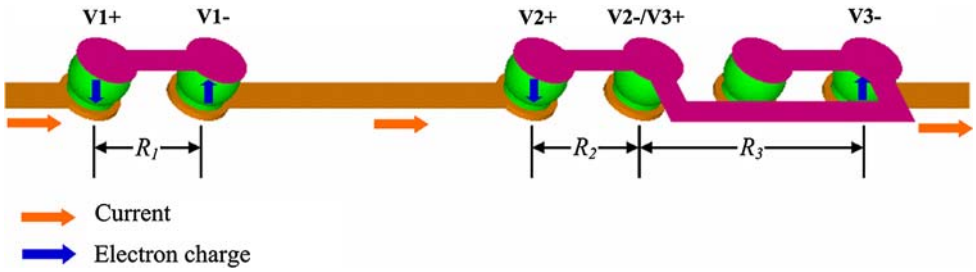

Fig. 4. Electrified daisy chain and directions of DC current and electron flow.

2 Ω.[5–7,15,16] Our experience shows that this failure criterion refers to the open-circuit failure rather than the failure corresponding to partial defects in the solder joint system, formed during current stressing.

Test vehicles were placed in a furnace to control the ambient temperature. In this work, we consider three test conditions with different average current densities in solder joints and ambient temperatures: 10 kA/cm^2 at 150°C, 10 kA/cm^2 at 160°C, and 15 kA/cm^2 at 125°C. The average current densities were calculated using the passivation opening area as a reference. In the present case, 10 kA/cm^2 and 15 kA/cm^2 refer to constant DC current stressing of 0.64 A and 0.96 A, respectively. For each of the three test conditions, 22 samples were prepared.

ELECTROMIGRATION RELIABILITY AND MORPHOLOGIES

Weibull cumulative distributions for electromigration reliability of Cu pillar flip-chip test vehicles under the three test conditions are shown in Fig. 5. Statistical characteristics are summarized in Table I, in which *ff* stands for the stressing duration until the first sample failed, η represents the characteristic life from the Weibull cumulative distribution, indicating that 63.2% of the population fails, and β refers to the Weibull slope. Though not directly comparable with previously published reliability characteristics of conventional solder joints with thin-film-stack UBM[5–7,15–17] because the test

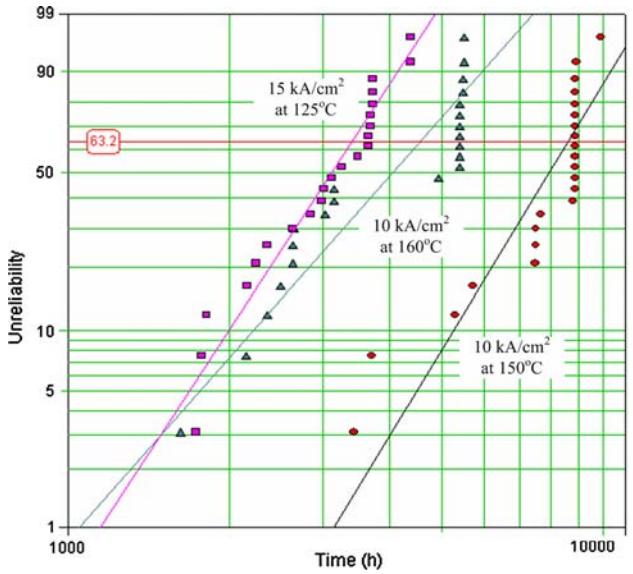

Fig. 5. Weibull cumulative distributions for electromigration reliability of Cu pillar solder joints.

Table I. Electromigration Reliability

	10 kA/cm^2 at 150°C	10 kA/cm^2 at 160°C	15 kA/cm^2 at 125°C
ff (h)	3428	1624	1736
η (h)	8591	4557	3387
β	4.57	3.14	4.26

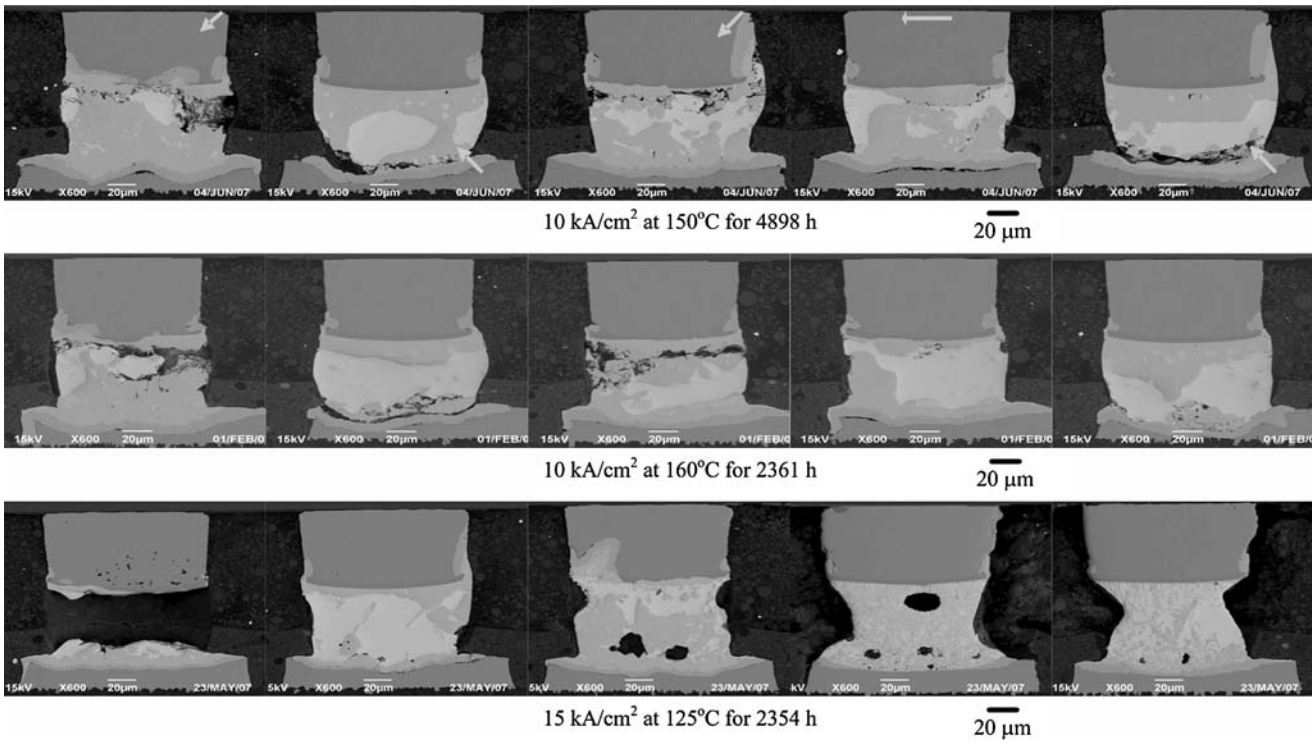

Fig. 6. Morphologies of current-stressed Cu pillar solder joints upon failure. Left to right: V1+, V1−, V2+, V2−/V3+, and V3− joints; arrows indicate the flow directions of electrons.

conditions are different, Cu pillar solder joints indeed exhibit extraordinary resistance to current stressing.

Figure 6 features morphologies of current-stressed Cu pillar solder joints upon failure. Close-up examination of individual solder joints in Fig. 6 are shown in Figs. 7–11. It is clear from Fig. 6 that the Cu pillar is quite intact without significant damage or consumption after long-term current stressing, except at its brim in contact with the solder. For the two test conditions with an average current density of 10 kA/cm^2, cracks were observed in $(Cu,Ni)_6Sn_5$ or Cu_6Sn_5 near the cathode side of the solder joint, as shown in Figs. 7b, 8b, and 9b. This is different from the conventional solder joints with the thin-film-stack UBM, in which the UBM itself tends to be the weakest among the components under current stressing.

Microstructural observations of IMCs indicate that the Ag_3Sn phase near the substrate side in the as-assembled solder joint (Fig. 2) has decomposed after current stressing. Furthermore, thick Cu_3Sn layers were present on the substrate side after long-term current stressing. This indicates that the consumption rate of the Cu substrate pad metallization is greater than that of the Cu pillar, on which the Ni layer serves as a diffusion barrier. The Ni layer itself has apparently been consumed in the solder joints, where electrons flow from the UBM to the substrate (V1+ and V2+ joints), as can be identified by the discontinuous Ni layer in Figs. 8b and 9b. On the other hand, in the solder joints where electrons flow from the substrate to the UBM (V1− and V3− joints) and the one where electrons bypass on the chip side (V2−/V3+ joint), the Ni layer does not seem to be consumed. The different consumption tendencies of Ni on the UBM side with respect to the flow direction of electrons indicates that Ni migrates along with the electrons.

It is particularly interesting to note from Fig. 8b that Cu_3Sn phases closely attached to the Cu pillar, $(Cu,Ni)_6Sn_5$, and Ni at the location where Ni was

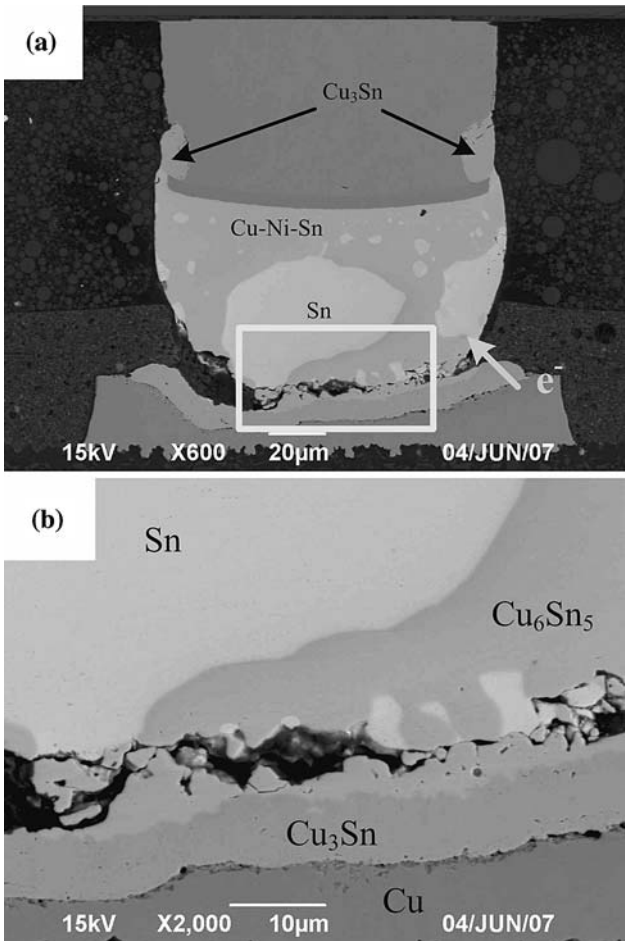

Fig. 7. (a) V3− joint under 10 kA/cm^2 at 150°C for 4898 h; (b) close-up view of encompassed region in (a).

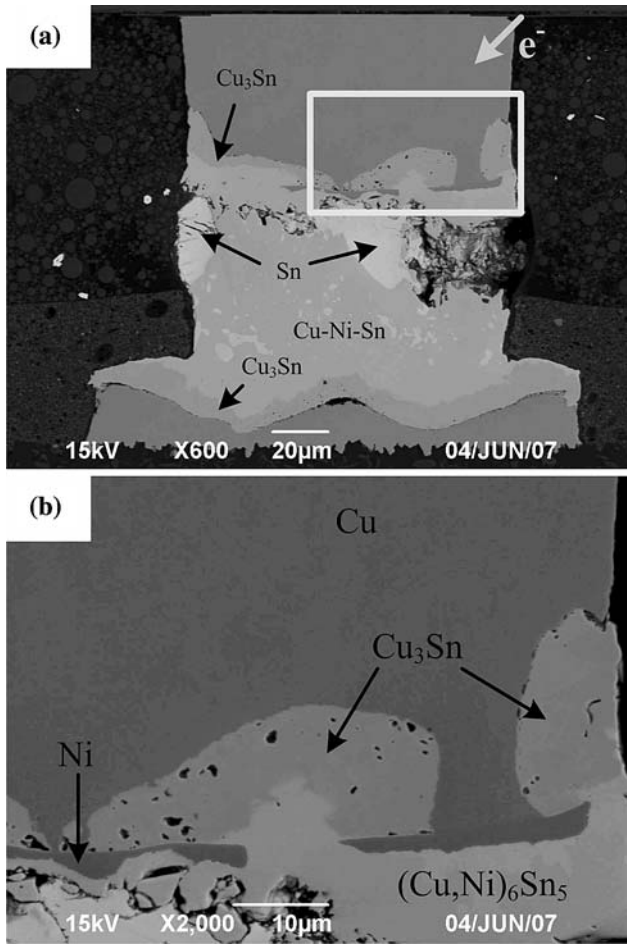

Fig. 8. (a) V1+ joint under 10 kA/cm^2 at 150°C for 4898 h; (b) close-up view of encompassed region in (a).

completely consumed. Upon penetration of the Ni layer, $(Cu,Ni)_6Sn_5$ would form first at the penetrated sites. Yu et al.[18] proposed that $(Cu,Ni)_6Sn_5$ may share a monoclinic lattice structure similar to that of Cu_6Sn_5, which is considered to be structurally unstable compared to the face-centered cubic (FCC) close-packed lattice structure of Cu_3Sn.[19] It is well known that η-Cu_6Sn_5 undergoes a transformation into ε-Cu_3Sn by the requirement of thermodynamic equilibrium in conventional Sn-Pb solder systems. Although to the best of our knowledge, theoretical calculations on the thermodynamics of ternary Sn-Ag-Cu solder systems are currently unavailable, similar formation kinetics may also account for the observed Cu_3Sn in Fig. 8b. This is also evidenced by the transformation of Cu_6Sn_5 (Fig. 2) into Cu_3Sn (Figs. 7a and 9b) on the brim of the Cu pillar after long-term current stressing. Furthermore, Cu_3Sn is a long-period superlattice (LPS) alloy with periodic antiphase domains similar to Cu_3Au. For the LPS, a definite relationship between the electron-atom ratio and the period of the antiphase was obtained from various experiments,[20,21] and therefore the appearance of Ni in the Cu_3Sn lattice structure is strongly disputable from the microscopic point of view. Moreover, since Ni migrates with the electrons, the Cu_3Sn phase located behind the Ni layer in Fig. 8b would have a small tendency to incorporate Ni.

From the figures, it is noted that the Sn-Ag-Cu solder in the Cu pillar solder joint after long-term current stressing has turned into a combination of ~80% Cu-Ni-Sn IMC and ~20% Sn-rich phases. The Sn-rich phases appeared in the form of large aggregates that in general were distributed on the cathode side of the solder joint. The continuous formation of Cu-Ni-Sn IMC is clearly a result of continuous Cu supply from the Cu substrate pad metallization and Cu pillar, after the Ni has been consumed. The preferable distribution of Sn-rich phases on the cathode side may be attributed to the back stress induced by electromigration,[7,22] whereas the formation of large aggregates of Sn-rich phases should be a result of long-term current stressing.

As depicted in Figs. 10 and 11, under 15 kA/cm^2 at 125°C for 2354 h, the solder between the Cu pillar and substrate pad metallization in certain solder

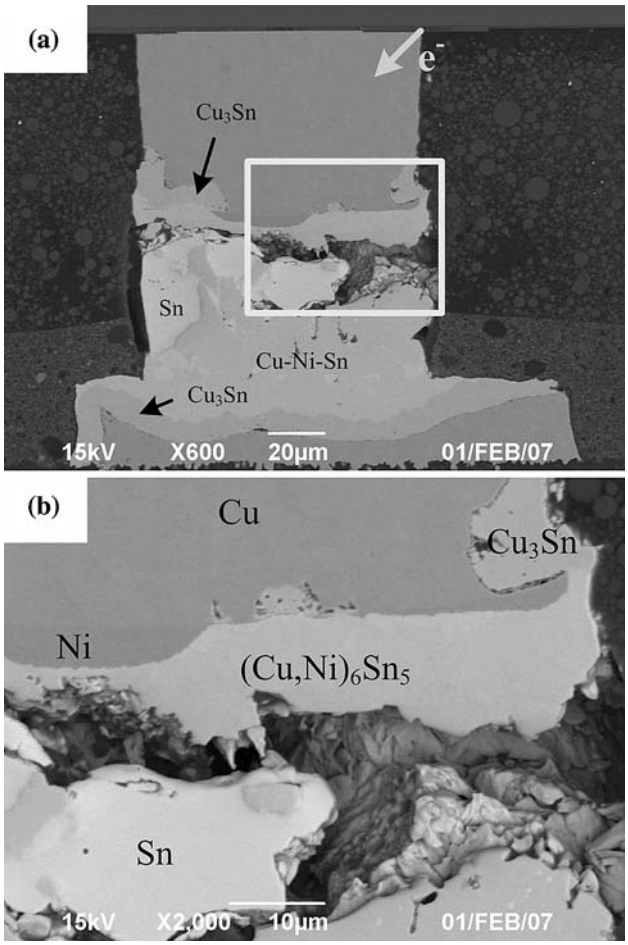

Fig. 9. (a) V1+ joint under 10 kA/cm^2 at 160°C for 2361 h; (b) close-up view of encompassed region in (a).

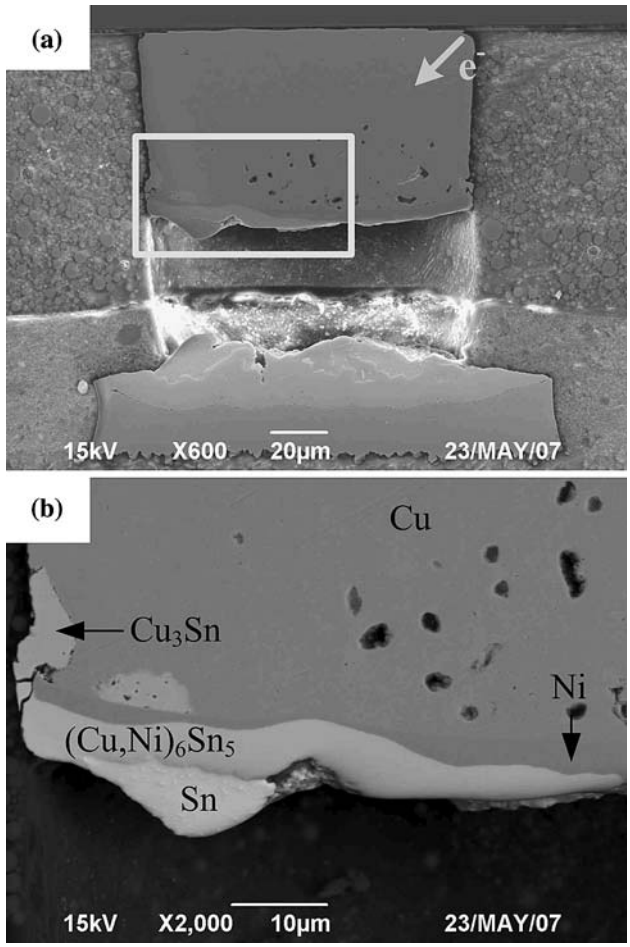

Fig. 10. (a) V1+ joint under 15 kA/cm^2 at 125°C for 2354 h; (b) close-up view of encompassed region in (a).

joints has shrunk or disappeared. Although this is not a particularly uncommon phenomenon for flip-chip solder joints subjected to a severe current stressing condition,[16,23–25] the mechanism responsible for the complete or partial disappearance of the solder as well as where and how the solder migrates within the solder joint system do require further identification. As shown in Fig. 11b, in the shrunken solder joint, the Cu_3Sn layer, within which Kirkendall voids were observable, was on top of the Cu substrate pad metallization. Moreover, large voids and Cu_6Sn_5 dendrites were seen to spread in the nearly pure Sn matrix. These features indicate that the solder has experienced extremely severe reactions, which may involve melting of the solder, under this particular current stressing condition.

CONCLUSIONS

We present in this work electromigration reliability and morphologies of Cu pillar flip-chip solder joints formed by joining Ti/Cu/Ni UBM with largely elongated ~62 μm Cu onto Cu substrate pad metallization using the Sn-3Ag-0.5Cu solder alloy. Three test conditions that controlled average current densities in solder joints and ambient temperatures were considered: 10 kA/cm^2 at 150°C, 10 kA/cm^2 at 160°C, and 15 kA/cm^2 at 125°C. Electromigration reliability of this particular solder joint turns out to be greatly enhanced compared with a conventional solder joint with thin-film-stack UBM.

Cross-sectional examinations of solder joints upon failure indicate that cracks formed in $(Cu,Ni)_6Sn_5$ or Cu_6Sn_5 IMCs near the cathode side of the solder joint. Moreover, the ~52-μm-thick Sn-Ag-Cu solder after long-term current stressing has turned into a combination of ~80% Cu-Ni-Sn IMC and ~20% Sn-rich phases, which appeared in the form of large aggregates that in general were distributed on the cathode side of the solder joint. The preferable distribution of Sn-rich phases on the cathode side may be attributed to the back stress induced by electromigration, while the formation of large aggregates of Sn-rich phases should be a result of long-term current stressing.

Under the severe current stressing condition of 15 kA/cm^2 at 125°C, the solder between the Cu

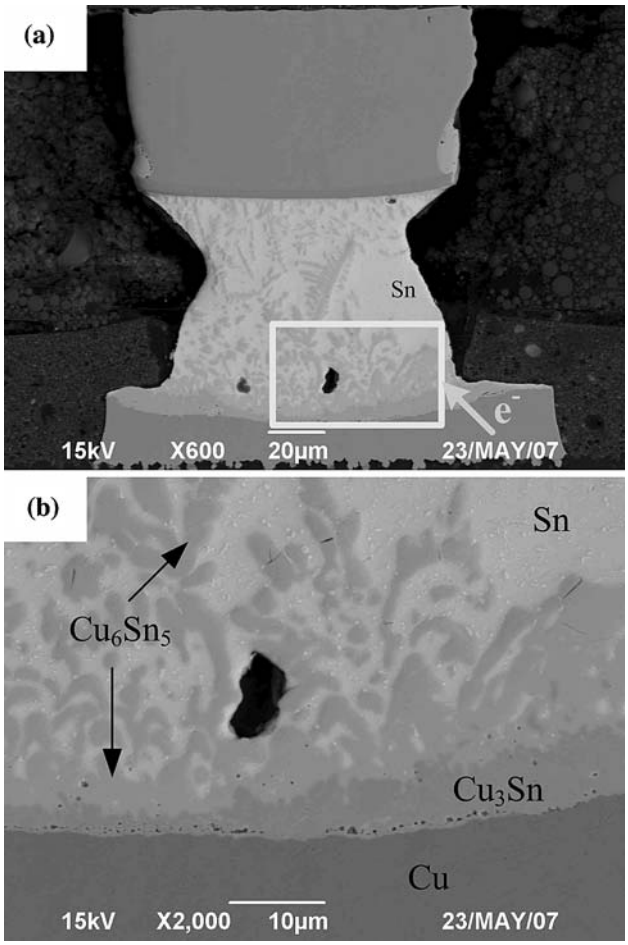

Fig. 11. (a) V3– joint under 15 kA/cm^2 at 125°C for 2354 h; (b) close-up view of encompassed region in (a).

pillar and substrate pad metallization in certain solder joints has shrunk or disappeared. Large voids and Cu_6Sn_5 dendrites were seen to spread in the nearly pure Sn matrix of the shrunken solder joints.

ACKNOWLEDGEMENT

The authors are grateful to their colleagues, Yu-Hsiu Shao and Chiu-Wen Lee, for experimental support.

REFERENCES

1. K.N. Tu, *J. Appl. Phys.* 94, 5451 (2003). doi:10.1063/1.1611263.
2. T.Y. Lee, K.N. Tu, and D.R. Frear, *J. Appl. Phys.* 90, 4502 (2001). doi:10.1063/1.1400096.
3. L. Zhang, S. Ou, J. Huang, K.N. Tu, S. Gee, and L. Nguyen, *Appl. Phys. Lett.* 89, 012106 (2006). doi:10.1063/1.2158702.
4. L. Xu, J.H.L. Pang, and K.N. Tu, *Appl. Phys. Lett.* 89, 221909 (2006). doi:10.1063/1.2397549.
5. Y.-S. Lai, C.-W. Lee, and C.-L. Kao, *J. Electron. Packag.* 129, 56 (2007). doi:10.1115/1.2429710.
6. Y.-S. Lai, K.-M. Chen, C.-L. Kao, C.-W. Lee, and Y.-T. Chiu, *Microelectron. Reliab.* 47, 1273 (2007). doi:10.1016/j.microrel.2006.09.023.
7. Y.-S. Lai and Y.-T. Chiu, *J. Electron Packag.* (in press).
8. K.N. Tu, C.C. Yeh, and C.Y. Liu, *C. Chen. Appl. Phys. Lett.* 76, 988 (2000). doi:10.1063/1.125915.
9. W.J. Choi, E.C.C. Yeh, and K.N. Tu, *J. Appl. Phys.* 94, 5665 (2003). doi:10.1063/1.1616993.
10. S.W. Liang, T.L. Shao, C. Chen, E.C.C. Yeh, and K.N. Tu, *J. Mater. Res.* 21, 137 (2006). doi:10.1557/jmr.2006.0004.
11. Y.-S. Lai and C.-L. Kao, *Microelectron. Reliab.* 46, 915 (2006). doi:10.1016/j.microrel.2005.02.007.
12. Y.-S. Lai and C.-L. Kao, *Microelectron. Reliab.* 46, 1357 (2006). doi:10.1016/j.microrel.2005.08.009.
13. J.-W. Nah, J.O. Suh, K.N. Tu, S.W. Yoon, V.S. Rao, V. Kripesh et al., *J. Appl. Phys.* 100, 123513 (2006). doi:10.1063/1.2402475.
14. S.K. Kang, W.K. Choi, Y. Shih, D.W. Henderson, T. Gosselin, A. Sarkhel et al., *JOM* 55, 61 (2003). doi:10.1007/s11837-003-0143-6.
15. J.D. Wu, P.J. Zheng, C.W. Lee, S.C. Hung, and J.J. Lee, *Microelectron. Reliab.* 46, 41 (2006). doi:10.1016/j.microrel.2005.01.012.
16. Y.-S. Lai and C.-W. Lee, *IEEE Trans. Compon. Packag. Tech.* 30, 526 (2007). doi:10.1109/TCAPT.2007.898681.
17. Y.-S. Lai and C.-L. Kao, *J. Electron. Mater.* 35, 972 (2006). doi:10.1007/BF02692556.
18. C. Yu, J. Liu, H. Lu, P. Li, and J. Chen, *Intermetallics* 15, 1471 (2007). doi:10.1016/j.intermet.2007.05.005.
19. J. Chen, Y.-S. Lai, C.-Y. Ren, and D.-J. Huang, *Appl. Phys. Lett.* 92, 081901 (2008). doi:10.1063/1.2884685.
20. H. Sato and R.S. Toth, *Phys. Rev.* 124, 1833 (1961). doi:10.1103/PhysRev.124.1833.
21. H. Sato and R.S. Toth, *Phys. Rev.* 127, 469 (1962). doi:10.1103/PhysRev.127.469.
22. C.Y. Liu, J.T. Chen, Y.C. Chuang, L. Ke, and S.J. Wang, *Appl. Phys. Lett.* 90, 112114 (2007). doi:10.1063/1.2714100.
23. A.T. Huang, K.N. Tu, and Y.-S. Lai, *J. Appl. Phys.* 100, 033512 (2006). doi:10.1063/1.2227621.
24. C.M. Tsai, Y.L. Lin, J.Y. Tsai, Y.-S. Lai, and C.R. Kao, *J. Electron. Mater.* 35, 1005 (2006). doi:10.1007/BF02692560.
25. F.-Y. Ouyang, K.N. Tu, C.-L. Kao, and Y.-S. Lai, *Appl. Phys. Lett.* 90, 211914 (2007). doi:10.1063/1.2743395.