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Review Article

Compliant Substrates for Heteroepitaxial Semiconductor Devices: Theory, Experiment, and Current Directions

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This review paper presents important findings relative to the use of compliant substrates for mismatched heteroepitaxial devices, including the theoretical background, experimental results, and the directions for current efforts. Theories for relative compliance and absolute compliance are presented. Key experimental results are summarized for a number of compliant substrate technologies, including cantilevered membranes, silicon-on-insulator, twist bonding, and glass bonding. Two approaches of current interest, layer transfer and universal compliant trench (UCT) substrates, are presented as potential solutions to the problem of limited absolute compliance in planar compliant substrates attached to handle wafers.

Key words: Compliant substrates, heteroepitaxy, silicon-on-insulator, twist bonded, wafer bonding, universal compliant trench substrates, critical layer thickness

INTRODUCTION

Compliant substrates represent one of the most promising defect engineering approaches for the realization of mismatched heteroepitaxial semiconductor devices. Using a compliant substrate, mismatched device layers may be grown virtually free from performance-degrading dislocation defects, and the lattice mismatch is accommodated by elastic or plastic strain in a compliant substrate layer. Modeling and experimental studies indicate that several fabrication approaches (especially wafer bonding and silicon-on-insulator) may be used to produce compliant substrates having adequate relative compliance e (a unitless ratio) for the required device applications. However, it has recently come to light that these approaches lack the necessary absolute compliance s (in units of length) for successful implementation on planar, large-area wafers. New approaches to the problem, including universal compliant trench (UCT) substrates being pursued at the University of Connecticut in collaboration with San Jose State University,[1] appear capable of solving these problems and finally delivering on the promise of compliant substrates. In this article, we review important modeling and experimental work on compliant substrates, discuss relative and absolute compliance, and describe new directions for the realization of compliant substrates for devices. Other application areas for compliant substrates such as flexible electronics and ferroelectric devices are also important but beyond the scope of this paper.

In planar mismatched heteroepitaxy on a thick substrate, the epitaxial layer assumes all of the mismatch strain so that this layer must be kept less than the critical layer thickness to avoid the generation of dislocations. However, the ability to grow pseudomorphic layers thicker than the critical layer thickness would be beneficial in many device applications. To meet this need, Lo[2] proposed the use of compliant substrates.

A compliant substrate is one sufficiently thin (or otherwise deformable) so that it will become strained by the deposition of a mismatched epitaxial layer. The partitioning of strain between the epitaxial layer and its substrate causes a reduction in the overall strain energy. If the substrate is sufficiently thin, the strain energy will never reach a

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level such as to cause the introduction of misfit dislocations. In this case, the effective critical layer thickness diverges to infinity with the result that a pseudomorphic layer of any thickness may be grown.

Practically speaking, a membrane thin enough to act as a compliant substrate is difficult to handle during device processing. In addition, thin compliant membranes are susceptible to curvature and distortions of their shape during strained heteroepitaxy. As a consequence, compliant substrate implementation requires the realization of a thin compliant layer on a rigid handle wafer, also known as a mechanical host substrate (MHS).[3] This handle wafer must restrain the compliant layer in the growth direction, to prevent buckling, but the compliant layer must be mechanically decoupled from its handle in the plane of the interface. Although practical schemes of this sort provide adequate relative compliance e (a percentage) they do not allow the needed absolute compliance s (or slip, in units of length) at the present point in time.

In this review paper, we first consider the theory of relative compliance and the historical background of compliant substrate implementation. We will then discuss the concept of absolute compliance and the newly developed approaches of layer transfer and universal compliant trench (UCT) substrates.[1]

THEORY OF RELATIVE COMPLIANCE

Suppose that there is no limit on the absolute compliance of an epitaxial layer which is grown coherently (without misfit dislocations) on a compliant substrate with lattice mismatch strain f [Here, we adopt the definition of f used in Ref. 4. Thus $f \equiv (a_s - a_e)/a_e$ is the lattice mismatch strain which exists in a coherently strained epitaxial layer, where a_s and a_e are the relaxed lattice constants of the substrate and epitaxial layer, respectively.] The following discussions are confined to the practical case of zero curvature (i.e., a flat interface between the compliant layer and its handle wafer); Bourret[5] has discussed the possible effects of curvature on the partitioning of strain in an epitaxial layer on a compliant substrate. Moreover, although Maroudas et al.[6] and Bourret[5] considered kinetic models for relative compliance based on plastic flow,[7] here we are more interested in equilibrium structures—these are more desirable for device structures which may be subjected to subsequent high-temperature processing during device fabrication. With no curvature of the bilayer structure, the compliant substrate and epitaxial layer will be oppositely strained such that

$$\varepsilon_{epi} - \varepsilon_{sub} = f, \tag{1}$$

where ε_{epi} and ε_{sub} are the in-plane strains in the epitaxial layer and the substrate, respectively. If the bending stresses are negligible, force balance in the structure dictates that

$$\sigma_{epi} h_{epi} + \sigma_{sub} h_{sub} = 0, \tag{2}$$

where h_{epi} and h_{sub} are the thicknesses of the epitaxial layer and substrate, respectively, and σ_{epi} and σ_{sub} are the in-plane stresses. The stresses are biaxial so that, if we assume isotropic behavior of the epitaxial and compliant layers,

$$\sigma_{epi} = \frac{Y_{epi}}{1 - \nu_{epi}} \varepsilon_{epi}, \tag{3}$$

and

$$\sigma_{sub} = \frac{Y_{sub}}{1 - \nu_{sub}} \varepsilon_{sub}, \tag{4}$$

where Y_{epi} and Y_{sub} are the Young's moduli and ν_{epi} and ν_{sub} are the Poisson ratios. Solution of these four equations yields

$$\varepsilon_{epi} = \frac{f}{1 + \left(K \frac{h_{epi}}{h_{sub}}\right)} \tag{5}$$

and

$$\varepsilon_{sub} = \frac{-f}{1 + \left(\frac{1}{K} \frac{h_{sub}}{h_{epi}}\right)}, \tag{6}$$

where K is given by

$$K = \frac{Y_{epi}}{(1 - \nu_{epi})} \frac{(1 - \nu_{sub})}{Y_{sub}}. \tag{7}$$

The areal strain energy can be found from

$$E_e = \int [Y/(1 - \nu)] \varepsilon^2 \mathrm{d}h, \tag{8}$$

where Y is the Young's modulus, ν is the Poisson ratio, ε is the strain, and the integration is over thickness. Integrating, we obtain the areal strain in the bilayer system as

$$E_e = \frac{Y_{epi}}{(1 - \nu_{epi})} h_{epi} \varepsilon_{epi}^2 + \frac{Y_{sub}}{(1 - \nu_{sub})} h_{sub} \varepsilon_{sub}^2. \tag{9}$$

If we assume that the substrate and epitaxial layer have approximately equal values for the Young's modulus and Poisson's ratio, the strain energy reduces to

$$E_e = \frac{Y}{(1 - \nu)} f^2 \left(\frac{h_{epi} h_{sub}}{h_{epi} + h_{sub}}\right). \tag{10}$$

The effective critical layer thickness h_{eff} for lattice relaxation may be estimated using the energy criterion of Matthews.[8] This is the thickness for which the areal strain energy exceeds the misfit dislocation energy per unit area E_d, and is given by

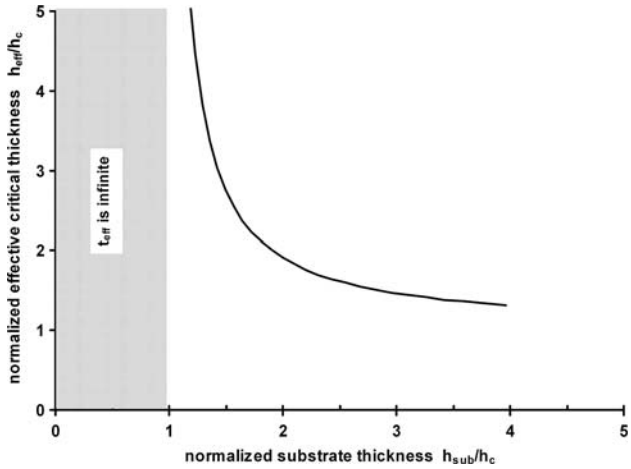

Fig. 1. Normalized critical layer thickness h_{eff}/h_c versus the normalized substrate thickness h_{sub}/h_c for the growth of a mismatched heteroepitaxial layer on a compliant substrate. h_{eff} is the effective critical layer thickness, h_{sub} is the thickness of the compliant substrate, and h_c is the Matthews and Blakeslee critical layer thickness. (Reprinted from Ref. 2 with permission. Copyright 2005, American Institute of Physics).

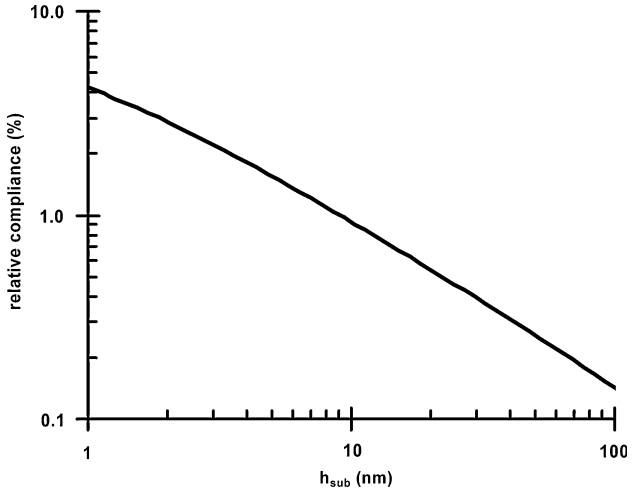

Fig. 2. Relative compliance as a function of compliant layer thickness.

$$\frac{1}{h_{\text{eff}}} = \frac{1}{h_c} - \frac{1}{h_{\text{sub}}}, \tag{11}$$

where h_c is the Matthews and Blakeslee critical layer thickness[9] and h_{sub} is the substrate thickness. Figure 1 shows the normalized critical layer thickness h_{eff}/h_c as a function of the normalized substrate thickness h_{sub}/h_c.

When $h_{sub} < h_c$, there exists no solution to Eq. 11 so that h_{eff} becomes infinite. This condition defines the relative compliance limit: it is the value of the lattice mismatch strain f for which $h_c = h_{sub}$. The critical layer thickness can be calculated using the Matthews and Blakeslee[9] relationship for a dislocation inherited from the substrate,

$$h_c = \frac{b(1 - \nu\cos^2\alpha)[\ln(h_c/b) + 1]}{8\pi|f|(1+\nu)\cos\lambda}, \tag{12}$$

where b is the length of the Burgers vector, ν is the Poisson's ratio, is the angle between the Burgers vector and the line vector, and λ is the angle between the Burgers vector and the line in the interface plane that is perpendicular to the intersection of the glide plane with the interface. Therefore, the relative compliance e is given by

$$e = \frac{b(1 - \nu\cos^2\alpha)[\ln(h_{\text{sub}}/b) + 1]}{8\pi h_{\text{sub}}(1+\nu)\cos\lambda}. \tag{13}$$

The relative compliance is plotted as a function of the substrate compliant layer thickness in Fig. 2, using the assumptions that $\cos\alpha = \cos\lambda = 1/2$, $b = 0.40$ nm, and $\nu = 1/3$. It can be seen that the relative compliance exceeds 1% if the compliant substrate layer can be made thinner than 10 nm; this level of relative compliance should be sufficient for many device applications.

For a twist-bonded compliant substrate, Obayashi and Shintani[10] have shown that the critical layer thickness will be increased relative to the value calculated in Eq. 12 by the interaction of the strain fields associated with the misfit dislocations and the screw dislocations in the twist boundary.

Other formulations for the critical layer thickness have been developed as well, in which different approaches have been used for the calculation of the energy of the misfit dislocation. Freund and Nix[11] used the concept of half-space image forces to find the misfit dislocation energy. Zhang et al.[12,13] analyzed the critical layer thickness for an epilayer on a substrate of finite thickness by an energy approach. To model the energy of an interfacial misfit dislocation, they used superposition and Fourier theory to account for the truncation of the dislocation stress field at the free surfaces.

Apart from the complete avoidance of relaxation, compliant substrates can also give rise to reduced dislocation densities in cases of partial lattice relaxation, when the lattice mismatch exceeds the relative compliance. As demonstrated by Lo,[2] this results from the modified image forces for dislocations in the partially relaxed bilayer structure. For a thick substrate, the image force always attracts dislocations toward the free surface of the epitaxial layer. In that case, the image force arises due to the truncation of the dislocation stress field at the free surface of the epitaxial layer, and it is equal to the attractive force which would exist between the real dislocation and its image, which has the opposite Burgers vector and is located at an equal but opposite distance from the surface. For the case of a compliant substrate, the image force can be greatly decreased in magnitude and may even change sign, driving the dislocation into the substrate rather than toward the epitaxial layer surface. Thus if the

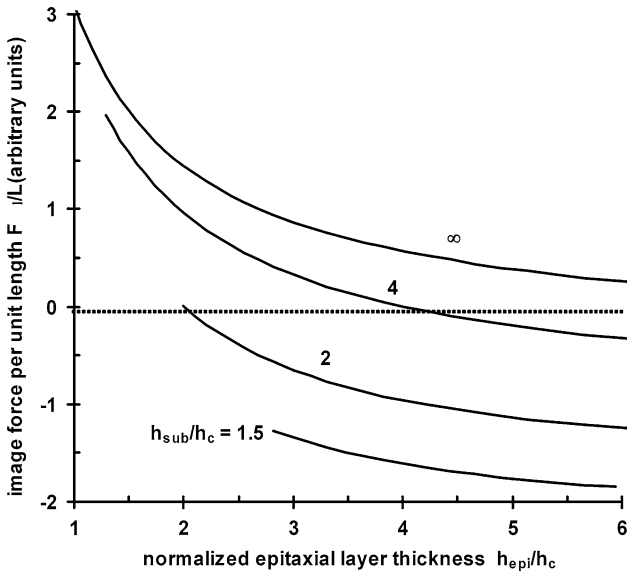

Fig. 3. Image force (arbitrary units) for a 60 deg misfit dislocation at the interface between an epitaxial layer and a compliant substrate, versus the normalized epitaxial layer thickness h_{epi}/h_c, and with the normalized substrate thickness h_{sub}/h_c as a parameter, where h_c is the Matthews and Blakeslee critical layer thickness. (Reprinted from Ref. 2 with permission. Copyright 2005, American Institute of Physics).

substrate is compliant, its "free" surface contributes to the overall image force along with the epitaxial layer surface. Lo calculated this image force for a 60 deg misfit dislocation along a ⟨110⟩ direction for (001) heteroepitaxy of a zincblende material on a compliant substrate, finding the image force per unit length of dislocation to be

$$\frac{F_I}{L}=\frac{Gb^2}{4}\left(\frac{1}{4}+\frac{1}{2(1-\nu)}\right)\left(\frac{1}{h_{epi}+h_{sub}}\right)\cot\left(\frac{\pi h_{epi}}{h_{epi}+h_{sub}}\right). \quad (14)$$

Misfit dislocations experience the greatest attractive image force in the case of an infinite (noncompliant) substrate. Any reduction in the thickness of the substrate decreases the absolute value of the image force, for a given epitaxial layer thickness. The image force sign may even change, indicating that the dislocations will be pushed toward the "free" surface of the compliant substrate layer. This is shown in Fig. 3, which provides the calculated image force (in arbitrary units) as a function of the normalized epitaxial layer thickness h_{epi}/h_c, with the normalized substrate thickness h_{sub}/h_c as a parameter.

IMPLEMENTATION OF CANTILEVERED MEMBRANE COMPLIANT SUBSTRATES

Some of the initial compliant substrate demonstrations used nonplanar approaches. The first was the cantilevered membrane, first proposed by Teng and Lo[14] and also demonstrated by Chua et al.[15] These implementations used two or four mounting points. Jones et al.[16] also demonstrated pedestal-mounted compliant membranes for the growth of InGaAs quantum well structures on GaAs substrates.

Multipoint-Mounted Membranes

Teng and Lo[14] first proposed a cantilevered membrane compliant substrate. Their design, shown in Fig. 4, could be fabricated using an undercutting wet etch. The membrane is supported at the four corners, but should behave as a compliant substrate in the central region away from the supports. Teng and Lo were able to produce cantilevered membranes of this type by the selective wet etching of GaAs/AlGaAs and InP/InGaAs epitaxial structures.

Chua et al.[15] demonstrated a cantilevered membrane compliant substrate with the bench structure shown in Fig. 5. To create the 80 nm membrane, they first grew a 80 nm GaAs/100 nm $Al_{0.8}Ga_{0.2}As$/GaAs (001) structure using molecular beam epitaxy

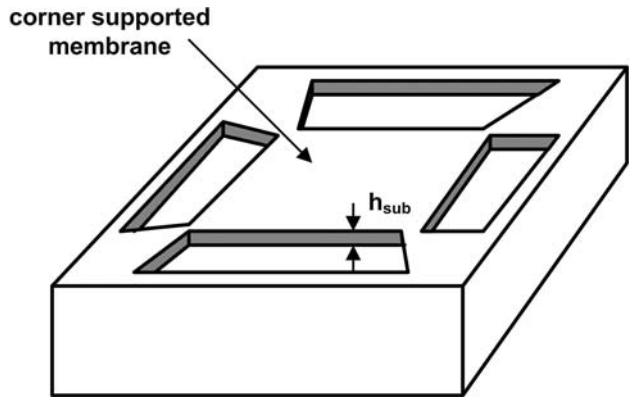

Fig. 4. A cantilevered membrane for use as a compliant substrate. Reprinted from Ref. 14 with permission. Copyright 1993, American Institute of Physics).

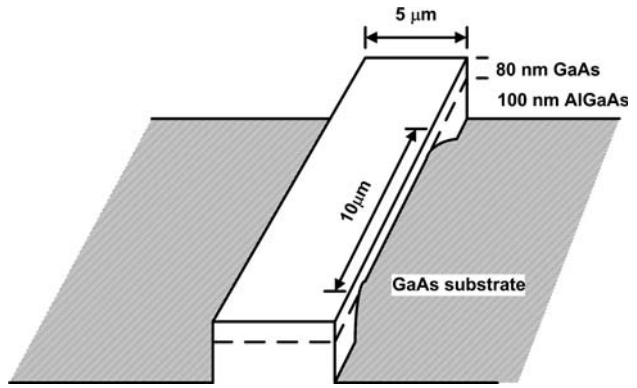

Fig. 5. Cantilevered membrane with a bench structure, for use as a compliant substrate. (Reprinted from Ref. 15 with permission. Copyright 1994, American Institute of Physics).

(MBE). Photolithography and a nonselective etch were used to obtain mesa-etched stripes 5 μm wide and with a 10 μm center-to-center spacing in the epitaxial material. A second photolithographic step was then used to open stripes perpendicular to the first set, having a width of 10 μm, and subsequently performed a selective etch of the through these openings with 1 HF:5 H_2O.

Using a cantilevered membrane compliant substrate, Chua et al.[15] grew $In_{0.14}Ga_{0.86}$ As with a room-temperature mismatch strain of $f = -0.94\%$ and a critical layer thickness of $h_c \approx 10$ nm. $In_{0.14}Ga_{0.86}As$ was grown simultaneously on the compliant platform and on a reference, unprocessed GaAs substrate, to a thickness of 200 nm, or about 20 times the expected critical layer thickness. The observed 004 x-ray diffraction peak separation (between the x-ray diffraction peaks for the GaAs and $In_{0.14}Ga_{0.86}As$) was significantly greater on the compliant platform than on the reference substrate; this was interpreted as an indication of tetragonal distortion in the GaAs platform, which would have been expected if it was compliant. Chua et al. also studied the surface morphology of the $In_{0.14}Ga_{0.86}As$ by atomic force microscopy (AFM). The layer on the reference substrate exhibited surface roughening associated with misfit dislocations but the layer grown on the compliant platform showed an absolutely smooth surface texture.

Pedestal-Mounted Membranes

Jones et al.[16] investigated the use of a pedestal-mounted compliant membrane for the growth of InGaAs quantum well structures on GaAs substrates. The pedestal structure was formed by growing a 5-μm-thick pedestal layer of $Al_{0.6}Ga_{0.4}As$ and a 40-nm-thick $In_{0.05}Ga_{0.95}As$ compliant layer by metalorganic vapor-phase epitaxy (MOVPE). Ring patterns were defined lithographically with a nonselective etch (1:8:80 H_2SO_4:H_2O_2:H_2O) and then a selective etch (2:5 HF:H_2O) was used to undercut the pedestal. In this way, compliant membranes of 13 μm diameter were produced on 1-μm-diameter pedestals. An InGaAs quantum well structure was then grown on the pedestal-mounted membrane by MOVPE, and the structure was characterized by photoluminescence (PL), cathodoluminescence (CL), and scanning electron microscopy (SEM). Figure 6 shows a schematic drawing of the final structure along with an SEM micrograph. PL and CL results showed relatively weak luminescence from the material grown directly over the pedestal due to the present of misfit dislocations, but there was no such evidence of dislocations in the material grown on the overhanging portion of the membrane.

The above results confirm the relative compliance performance in cantilevered compliant membranes, and are significant from a proof-of-principle point of view. On the other hand, cantilevered membranes are expected to be mechanically fragile and will have compromised heat-removal properties. For these reasons planar approaches, which produce a thin compliant layer on a handle wafer, have been pursued by a number of research groups.

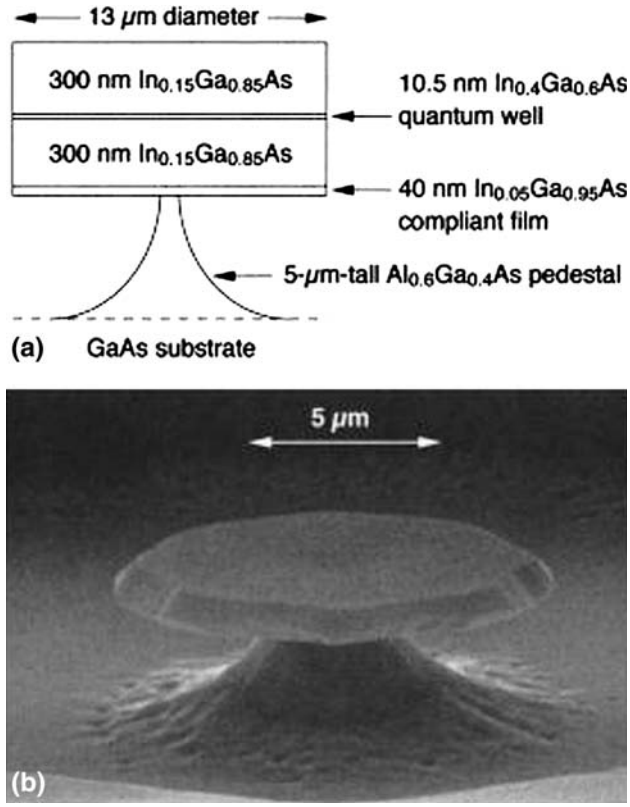

Fig. 6. InGaAs quantum well structure grown on a pedestal-mounted compliant membrane: (a) schematic and (b) scanning electron microscope micrograph. (Reprinted from Ref. 16 with permission. Copyright 1999 American Institute of Physics).

IMPLEMENTATION OF PLANAR COMPLIANT SUBSTRATES

Planar approaches to compliant substrates generally involve the realization of a thin compliant layer, which is on top of a thick handle wafer but mechanically decoupled from it. Along these lines, wafer bonding is the most studied method. Here, an etch-stop layer and compliant layer are grown epitaxially on one wafer, which is then bonded to a handle wafer. The former wafer is then removed by lapping and etching, leaving just the compliant layer bonded to the handle wafer. The desired relative compliancy may be achieved by the use of an appropriate thickness for the compliant layer, provided that it is mechanically decoupled from the handle by an intermediate layer (e.g., metal or glass) or by a twist bond. Carter-Coman et al.[17,18] developed compliant substrates using wafer bonding with an intermediate layer of indium. The indium layer melts at epitaxial growth temperatures to render the thin layer compliant. Moran et al.[19,20] have developed a bonded compliant substrate technology which uses an intermediate layer

of borosilicate glass (BSG); other glass bonding techniques may be used as well. Twist-bonded compliant substrates avoid the need for the insertion of an intermediate layer; instead, the array of screw dislocations at the twist boundary is intended to provide the required slip for compliant growth. Still another handle-wafer approach which does not require wafer bonding is the use of silicon-on-insulator (SOI) wafers. To this end, Powell et al.[21] studied the epitaxy of SiGe alloys on an ultrathin SOI layer. Yang et al.[22] extended this work to the growth of GaN on both SOI substrates and also SiC-on-silicon-on-insulator substrates. However, Rehder et al.[23] showed that, in the case of large-area SiGe heteroepitaxy, a thin SOI layer does not act as a compliant substrate (in the sense of strain partitioning), even though it does alter the dislocation structure and dynamics.

Silicon-on-Insulator (SOI) Compliant Substrates

Silicon-on-insulator (SOI) has been studied extensively as a planar compliant substrate for the growth of SiGe alloys, GaN, and GaAs. Here, the silicon-on-insulator will act as a compliant substrate with a relative compliance given by Fig. 2 as long as it is mechanically decoupled from the wafer by sufficient slip (absolute compliance) at the Si/SiO_2 interface. Mixed experimental results with this type of compliant substrate indicate that the necessary absolute compliance may be difficult to obtain. Recent experiments by Rehder et al.[23] involving the growth of SiGe on SOI wafers indicate that the silicon layer does not behave as a compliant substrate in the usual sense, even though they found partial strain partitioning between the thin Si layer and the SiGe, and observed the preferential introduction of dislocations in the compliant layer.

Powell et al.[21] performed early investigations with ultrathin SOI as a compliant substrate, for the growth of SiGe alloys. In their experiments, they etched an SOI wafer to leave only 50 nm thickness of silicon. Then they grew 10 nm of homoepitaxial Si followed by 60 nm to 170 nm of $Si_{0.85}Ge_{0.15}$ by MBE at 500°C. (For $Si_{0.85}Ge_{0.15}$/Si, the room-temperature mismatch strain is $f = -0.0062$, corresponding to $h_c = 17$ nm.) Various epitaxial layer thicknesses were obtained using shadow masking, to keep all other growth conditions the same. It was found that, for a 170-nm-thick layer of $Si_{0.85}Ge_{0.15}$ on the ultrathin SOI substrate, lattice relaxation occurred by the introduction of dislocations in the thin Si layer rather than the $Si_{0.85}Ge_{0.15}$. After a 1 h anneal at 700°C, 800°C, or 900°C, the layer had relaxed significantly compared to the as-grown layer. Also, transmission electron microscopy (TEM) analysis revealed that the structure annealed at 700°C contained misfit dislocations at the $Si/Si_{0.85}Ge_{0.15}$ interface, but that the associated threading dislocations only penetrated the Si layer, and not the epitaxial $Si_{0.85}Ge_{0.15}$. They interpreted these results as evidence of compliance in the Si layer, associated with slip at the Si/SiO_2 interface. A conclusive test of compliant behavior in this material system could be made by growing various thicknesses of $Si_{0.85}Ge_{0.15}$ on an SOI layer less than $h_c = 17$ nm in thickness. Such an SOI layer would have sufficient relative compliance so that no misfit dislocations would be expected to form at the Si/SiGe interface. However, a 60-nm-thick SOI layer was used by Powell et al. so no definitive test of the absolute compliance could be undertaken.

LeGoues et al.[24] studied the *ex situ* relaxation of SiGe on SOI compliant substrates. The SOI wafer used in this study was produced using separation by ion implantation of oxygen (SIMOX), and had a top Si layer 65 nm thick with a dislocation density of $\sim 10^5$ cm^{-2}. An 180-nm-thick $Si_{0.85}Ge_{0.15}$ layer ($f = -0.0062$ and $h_c = 17$ nm) was grown by MBE at 400°C, and the relaxation and dislocation structure were observed in the as-grown sample and after post-growth annealing. In an as-grown sample, no dislocations were observed by cross-sectional transmission electron microscopy (XTEM), indicating a threading dislocation density less than about 10^6 cm^{-2} for the experimental conditions used. The as-grown $Si_{0.85}Ge_{0.15}$ was believed to be pseudomorphic because, according to x-ray diffraction measurements, the $Si_{0.85}Ge_{0.15}$ and underlying Si exhibited equal in-plane lattice constants. Upon annealing at 700°C or 900°C in an inert ambient, the $Si_{0.85}Ge_{0.15}$ relaxed by the formation of 60 deg interfacial dislocations, but the associated threading dislocations only propagated in the thin Si layer. This was interpreted as evidence of ideal compliancy in the SIMOX SOI wafer, but they did not compare this behavior to the case of growth on standard silicon control wafers. Also, as with the previous study by Powell et al.,[21] they did not grow on a Si layer of less than 17 nm thickness to test the ability to grow a coherent layer with unlimited thickness.

Yang et al.[22] demonstrated the growth of GaN on SiC on SOI. In their work, they produced a thin layer of SiC on a bonded and etched SOI (BESOI) wafer by heat treatment of the top silicon layer with a flux of carbon or acetylene at 900°C. Following this they grew GaN on the SiC-on-SOI wafer using a 10 nm AlN nucleation layer, a 10 nm GaN layer, and ten periods of AlN/GaN superlattice (period = 4 nm). A top layer of GaN, 200 nm thick, was then grown, but few details of its material properties were provided.

Seaford et al.[25] compared the MBE growth of GaAs on Si (511) and SOI (511) wafers. The SOI (511) wafer was fabricated by bonding and the top layer of silicon was thinned to 100 nm. Compared to growth on the control substrate, GaAs grown on the SOI (511) wafer exhibited a 25% reduction in the 004 rocking curve full-width at half-maximum (FWHM) and an order-of-magnitude reduction in the threading dislocation density as determined by

XTEM characterization. However, based on the thickness of the SOI layer, the relative compliancy would not have been sufficient to completely avoid dislocations in the epitaxial material in these experiments.

Pei et al.[26] also studied the growth of GaAs on SOI (511) wafers, with top silicon thicknesses of 100 nm and 200 nm. They showed by XTEM that the GaAs on the thinner (100 nm) SOI layer had a lower threading dislocation density than the GaAs grown on the thicker (200 nm) SOI layer. Neither layer, however, would be expected to have sufficient relative compliance for growth free from misfit dislocations according to Fig. 2.

Another variation on the SOI compliant substrate involves the use of ion implantation to convert the SiO_2 layer to borosilicate glass (BSG), as pioneered by Luo et al.[27] In this work, boron and oxygen were ion implanted into a commercial SOI wafer and a two-step annealing process was used to render the insulator layer as BSG with the desired composition. The BSG SOI compliant substrates have been used for the heteroepitaxy of SiGe, with improved quality relative to growth on control Si wafers.

Despite extensive published results, the question remained as to whether a silicon-on-insulator layer could serve as a true compliant substrate, mechanically released from its handle substrate, if the silicon layer were designed to provide sufficient relative compliance. Pei et al.[28] argued that the benefit of growing on an SOI wafer came from modified dislocation dynamics rather than true compliant substrate behavior. In order to address this question, Rehder et al.[23] undertook a detailed experimental and modeling study of SiGe relaxation on silicon-on-insulator substrates. The $Si_{0.82}Ge_{0.18}$ layers ($f = -0.0074$ and $h_c = 14$ nm) were grown by vapor-phase epitaxy (VPE) to various thicknesses at temperatures of 550°C, 630°C, and 670°C. $Si_{0.82}Ge_{0.18}$ was also grown at 700°C, but only to a thickness of 6 nm because it immediately roughened. The substrates were SOI wafers with top Si thicknesses of 40 nm, 70 nm, 330 nm, and 10,000 nm as well as bulk Si control wafers. The resulting samples were examined by XRD, AFM, and TEM.

In this study it was found that pseudomorphic $Si_{0.82}Ge_{0.18}$, 150 nm thick, could be grown on 40-nm- or 70-nm-thick SOI layers. However, the films were metastable and could be relaxed *ex situ* by annealing in the temperature range from 875°C to 1050°C. Following annealing at 950°C, the SOI was found to develop a strain (0.047% and 0.035% for the 40 nm and 70 nm SOI layers, respectively). However, these values of strain were only about one-quarter of the values expected for an ideally compliant layer. In addition, the strain in the SOI layer only appeared in conjunction with the broadening of the SiGe XRD peak and the appearance of surface crosshatch, both of which are indirect indications of misfit dislocation production at the SiGe/Si interface.

Rehder et al. also studied the *in situ* relaxation of $Si_{0.82}Ge_{0.18}$ grown at 630°C. SiGe layer thicknesses of 150 nm, 340 nm, 765 nm, and 1200 nm were grown, giving rise to a wide range of *in situ* strain relaxation; the 150 nm layer exhibited zero lattice relaxation whereas the thickest layer had 80% lattice relaxation.

To understand whether the SOI behaved as an ideal compliant substrate, Rehder et al. compared their experimental results to four equilibrium models for the strain in the thin Si layer of the SOI. In the compliant substrate model of Lo,[2] if it is assumed that $\nu_{SiGe} = \nu_{Si}$ and $E_{SiGe} = E_{Si}$, then the in-plane strains in the SiGe and Si should be

$$\varepsilon_{SiGe} = \frac{f}{1 + h_{SiGe}/h_{Si}}, \tag{15}$$

and

$$\varepsilon_{Si} = \frac{-f}{1 + h_{Si}/h_{SiGe}}, \tag{16}$$

respectively.

Rehder et al. developed three additional models by equating the line tension on the misfit segment of a dislocation (at the SiGe/Si interface) with the strain force exerted on the threading segment of the dislocation in the thin silicon-on-insulator layer. In model 1, the line tension of the misfit segment of a dislocation at the interface was assumed to be the same as in the case of growth on a thick, noncompliant substrate. Neglecting the core parameter, this is given by

$$F_L = \frac{Gb(1 - \nu\cos^2\alpha)}{4\pi(1 - \nu)} \ln\left(\frac{h_{SiGe}}{b}\right), \tag{17}$$

where G is the shear modulus and has been assumed to be equal for the epitaxial layer and the substrate, α is the angle between the Burgers vector and the line vector for the dislocations, and h_{SiGe} is the epitaxial layer thickness. However, they recognized that the line tension of the misfit segment would be reduced by the presence of the SiO_2 layer, because of its lower shear modulus. In model 2, the line tension was calculated using Eq. 17 but the average shear modulus for Si and SiO_2 was used. In developing model 3, they assumed that the oxide acts as a free surface, leading to a modified line tension given by

$$F_L = \frac{Gb(1 - \nu\cos^2\alpha)}{4\pi(1 - \nu)} \ln\left(\frac{h_{Si}h_{SiGe}}{b(h_{Si} + h_{SiGe})}\right). \tag{18}$$

For all three models, the strain force on the threading segment of the dislocation in the silicon on insulator was calculated using

$$F_{TD} = \frac{Gb\varepsilon_{Si}h_{Si}(1 + \nu)}{(1 - \nu)}, \tag{19}$$

where ε_{Si} is the in-plane strain in the silicon layer. The equilibrium strain in the Si is predicted to be

$$\varepsilon_{Si} = \frac{b(1-\nu\cos^2\alpha)}{4\pi h_{Si}(1+\nu)}\ln\left(\frac{h_{SiGe}}{b}\right); \quad \text{(Model 1)} \qquad (20)$$

$$\varepsilon_{Si} = \left(\frac{G_{Si}+G_{SiO_2}}{2G_{Si}}\right)\frac{b(1-\nu\cos^2\alpha)}{4\pi h_{Si}(1+\nu)}\ln\left(\frac{h_{SiGe}}{b}\right); \quad \text{(Model 2)} \qquad (21)$$

$$\varepsilon_{Si} = \frac{b(1-\nu\cos^2\alpha)}{4\pi h_{Si}(1+\nu)}\ln\left(\frac{h_{Si}h_{SiGe}}{b(h_{Si}+h_{SiGe})}\right); \quad \text{(Model 3)} \qquad (22)$$

or

$$\varepsilon_{Si} = \frac{|f|}{1+h_{Si}/h_{SiGe}}. \quad \text{(Lo Model)} \qquad (23)$$

Figure 7 shows the out-of-plane strain calculated using these four models, along with the experimental results of Rehder et al. The calculated results are shown for model 1 (dashed curve), model 2 (dotted curve), and model 3 (solid curve). The solid curve at the top labeled "compliant substrate" was calculated using the Lo model. The experimental results for $Si_{0.82}Ge_{0.18}$ layers with thicknesses of 1200 nm and 765 nm are plotted as well, and can be fit very well using model 3. However, the strain partitioning in the silicon-on-insulator layers does not follow the compliant substrate theory.

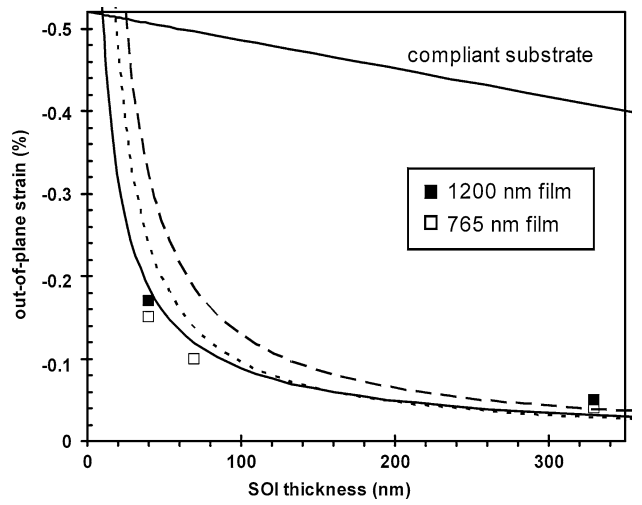

Fig. 7. Out-of-plane strain in a silicon-on-insulator layer as a function of the Si thickness. The calculated results are shown for model 1 (dashed curve), model 2 (dotted curve), model 3 (lower solid curve), and the Lo compliant substrate model (upper solid curve). Also shown are experimental results for the growth of $Si_{0.82}Ge_{0.18}$ layers on SOI substrates, with $Si_{0.82}Ge_{0.18}$ thicknesses of 1200 nm and 765 nm. (Reprinted from Ref. 23 with permission. Copyright 2003, American Institute of Physics).

In summary, Rehder et al. found that the dependence of the $Si_{0.82}Ge_{0.18}$ relaxation on the temperature and thickness was similar on bulk Si and SOI wafers. In all cases, relaxation of the $Si_{0.82}Ge_{0.18}$ was accompanied by the introduction of misfit dislocations at the SiGe/Si interface. Tensile strain in the Si, predicted by compliant substrate theory, only occurred with the introduction of interfacial misfit dislocations. Moreover, the amount of strain in the Si was too small to be attributed to a compliant substrate mechanism. The only important effect of the SOI substrate is that the buried oxide layer reduces the line energies of misfit dislocations. Whereas a compliant substrate is supposed to increase the critical layer thickness for an epitaxial overlayer, the reduction in the misfit dislocation line energy actually decreases the critical layer thickness. These results show that, in the work of Rehder et al., the SOI did not behave as a compliant substrate for the overgrowth of SiGe.

Twist-Bonded Compliant Substrates

Ejeckam et al.[29,30] developed a compliant substrate approach based on the twist-bonding of two wafers, followed by the thinning of the top wafer to render it compliant. This twist-bonded structure was called a compliant universal (CU) substrate.[31]

The twist bonding process developed by Ejeckam et al.[30] is illustrated schematically in Fig. 8. It begins with two standard GaAs (001) wafers. An AlAs (or $Al_yGa_{1-y}As$) etch-stop layer and a 10-nm-thick compliant layer of GaAs are grown epitaxially on one of the wafers. Next, the two wafers are bonded together with a twist angle. The top GaAs substrate is etched away to the etch stop layer, and then the AlAs layer itself is removed by another selective etch step. This leaves only the thin (compliant) GaAs layer twist-bonded to the handle wafer. It has been found that the bonding[32] and

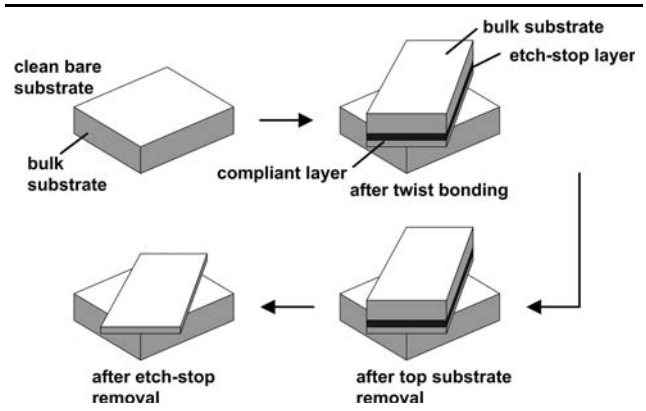

Fig. 8. Fabrication process for a twist-bonded compliant substrate. (Reprinted from Ref. 30 with permission. Copyright 1997 American Institute of Physics).

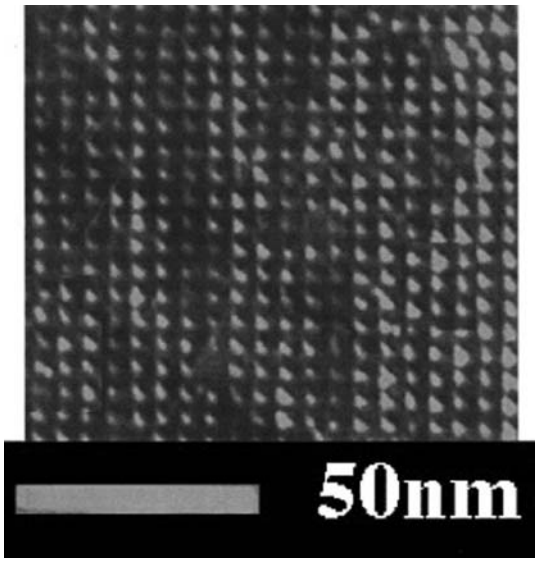

Fig. 9. Plan-view dark-field weak-beam TEM micrograph of a twist boundary created by bonding a 10 nm GaAs compliant layer to a GaAs (001) substrate. The twist angle is 4.2 deg, and the spacing of the screw dislocations is $d = 5.3$ nm (Reprinted from Ref. 30 with permission. Copyright 1997, American Institute of Physics).

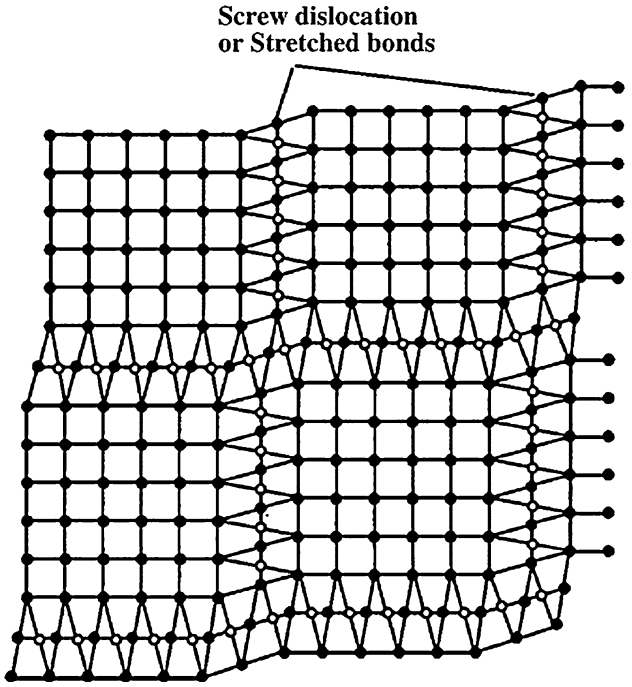

Fig. 10. Schematic of a twist boundary between simple cubic crystals. The open circles represent atoms in the thin, compliant layer while the closed circles represent atoms in the substrate wafer (Reprinted from Ref. 30 with permission. Copyright 1997, American Institute of Physics).

etching[33] steps are critical for the realization of a high-quality twist-bonded interface.

At the twist bond there is a large angular misalignment (several degrees) between the $\langle 110 \rangle$ directions of the compliant layer and the substrate, though the $\langle 001 \rangle$ directions are parallel. This results in a square array of screw dislocations, with a spacing d given by Frank's rule:

$$d = \frac{b}{2\sin(\theta/2)}, \tag{24}$$

where b is the length of the Burgers vector and θ is the twist angle. Figure 9 shows a plan-view TEM micrograph of such a twist boundary created by bonding a 10 nm GaAs compliant layer to a GaAs (001) substrate. With a twist angle of 4.2 deg, the spacing of the screw dislocations is $d = 5.3$ nm, very close to the value predicted by Frank's rule ($d = 5.5$ nm).

The atomic structure of the twist boundary is shown schematically in Fig. 10 for the case of simple cubic crystals. The open circles (closed circles) represent atoms in the compliant layer (handle wafer). Inside the square regions, the atoms in the twist-bonded layer line up with the atoms in the underlying handle wafer, but in the boundaries between the square regions, there are significant atomic displacements associated with the array of screw dislocations.

Jesser et al.[3] made a detailed theoretical study of the implementation of twist-bonded compliant substrates. Two of their key findings were (1) that the twist angle should be large (greater than about 8 deg), and (2) that coincidence angles should be avoided. A large twist angle results in overlapping strain fields for the screw dislocations at the boundary, thus providing the necessary relative compliance. On the other hand, a coincidence angle (one which causes a large number of lattice sites to align across the boundary) should be avoided because this locks the thin twist-bonded layer into a deep energy minimum with respect to the handle wafer, and renders it noncompliant.

The design requirements for a twist-bonded compliant substrate, as enumerated by Jesser, van der Merwe, and Stoop, are summarized below:

1. The compliant layer should be as thin as possible, but not so thin that the screw dislocations at the twist boundary are attracted to its surface.
2. The twist angle should be greater than about 8 deg.
3. Coincidence angles should be avoided.
4. Ideally, the compliant layer should be selected to have a small lattice mismatch with the heteroepitaxial material which will be grown on top of it, but the compliant layer need not be lattice matched with the handle substrate.
5. The compliant layer should be chosen to induce layer-by-layer growth of the heteroepitaxial layer on top of it; island growth will lead to geometrically necessary dislocations where the islands coalesce.
6. Ideally, the compliant layer should have a smaller Young's modulus than the heteroepitaxial material which will be grown on top of it.

7. The handle wafer should have a large mismatch with respect to the compliant layer, achieved either through a large twist angle or a large lattice constant mismatch, but need not be of the same crystal structure as the compliant layer.

Practical twist-bonded compliant substrates often satisfy several but not all of these design criteria but have nonetheless been used with varying levels of success for the growth of heteroepitaxial InGaP, $In_{0.22}Ga_{0.78}As$, GaSb, and InSb.

Ejeckam et al.[30] used twist-bonded GaAs compliant substrates to grow $In_{0.35}Ga_{0.65}P$. Their compliant substrates included a 10 nm top layer bonded to a GaAs substrate with a twist angle of 9 deg, 17 deg, or 32 deg. They grew 300 nm of $In_{0.35}Ga_{0.65}P$ on the twist-bonded compliant substrates by metalorganic vapor-phase epitaxy (MOVPE). For this composition, $f = 0.01$ and $h_c \approx 10$ nm. Though these layers are ~30 times the critical layer thickness for this heteroepitaxial material system, they were observed to be free from dislocations for all values of the twist angle investigated.

In a second study, Ejeckam et al.[31] used twist-bonded GaAs compliant substrates to grow InSb ($f = -12.7\%$). The twist-bonded wafer had a 3 nm compliant layer bonded with a twist angle of 40 ± 5 deg. On these compliant substrates, it was possible to grow pseudomorphic layers of InSb up to 650 nm thick, many times the critical layer thickness.

Glass-Bonded Compliant Substrates

Hansen et al.[34] and Moran et al.[19,20] studied the growth of InGaAs on GaAs compliant substrates which were glass-bonded using borosilicate glass (glass compositions between 10% and 50% B_2O_3 were investigated). In this approach, the borosilicate glass is designed to have a low viscosity at the temperature used for heteroepitaxy, thus (hopefully) allowing sufficient slip between the compliant layer and the handle wafer, and the viscosity is controlled by the glass composition.

Moran et al.[19,20] characterized $In_{0.44}Ga_{0.56}As$ grown on GaAs compliant substrates which were glass-bonded using borosilicate glass with a composition of either 10% or 30% B_2O_3. The 10% and 30% borosilicate glasses have viscosities of 10^{17} P and 10^{12} P, respectively, at the growth temperature of 650°C. In this study, $In_{0.44}Ga_{0.56}As$ layers 3 μm thick were grown on unprocessed GaAs control substrates, 12 deg twist-bonded compliant substrates, and both low- and high-viscosity glass-bonded compliant substrates. They found that the material grown on the glass-bonded compliant substrates (either low- or high-viscosity) had the best crystal quality (as judged by the 004 x-ray rocking curve FWHM). Interestingly, the material grown on the twist-bonded wafer appeared to be inferior to that grown on the conventional GaAs substrate.

Other Wafer-Bonding Approaches

Other bonding approaches have also been investigated for compliant substrate fabrication. Doolittle et al.[35] demonstrated a compliant substrate technology in which a thin GaN film was grown epitaxially on lithium gallate ($LiGaO_2$ or LGO) removed by selective etching, and then bonded on GaAs. In their work, a 0.28-μm-thick layer of GaN was grown by radiofrequency (RF) plasma MBE on an LGO host wafer at a temperature in the range of 600°C to 900°C. Following epitaxial growth, the host wafer was inverted and bonded to a bare GaAs (001) wafer. Using a basic etch solution, the LGO could be removed with great selectivity, leaving just the thin GaN layer bonded to the GaAs handle wafer. This process will render a large density of dislocations at the bonded interface between the thin GaN layer and the GaAs substrate; as in the case of the twist-bonded compliant substrate, this might allow a sufficient degree of relative compliance in the GaN layer. However, it is not clear that the required absolute compliance may be achieved for large-area applications, and there has been no demonstration of epitaxial layer/compliant layer strain partitioning as expected in the case of a truly compliant substrate.

Other Approaches

Other approaches have also been proposed for the realization of compliant substrates. Luo et al.[36] showed that, for the MBE growth of SiGe on Si (001) substrates, a low-temperature Si buffer can act as a compliant layer and reduce the strain in the SiGe. Ion implantation into Si has been used to create compliant substrates, by the implantation of Ar^+ to create subsurface damage[37] or the implantation of He^+ to create a nanoporous weak layer.[38]

It is possible that subsurface ion implantation damage could create a weak layer in a semiconductor wafer, allowing slip of the thin layer above it and resulting in compliant substrate behavior. Along these lines, Chen et al.[37] studied the growth of SiGe epitaxial layers on Si substrates which had been ion-implanted with Ar^+. The implantation energy was 30 keV, 40 keV, or 60 keV and the dose was 3×10^{15} cm^{-2}. $Si_{0.81}Ge_{0.19}$ films were grown by ultrahigh-vacuum chemical vapor deposition. Rutherford back-scattering and channeling (RBS/C) measurements were used to characterize samples grown on the implanted compliant substrates and a control wafer. The SiGe layers grown on the implanted wafers exhibited a much higher degree of lattice relaxation (82% to 98%) compared to the SiGe on the control wafer (18%), and this was interpreted as evidence for a compliant substrate effect in the implanted wafers. However, the observed strain relaxation does not agree with the Lo theory for strain partitioning in a compliant substrate/epitaxial layer system, and the expected increase in the critical layer thickness has not been verified.

Beji et al.[39] showed that the heteroepitaxial growth of InAs on porous GaAs led to an increase in the critical layer thickness relative to growth on a nonporous substrate. This led to interest in the use of a porous layer as a weak layer to allow slip between a compliant substrate layer and its handle wafer. Chicoine et al.[38] investigated compliant substrates of this type, implemented by the inclusion of nanocavities below the surface of an InP wafer. These nanocavities were produced by ion implanting He^+ into an InP (001) wafer followed by thermal annealing under a phosphorous overpressure. Implantation energies ranged from 25 keV to 100 keV; the doses varied from 1×10^{16} cm^{-2} to 3×10^{16} cm^{-2}. InAsP/InP heterostructures were grown epitaxially on the porous compliant substrates as well as InP control wafers. The epitaxial structures on the compliant substrates showed a greater extent of lattice relaxation compared to those on the control wafers. Also, in the case of the compliant substrates, some of the threading dislocations were seen to propagate into the compliant layer rather than the epitaxial structure. These results are promising, but there does not appear to have been the expected ideal strain partitioning between the epitaxial structures and the compliant layer on the porous compliant substrate.

RELATIVE AND ABSOLUTE COMPLIANCE

For any compliant substrate using a thin compliant layer on a handle wafer, the relative compliance e (a unitless ratio) is determined entirely by the thickness and elastic properties of the compliant layer, but the absolute compliance s (in units of length) is limited by the amount of slip which can be achieved at the interface between the compliant layer and its handle. For most applications, the necessary relative compliance may be achieved using any of a number of compliant layer materials simply by proper choice of the compliant layer thickness. On the other hand, the experimental results to date suggest that current technologies for the fabrication of large-area compliant substrates fail to achieve sufficient mechanical decoupling of the compliant layer and its handle wafer within the plane of the interface; in other words, there is insufficient absolute compliance.

The issue of absolute compliance can be understood by considering the growth of a thick, pseudomorphic heteroepitaxial layer on a thin compliant substrate with a handle wafer. If the heteroepitaxial layer is much thicker than the compliant layer then all of the lattice mismatch should be accommodated by elastic strain in the compliant layer. For a lattice mismatch of 1%, the compliant substrate would develop an elastic in-plane strain of −1%. The required lateral slip (absolute compliance) between the compliant substrate and its handle (assumed to be rigid and unstrained) will be

$$s = -\frac{fD}{2}, \tag{25}$$

where f is the lattice mismatch between the heteroepitaxial layer and the compliant substrate and D is the wafer diameter. For the case of a 300 mm wafer with $|f| = 1\%$ the required absolute compliance (slip) will be 1.5 mm. However, absolute compliance of this magnitude is apparently not possible with the compliant substrate technologies which have been investigated up to the present time. This problem was recognized as early as 2000 by Bourret.[5] Kastner and Gosele later pointed out that, because the predicted absolute slip has not been observed at the periphery of epitaxial layers on compliant wafers, it is necessary to reject the concept of strain partitioning in large-area compliant substrates.[40] They therefore developed a modified theory which predicts a decrease in the critical layer thickness for growth on a large-area compliant substrate.[41] The underlying causes for limited absolute compliance will differ depending on the compliant substrate technology, but for the case of twist-bonded wafers they may include dislocation bunching, untwisted domains growing in interfacial pinholes,[42] or voids and inclusions such as those observed in bonded GaAs wafers.[43]

CURRENT DIRECTIONS

Current research on compliant substrates focuses on the need to limit the lateral dimensions of the device regions so that the required slip (absolute compliance) can be kept at a realizable level. One approach involves the transfer of a compliant layer plus epitaxial layer to an oxide-coated handle wafer. This approach is especially valuable for investigations of carrier transport in SiGe layers subjected to uniaxial or biaxial strain. Another approach, called universal compliant trench (UCT) substrates,[1] is more flexible because it does not mandate the inclusion of an oxide layer and because it places fewer restrictions on the composition and thickness of the compliant layer. Either approach has the potential for adoption in commercial production of SiGe-based very large-scale integrated circuits.

Transfer to a Compliant Oxide

Hobart et al.[44,45] pioneered a compliant substrate technology involving transfer to a borophosphosilicate glass (BPSG)-coated Si wafer. First a (sacrificial) host Si wafer is used for the pseudomorphic growth of $Si_{0.7}Ge_{0.3}$ (30 nm) followed by a cap layer of Si (2 nm). The sacrificial wafer is then implanted with H_2^+ at an energy of 180 keV and with a dose of 4.5×10^{16} cm^{-2}, to facilitate separation. About 200 nm of BPSG is deposited on a second (handle) wafer. The host wafer and handle wafer are bonded together at room temperature, followed by a bond-enhancing anneal (250°C for 4 h) and a separation anneal (550°C in N_2). After removal of remaining Si

on the separated structure (selective etching using KOH, 10% by weight), the end result is 30 nm $Si_{0.7}Ge_{0.3}$/2 nm Si/200 nm BPSG/Si handle wafer. The 2 nm Si layer has little effect on the strain in the $Si_{0.7}Ge_{0.3}$. After lithographic patterning, the $Si_{0.7}Ge_{0.3}$ may be used as a compliant substrate for the growth of Si, SiGe, or possibly other materials. Within limits, the thickness or composition of the compliant layer may be tailored for the application at hand. However, the approach is restricted to compliant layers which may be grown coherently on a Si wafer. Otherwise, the compliant layer will develop a large dislocation density and this will be inherited by the epitaxial material on top of it.

An interesting application of transfer to a compliant oxide is the development of material with tailored strain for improved carrier mobility in metal-oxide-semiconductor field-effect transistors (MOSFETs). Yin et al.[46] and Peterson et al.[47] demonstrated that the patterned $Si_{0.7}Ge_{0.3}$ regions relax during annealing in such a way that the strain near their centers follows an exponential with a time constant given by

$$\tau_L = \frac{\eta L^2}{c'_{11} h_f h_g}, \tag{26}$$

where η is the viscosity of the BPSG, L is the width of the patterned region along the direction for which the strain is measured, c'_{11} is the elastic stiffness constant for this crystal direction, h_f is the SiGe thickness and h_g is the glass thickness. In the case of rectangular islands, the strain relaxation behavior may be very different in the two axial directions, so that uniaxial strain may even be approximated. In general, the state of strain may be tailored to optimize the transport properties in n-channel or p-channel MOSFETs.

Universal Compliant Trench (UCT) Substrates

A more flexible approach involving patterned compliant regions is called universal compliant trench (UCT) substrates.[1] These may be fabricated using metal-bonded, glass-bonded, twist-bonded, or SOI techniques, after which anisotropic etching is used to create trenches between compliant regions which can be used for device and circuit fabrication. The basic steps in the fabrication of a UCT compliant substrate are illustrated in Fig. 11, for the case of twist-bonding. The trench-defined regions can be rectangular or of any arbitrary shape. If the largest dimension of these regions is d, then the necessary slip (absolute compliance) will be limited to

$$s = -\frac{fd}{2}. \tag{27}$$

In the practical implementation of a UCT substrate, using a twist-bonded compliant layer, the compliancy derives from an array of screw dislocations having a Burgers vector b. If the maximum slip is limited to $5b$ at the twist-bonded interface,[48] then

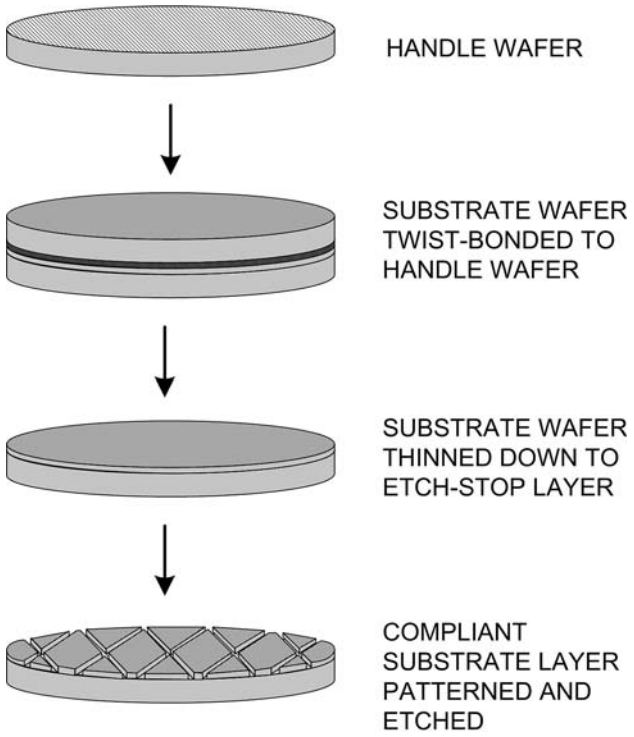

Fig. 11. The universal compliant trench (UCT) fabrication process. For specificity, a twist bonding approach is shown. Other bonding approaches or silicon-on-insulator wafers may be used with appropriate changes in the design rules.

the compliant substrate can accommodate at most a lattice mismatch equal to

$$|f_{max}| = \frac{10b}{d}. \tag{28}$$

Then for the accommodation of ±0.4% lattice mismatch with b = 0.4 nm, the compliant pads may be made up to 1000 nm in size. This will be sufficient for many device applications, including digital transistors, light-emitting diodes, and detectors. These engineering calculations strongly suggest that device-sized compliant pads can be achieved using the UCT concept. Current work at the University of Connecticut in collaboration with San Jose State University is aimed at UCT substrate research, including fabrication and performance assessment.

CONCLUSION

In this review article, theories have been presented for relative compliance and absolute compliance. Key experimental results have been summarized for a number of compliant substrate technologies, including cantilevered membranes, silicon-on-insulator, twist bonding, and glass bonding. These results suggest that the limited success of large-area, planar compliant substrates on handle wafers may be related to insufficient absolute

compliance (slip) at the compliant layer—handle wafer interface. Two newly developed approaches, layer transfer and universal compliant trench (UCT) substrates, have been presented as potential solutions to this problem.

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48. Because of the lack of experimental data, this represents a best estimate which should be verified experimentally. However, it is reasonable to expect the absolute compliance will be on the order of a few times the length of the Burgers vector.