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A Study on the Thermal Reliability of Cu/SnAg Double-Bump Flip-Chip Assemblies on Organic Substrates

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The Cu/SnAg double-bump structure is a promising candidate for fine-pitch flip-chip applications. In this study, the interfacial reactions of Cu (60 μm)/SnAg (20 μm) double-bump flip chip assemblies with a 100 μm pitch were investigated. Two types of thermal treatments, multiple reflows and thermal aging, were performed to evaluate the thermal reliability of Cu/SnAg flip-chip assemblies on organic printed circuit boards (PCBs). After these thermal treatments, the resulting intermetallic compounds (IMCs) were identified with scanning electron microscopy (SEM), and the contact resistance was measured using a daisy-chain and a four-point Kelvin structure. Several types of intermetallic compounds form at the Cu column/SnAg solder interface and the SnAg solder/Ni pad interface. In the case of flip-chip samples reflowed at 250°C and 280°C, Cu_6Sn_5 and $(Cu, Ni)_6Sn_5$ IMCs were found at the Cu/SnAg and SnAg/Ni interfaces, respectively. In addition, an abnormal Ag_3Sn phase was detected inside the SnAg solder. However, no changes were found in the electrical contact resistance in spite of severe IMC formation in the SnAg solder after five reflows. In thermally aged flip-chip samples, Cu_6Sn_5 and Cu_3Sn IMCs were found at the Cu/SnAg interface, and $(Cu, Ni)_6Sn_5$ IMCs were found at the SnAg/Ni interface. However, Ag_3Sn IMCs were not observed, even for longer aging times and higher temperatures. The growth of Cu_3Sn IMCs at the Cu/SnAg interface was found to lead to the formation of Kirkendall voids inside the Cu_3Sn IMCs and linked voids within the Cu_3Sn/Cu column interfaces. These voids became more evident when the aging time and temperature increased. The contact resistance was found to be nearly unchanged after 2000 h at 125°C, but increases slightly at 150°C, and a number of Cu/SnAg joints failed after 2000 h. This failure was caused by a reduction in the contact area due to the formation of Kirkendall and linked voids at the Cu column/Cu_3Sn IMC interface.

Key words: Cu/SnAg double-bumps, fine-pitch flip chip, thermal reliability, reflow, thermal aging, interfacial reactions

INTRODUCTION

In order to obtain better electrical performance in first-level chip interconnections, the pitch and diameter of flip chip joints need to be reduced.[1] According to the International Technology Roadmap for Semiconductor (ITRS), the pad pitch of area array flip chips was reduced to 130 μm in 2005, and will be further reduced to 100 μm in 2009.[2] Due to the limitations of solder bumps in fine pitches less than 150 μm, a double-bump structure consisting of a metal column and Sn-based solder bumps has been proposed, and its assembly processes and

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reliability issues have been investigated.[3–6] The authors have also proposed and successfully demonstrated a Cu column/SnAg double-bump structure as an alternative to solder flip-chip assemblies in ultrafine-pitch applications.[7]

The Cu/SnAg double-bump structure has three significant advantages for flip-chip assembly. First, this structure enables finer-pitch flip-chip interconnections due to the straight shape of Cu column bumps. Secondly, better thermomechanical reliability can be achieved by changing the height of the column bumps. Given that Cu column bumps can reduce the strain in solder bumps,[3–6] a flip-chip assembly with better thermal cycling reliability is expected at a higher stand-off bump height. The Cu column bump height can easily be varied with electroplating methods. Finally, this structure guarantees excellent electromigration reliability due to its high melting point and the good thermal and electrical conductivity of Cu at a current-crowded site. In conventional solder flip-chip assemblies, Sn reacts with Cu or Ni underbump metallurgy (UBM) very quickly due to its low melting temperature under current stress. In particular, Sn and Cu or Ni atoms used as UBM materials at a current-crowded site are mostly consumed. This is the origin of the lowering of the reliability of solder joints under current stress.[6,8,9]

In spite of these advantages, studies of Cu/SnAg double-bump flip chips are relatively uncommon. The interfacial properties of Cu/SnAg double-bump structures are among several issues for their application in actual devices. Sn-based solder reacts with Cu and Ni during solder reflow or solid-state aging. In particular, SnAg solder and electroless Ni pads are expected to be much faster than in a conventional solder flip chip, because a Cu/SnAg double-bump flip chip can have a solder thickness of only 20 μm. The excessive growth of brittle IMCs and the consumption of solder can result in a decline in the thermal reliability of joints due to degradations of the contact resistance and the mechanical adhesion strength. Therefore, understanding the interfacial reactions at the Cu/SnAg/Ni joints, such as the growth of IMCs and the consumption of solder, is essential to the investigation of the thermal reliability of double-bump flip-chip assemblies for fine-pitch applications.

EXPERIMENTS

Test chips were fabricated with the procedure shown in Fig. 1. First, a 1500-Å-thick silicon oxide layer was deposited on an eight-inch silicon wafer by using thermal oxidation and a Ti (100 Å)/TiN (200 Å) layer was deposited onto the silicon oxide layer as the stress buffer and adhesion layers, respectively. A 1-μm-thick Al layer was then sputtered and patterned with metal pads and conductor lines. The size of the Al pad was 60 μm × 60 μm, and the pitch was 100 μm. An 8 μm passivation layer was coated onto the wafer. The opening diameter of the passivation layer was 40 μm. TiW (1000 Å) was then deposited as an adhesion promotion and diffusion barrier layer, and Cu (4000 Å) was deposited as a seed layer for electroplating on the top surface of the silicon wafer. In addition, a thick photoresist (PR) was spin-coated and patterned by using photolithography processes. A PR thickness of 110 μm was obtained through double coating, with an opening size of 60 μm. After the PR patterning, the Cu and SnAg bumps were deposited with an electroplating method. Cu and Sn-2.5Ag solder were electroplated at a current density of 3 ASD (Ampere/square decimeter = A/dm^2) for 90 min and at 3.5 ASD for 15 min. The target heights of the electroplated Cu and SnAg bumps were 60 μm and 20 μm, respectively. After the electroplating of the Cu/SnAg double bumps, the thick PR was stripped away, and the Cu and TiW seed layers were etched with etching solutions for 120 s and 250 s, respectively.

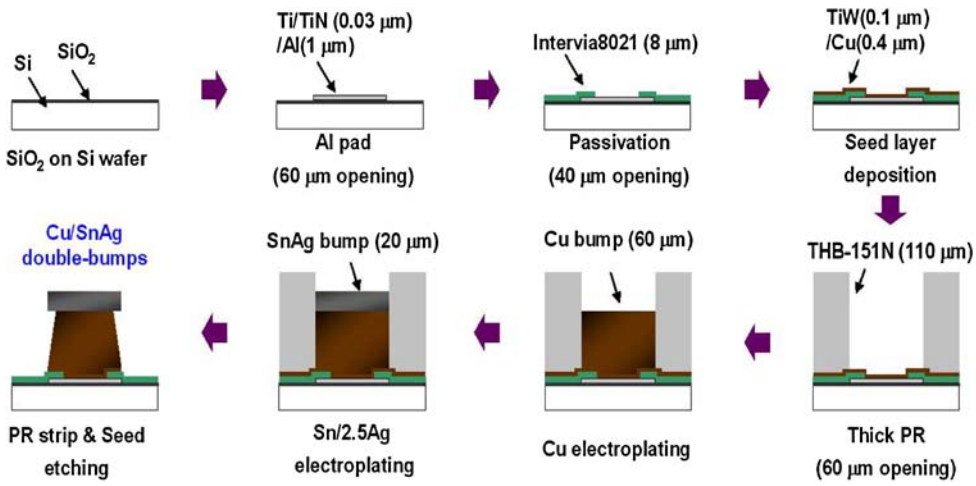


Fig. 1. Schematic illustration of the test chip fabrication processes.

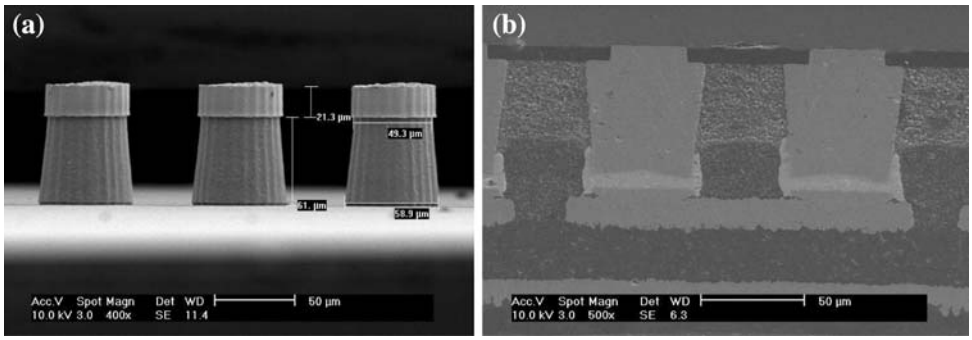


Fig. 2. (a) Cu/SnAg double-bumps and (b) cross-sectional image of Cu/SnAg double-bumps of an assembled flip chip.

Figure 2 shows cross-sectional scanning electron microscopy (SEM) images of the Cu/SnAg double bumps and the assembled flip-chip samples. A test chip was flip-chip assembled onto a PCB test substrate with 18-μm-thick Cu and Ni (8 μm)/Au (0.1 μm) finished metal pads. The opening size and the thickness of the PCB solder mask were 50 μm and 18 μm, respectively. The pitch of the PCB metal pads was 100 μm. PCB Cu lines were added for electrical continuity measurements. The contact resistance of each bump was measured with a four-point Kelvin structure. Figure 3 shows a schematic diagram of the method used for measuring the bump contact resistance using the four-point Kelvin structure.

To investigate the interfacial reactions of the Cu/SnAg double-bump flip-chip assembly, the samples were exposed to two types of thermal treatment: multiple reflows and solid-state aging. Multiple reflows with peak temperatures of 250°C and 280°C were performed from one to five times. Solid-state aging was performed for up to 2000 h at 125°C and 150°C. The thermally treated samples were ground and polished for the observation of the cross-sectioned area. The SnAg solder was then selectively etched with a mixture of methanol, hydrochloric acid, and nitric acid in order to examine the IMC morphology clearly. The Cu/SnAg joint morphology was observed with SEM and backscattered electron (BSE) imaging, and the bump contact resistance was measured with the four-point Kelvin structure. SEM energy-dispersive spectroscopy (SEM-EDS) and focused ion beam (FIB) techniques were used to examine the IMC phases and their morphologies, as were wavelength dispersive spectroscopy (WDS) and transmission electron microscopy (TEM).

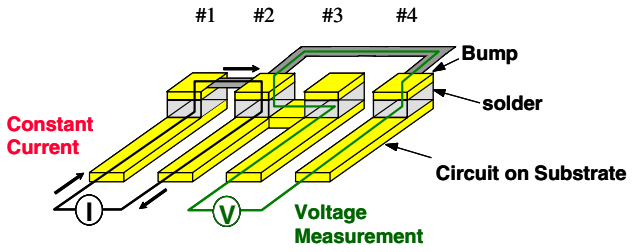


Fig. 3. Schematic illustration of a four-point Kelvin structure for the contact resistance measurement of a bump.

RESULTS AND DISCUSSION

A number of studies on Cu-Sn and Ni-Sn interfacial reactions have been carried out on conventional solder bump structures. Even though the solder reactions are similar in conventional solder bump and Cu/SnAg double-bump flip-chip assemblies, interfacial reactions in Cu/SnAg double-bump structure with much smaller solder volume should be discussed because they may more dominantly affect thermal reliability during thermal aging and multiple reflows than in the conventional solder bump structure.

Figures 4 and 5 show cross-sectional SEM-BSE images of a reflowed Cu/SnAg double bump at 250°C and 280°C. After the solder reflow, intermetallic compounds (IMCs) are visible at the solder joints, which arise because molten Sn atoms diffuse into the Cu column side and the Ni pad side, and then Cu-Sn and Ni-Sn IMCs form. On the Cu column side, scallop-like Cu_6Sn_5 (η) IMCs have formed at the Cu/SnAg interface. Thin Cu_3Sn (ε) IMCs less than 0.1 μm thick are present between the Cu_6Sn_5 IMCs and the Cu column bumps. In addition, Kirkendall voids have formed along the Cu/Cu_6Sn_5 interface. The Cu atoms dissolved into the SnAg solder during the solder reflow of the flip-chip assembly, resulting in IMC formation on the PCB pad side. During the initial stages of the multiple reflows, needle-like Ni_3Sn_4 IMCs formed on the PCB Ni/Au pads, and all the IMCs are then converted to $(Cu, Ni)_6Sn_5$ IMCs. As the Cu-rich IMCs have a lower activation energy for formation than do the Ni_3Sn_4 IMCs,[10] $(Cu, Ni)_6Sn_5$ IMCs are mainly observed on the PCB pad side rather than in the Ni_3Sn_4 phase. As the number of multiple reflows increased, a dark P-rich Ni layer forms between the electroless Ni/Au pad and the $(Cu, Ni)_6Sn_5$ IMCs. The thickness of the P-rich Ni layer, Cu_6Sn_5, and $(Cu, Ni)_6Sn_5$ IMCs increase as the number of reflows and the reflow temperature increased. At 250°C, the thickness of the Cu_6Sn_5 IMCs on the

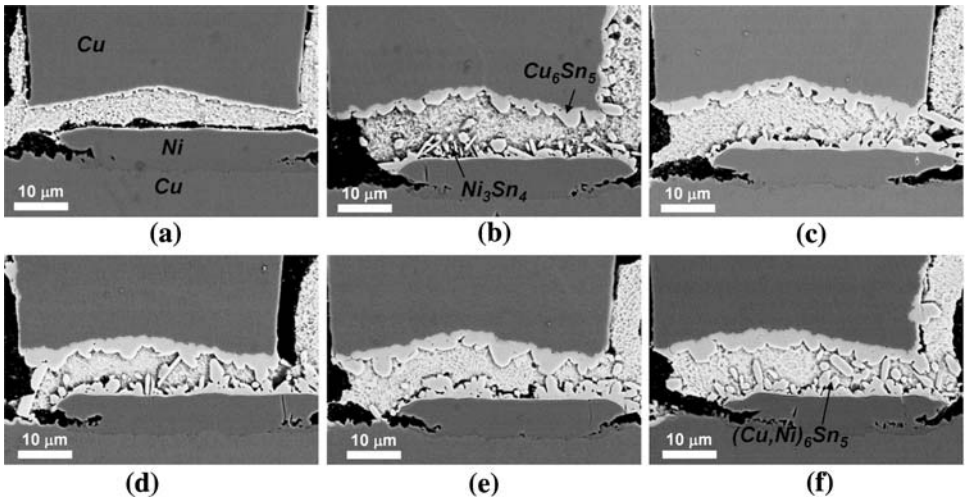


Fig. 4. Cross-sectional SEM-BSE images of a reflowed Cu/SnAg double-bump with the number of the additional reflows at 250°C (a) as-assembled, (b) one reflow, (c) two reflows, (d) three reflows, (e) four reflows, and (f) five reflows.

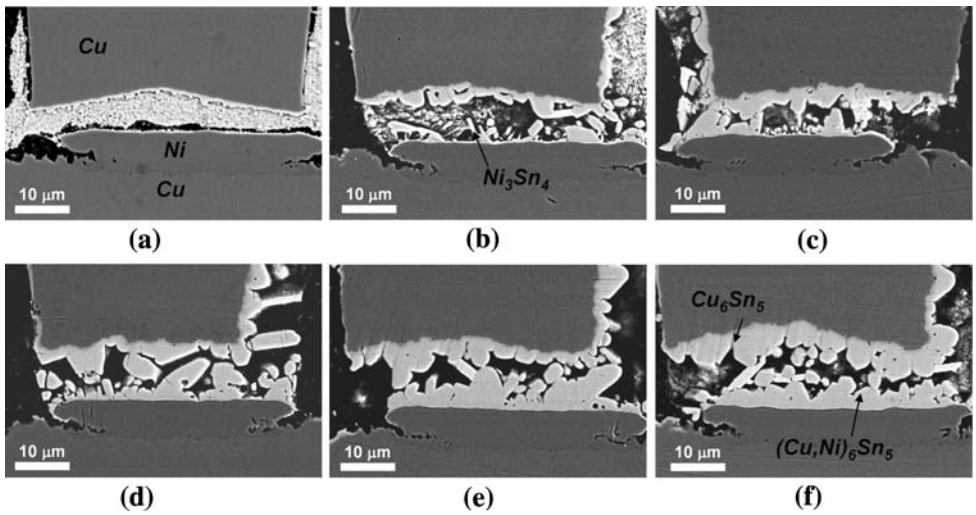


Fig. 5. Cross-sectional SEM-BSE images of a reflowed Cu/SnAg double-bump with the number of the additional reflow at 280°C (a) as-assembled, (b) one reflow, (c) two reflows, (d) three reflows, (e) four reflows, and (f) five reflows.

Cu column side were found to be approximately 3 μm to 4 μm after five reflows. However, at 280°C they grow to 5 μm to 7 μm, and the $(Cu, Ni)_6Sn_5$ IMCs on the PCB pad side reach a thickness of 4 μm to 6 μm. Whereas half of the SnAg solder remains after five reflows at 250°C, nearly all of the SnAg solder is consumed at 280°C. In addition, abnormal Ag_3Sn IMCs and Cu_6Sn_5 IMCs spall into the SnAg solder to reduce their surface energy,[11,12] as shown in Fig. 6. The growth of brittle IMC phases such as Cu_6Sn_5 and Ag_3Sn can prevent plastic deformation when thermomechanical stress is applied to a

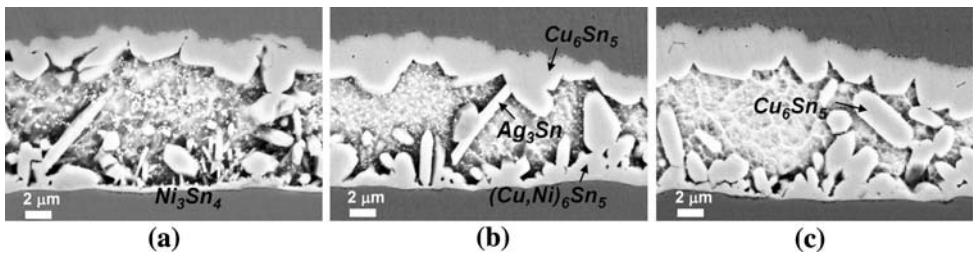


Fig. 6. IMC growth and spalling after 250°C reflows: (a) one reflow, (b) three reflows, and (c) five reflows.

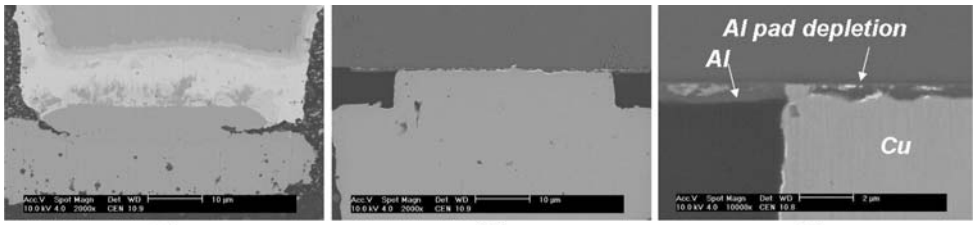


Fig. 7. A failed bump after thermal cycling (a) Cu/SnAg/Ni interface, (b) Al/TiW/Cu column interface, and (c) magnified image of (b) showing UBM depletion.

flip-chip assembly. In the results of the thermal cycling reliability test, however, failure occurred at the interface between the Al pad and the Cu column bump on the chip side, rather than in the solder, as shown in Fig. 7. This indicates that the growth of thick intermetallic compounds does not have an effect on the thermomechanical reliability of Cu/SnAg double-bump flip-chip assemblies, in which the heights of the solder bumps are much lower than those of conventional solder flip-chip assemblies.

The solid-state interfacial reactions that occur during thermal aging were studied. Figures 8 and 9 show cross-sectional SEM-BSE images of flip-chip samples aged at 125°C and 150°C, respectively. The IMC formation resulting from thermal aging has different characteristics to that found for multiple reflows. During thermal aging, thick Cu-Sn IMCs grow at the Cu column/SnAg solder interface. Scallop-like Cu_6Sn_5 IMCs (η) were found at the interface and a Cu_3Sn IMC (ε), which appears darker than the Cu_6Sn_5 IMCs, was found between the Cu_6Sn_5 IMCs and the Cu column interface. The Cu_6Sn_5 IMCs increase in size as the aging time increases, and Sn atoms diffuse into the Cu column/Cu_6Sn_5 IMC interface through the channels between the Cu_6Sn_5 IMCs.[12] As a result, the Cu_6Sn_5 IMCs are converted into a Cu-rich phase consisting of Cu_3Sn IMCs.

$$Cu_6Sn_5 \rightarrow 2Cu_3Sn + 3Sn \quad (1)$$

As shown in Figs. 8 and 9, many Kirkendall voids are present in the Cu_3Sn IMC layer. The voids produced by aging at 150°C are larger than those produced at 125°C, and they are linked to each other; these voids result from the difference between the diffusion rates of Cu and Sn. There are sufficient Cu atoms at the Cu/Cu_6Sn_5 interface to form a Cu_3Sn IMC, and the required Sn atoms diffuse across the Cu_6Sn_5 IMC. At this time, nine Cu atoms are needed to form three Cu_3Sn IMCs for three Sn atoms generated by the resolution reaction of Cu_6Sn_5 IMCs of Eq. 1.[13,14] Therefore, two vacancies are formed as a result of the formation of one Cu_3Sn IMC. The formation of Kirkendall voids at the Cu/SnAg interface of a flip-chip joint is expected to weaken its mechanical strength.

$(Cu, Ni)_6Sn_5$ IMCs are visible on the PCB Ni/Au pad side. The Cu_6Sn_5 IMCs form a stable phase in the Cu/Sn interface, but Ni is substituted into the Cu lattice points of the Cu_6Sn_5 IMCs due to the presence of Ni in the electroless Ni/Au pads. As can

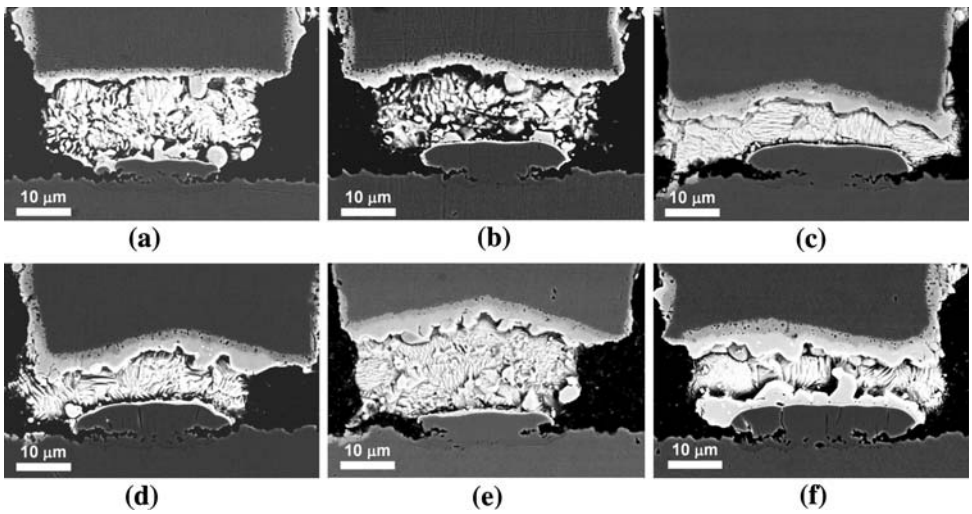


Fig. 8. Cross-sectional SEM-BSE images of thermally aged flip-chip samples at 125°C (a) 250 h, (b) 500 h, (c) 750 h, (d) 1000 h, (e) 1500 h, and (f) 2000 h.

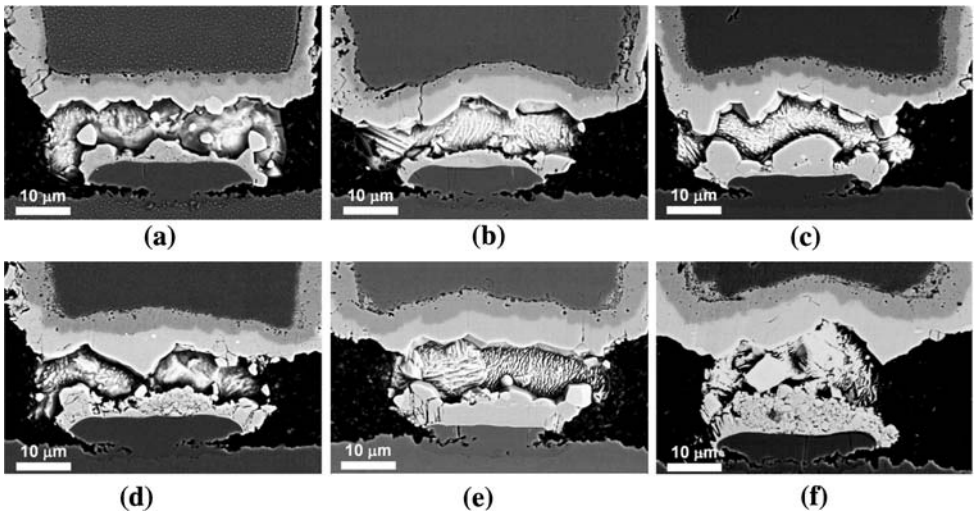


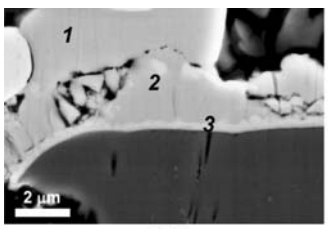
Fig. 9. Cross-sectional SEM-BSE images of thermally aged flip-chip samples at 150°C (a) 250 h, (b) 500 h, (c) 750 h, (d) 1000 h, (e) 1500 h, and (f) 2000 h.

be seen in the results of the SEM-EDS spot analysis shown in Fig. 10, the amount of Sn is nearly constant within the Cu_6Sn_5 IMCs. However, the amount of Ni increases as the distance from the Ni pad decreases. In contrast to the case for multiple reflows, no Ni_3Sn_4 IMCs were observed on the PCB Ni/Au pads. With multiple reflows, the thickness of (Cu, Ni)$_6Sn_5$ IMCs on the PCB pad side were almost the same as that of the Cu_6Sn_5 IMCs on the Cu column side. However, the Cu_6Sn_5 IMCs grow faster than the (Cu, Ni)$_6Sn_5$ IMCs during thermal aging. At 125°C up to 1500 h, there is little formation of (Cu, Ni)$_6Sn_5$ IMCs on the PCB Ni/Au pads. (Cu, Ni)$_6Sn_5$ IMCs that are nearly 5 μm thick form during aging at 150°C up to 2000 h, but the growth of the Cu_6Sn_5 IMCs on the Cu column side is more evident than that of the (Cu, Ni)$_6Sn_5$ IMCs on the PCB pad side. This result can be explained in terms of the diffusivity of Cu and Ni in solid and liquid Sn. Table I shows the diffusion coefficients of Cu and Ni in solid and liquid Sn.[15,16] The diffusion coefficients of Cu and Ni in liquid Sn at 287°C are nearly identical. However, the diffusion coefficient of Cu is approximately 50 times higher than that of Ni. Therefore, the growth of Cu_6Sn_5 and Cu_3Sn IMCs proceeds rapidly, and the levels of consumption of Cu and Sn and Kirkendall void formation in Cu_3Sn IMCs are remarkable. After 2000 h of aging at 150°C, the CuSn IMC thickness is approximately 10 μm, and the total IMC thickness is nearly 15 μm.

Table I. Diffusion Coefficients of Cu and Ni into Solid or Liquid Sn

Temperature	Cu	Ni
150°C (Solid Sn)	1.96×10^{-7} cm^2/s	3.79×10^{-9} cm^2/s
287°C (Liquid Sn)	4.13×10^{-5} cm^2/s	3.92×10^{-5} cm^2/s

A brightly colored layer was observed between the electroless Ni/Au pads and the (Cu, Ni)$_6Sn_5$ IMCs. The FIB images in Fig. 11 show that a bright layer with a thickness of approximately 200 nm is present at the electroless Ni/(Cu, Ni)$_6Sn_5$ IMC interface. The atomic concentration of this layer is similar to that of (Cu, Ni)$_6Sn_5$, but Au is also present in this layer, as shown in the WDS analysis results in Fig. 12. The atomic percentage of Au is in the range of 2% to 3%. To identify the phase of this layer, a TEM selected-area electron diffraction (SAED) analysis was performed. Figures 13 and 14 show TEM bright-field images and TEM diffraction images



(a)

Position	Cu	Ni	Sn	Au
1	50.7	-	47.2	0.5
2	43.6	9.6	46.3	0.5
3	32.4	22.2	43.5	1.9

(b)

Fig. 10. SEM-EDS spot analysis results of (Cu, Ni)$_6Sn_5$ IMCs at SnAg/electroless Ni-Au pad interface: (a) SEM image and (b) EDS spot analysis result (units: at.%).

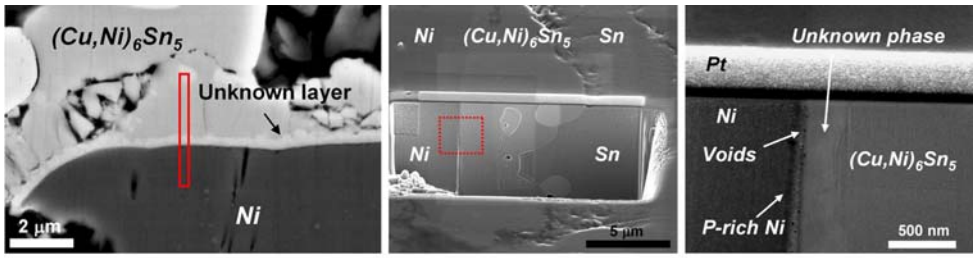


Fig. 11. FIB images of SnAg solder and electroless Ni-Au pad interface after 500 h aging at 150°C: (a) SEM image, (b) FIB image, and (c) magnified FIB image of the box area of (b).

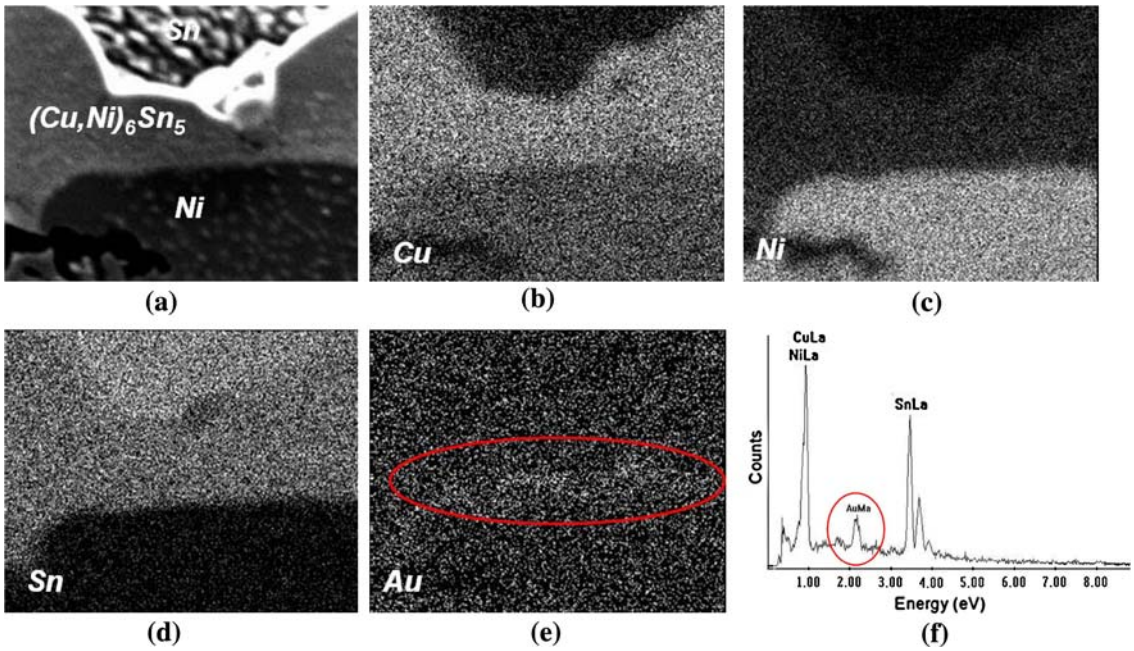


Fig. 12. WDS mapping result of the SnAg solder and electroless Ni-Au pad interface: (a) SEM image, (b) Cu mapping, (c) Ni mapping, (d) Sn mapping, (e) Au mapping, and (f) WDS spot analysis of an Au-rich area between the $(Cu, Ni)_6Sn_5$ IMC and the Ni pad.

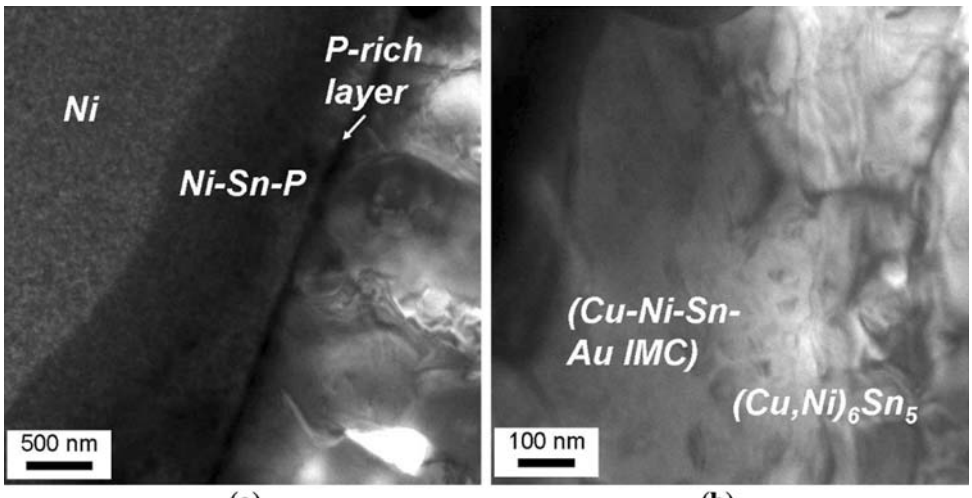


Fig. 13. TEM bright-field images at the SnAg/Ni interface: (a) PCB electroless Ni pad and solder interface and (b) Cu-Ni-Sn-Au quaternary IMC and $(Cu, Ni)_6Sn_5$ IMC on a PCB Ni pad.

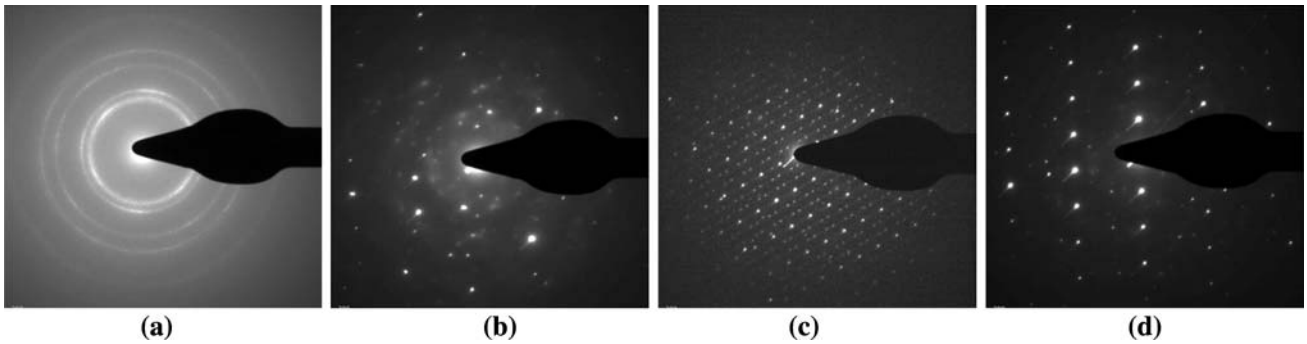


Fig. 14. TEM diffraction patterns of each phase at the SnAg/Ni interface: (a) electroless Ni (crystallized), (b) P-rich Ni layer (amorphous), (c) Cu-Ni-Sn-Au IMC, and (d) (Cu, Ni)$_6$Sn$_5$.

of each phase in the Cu/SnAg double-bump joints. Two weak spots are visible between the strong spots that are the lattice points of the Cu_6Sn_5 IMCs. These two weak spots are due to the Au atoms. The ordered distribution of the Au atoms makes up a superlattice structure that is three times larger than the Cu_6Sn_5 IMC.[10] This shows that the Au atoms that were not fully dissolved into the SnAg solder during the flip-chip assembly contribute to the formation of a CuNiAuSn quaternary IMC. However, this thermal history does not reduce the interfacial adhesion.

Figures 15 and 16 show schematically the changes in morphology that are due to interfacial reactions in the Cu/SnAg double-bump joints. First, metal atoms such as Au, Ni, and Cu dissolve into the solder during the reflow step of the flip-chip assembly process. During this process, a thin Cu_6Sn_5 IMC forms on the Cu column side, and a CuNiSnAu quaternary IMC forms on the PCB pad side. When there are additional solder reflows, scallop-like Cu_6Sn_5 IMCs grow on the Cu column side, and needle-like Ni_3Sn_4 and scallop-like (Cu, Ni)$_6$Sn$_5$ IMCs form and grow on the PCB pad side. As the number of reflows increases, the size of the Cu_6Sn_5 IMCs increases, and the IMC phases on the PCB pad side are converted to (Cu, Ni)$_6$Sn$_5$ IMCs.

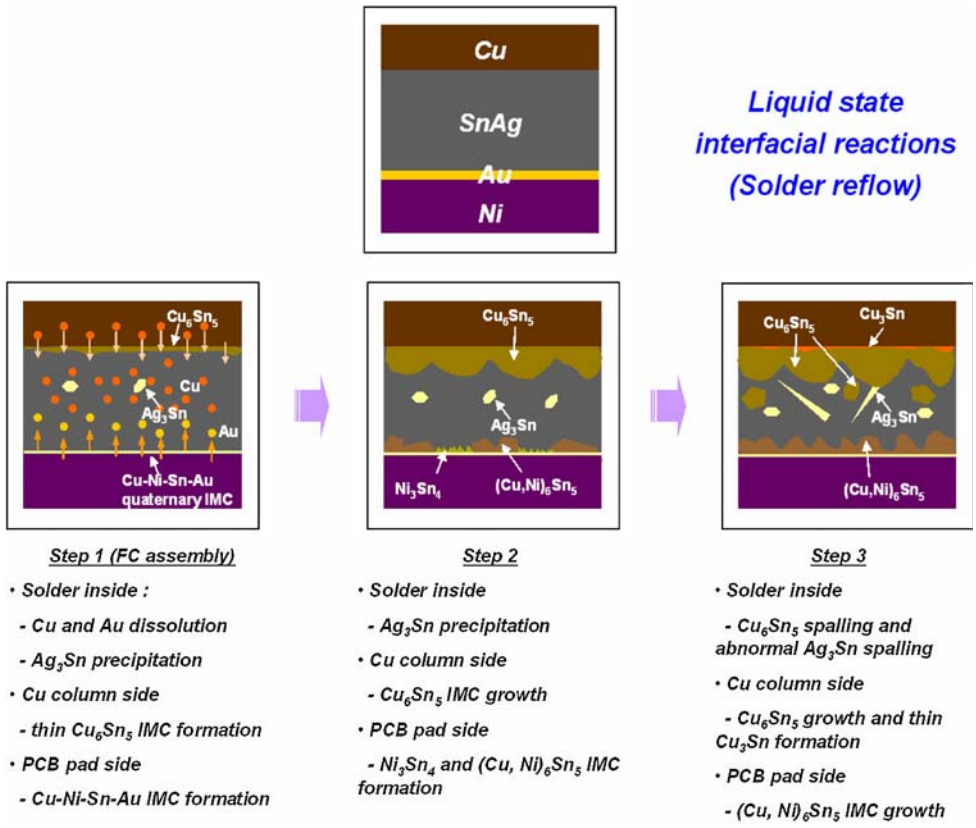


Fig. 15. Schematic illustration of interfacial reactions in Cu/SnAg double-bump joints after solder reflows.

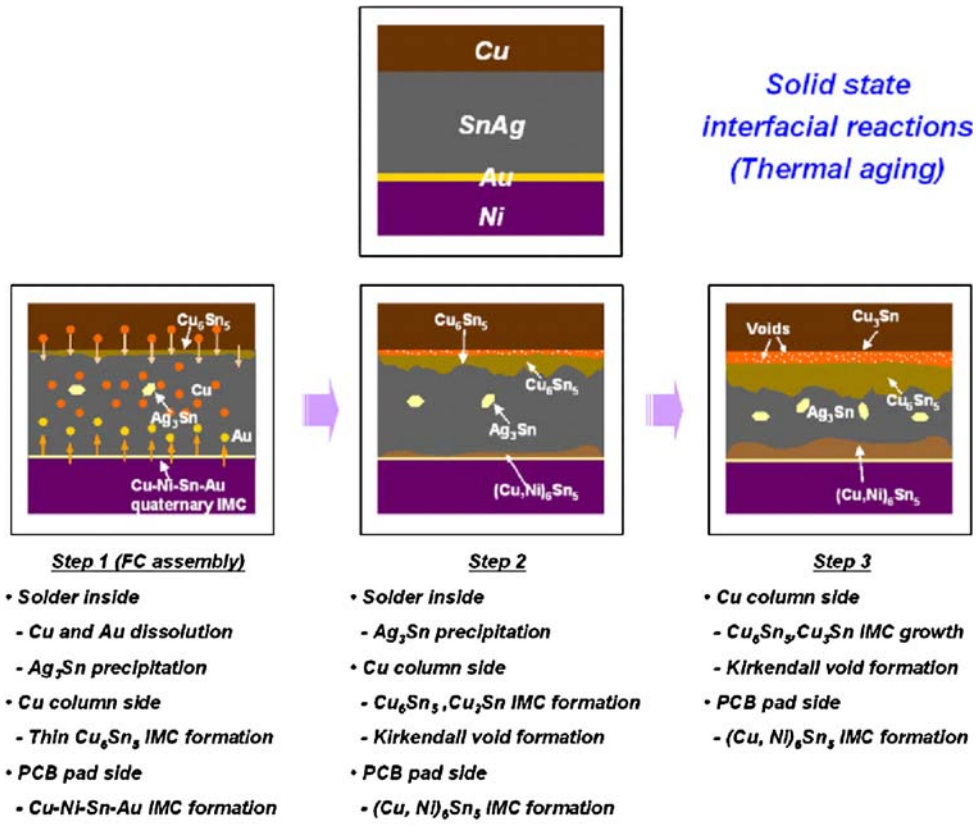


Fig. 16. Schematic illustration of interfacial reactions in Cu/SnAg double-bump joints after thermal aging.

The spalling of abnormal Ag_3Sn and Cu_6Sn_5 IMCs can also occur. In the case of thermal aging, layered Cu_3Sn IMCs as well as Cu_6Sn_5 IMCs form on the Cu column side. The roughness of the Cu_6Sn_5 IMCs is then less than that of the Cu_6Sn_5 IMCs after the solder reflows, and its morphology resembled that of a layered IMC. As the thermal aging time increases, the thickness of the Cu_3Sn and Cu_6Sn_5 IMCs on the Cu column side and the $(Cu, Ni)_6Sn_5$ IMCs on the PCB pad side increase. As a result of the dissolution of the Cu_6Sn_5 phase, Kirkendall voids form in the Cu_3Sn IMC layer and along the Cu column/Cu_3Sn IMC interface.

Figure 17 shows the bump contact resistance of a Cu/SnAg double-bump joint after multiple reflows. As shown in Figs. 4 and 5, the formation of thick IMCs between the Cu column bump and the electroless Ni/Au pad can lead to an increase in the bump contact resistance. Cu_6Sn_5 and Ni_3Sn_4 have larger electrical conductivities than Cu or Ni. However, the formation of a thick IMC after multiple reflows does not affect the electrical contact resistance.

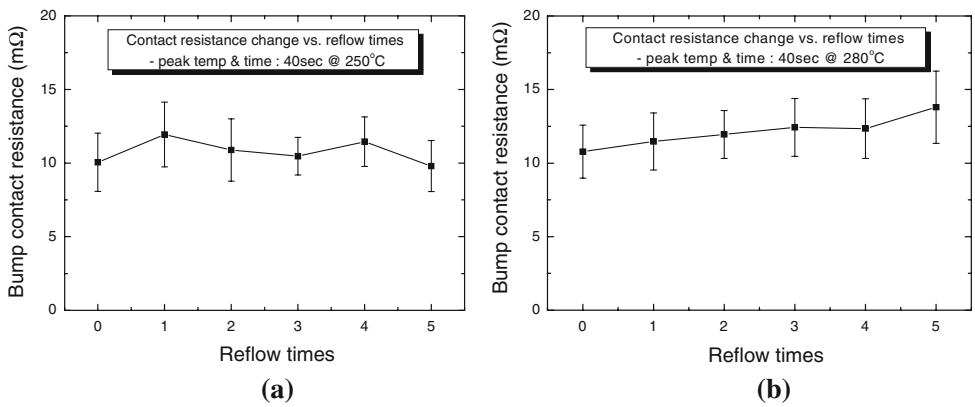


Fig. 17. Contact resistance changes after multiple solder reflows at (a) 250°C and (b) 280°C.

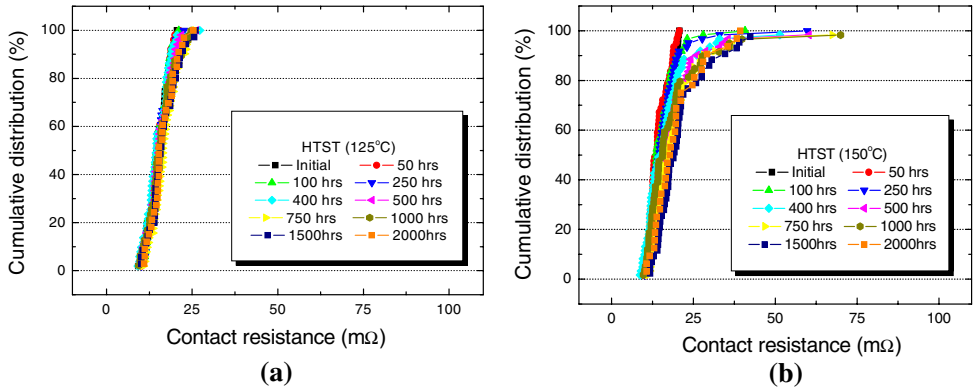


Fig. 18. Cumulative distribution after thermal aging at (a) 125°C and (b) 150°C.

Figure 18 shows the cumulative distribution of the bump contact resistance after thermal aging. These results correspond to those of high-temperature storage tests (HTST). After testing for 2000 h at 125°C, there is no change in the contact resistance. The contact resistances of some Cu/SnAg double bumps slightly increase at 150°C as the aging time increased, and one was electrically opened. This suggests that the formation of Kirkendall voids inside the Cu_3Sn IMCs and linked voids along the Cu column/Cu_3Sn interface result in a reduction in the contact resistance, because these voids reduce the contact area of the Cu and Cu_3Sn IMC interfaces. Void formation at the Cu/SnAg interface should be restricted, as it affects mechanical joint reliability factors such as drop-test reliability and electrical contact resistance.[14]

CONCLUSIONS

In this study, the interfacial reactions of Cu (60 μm)/SnAg (20 μm) double-bump flip-chip assemblies with a pitch of 100 μm were investigated. During multiple reflows, Cu_6Sn_5 IMCs form at the Cu column/SnAg solder interface, and Ni_3Sn_4 and (Cu, $Ni)_6Sn_5$ IMCs form at the SnAg solder/electroless NiAu interface. Abnormal Ag_3Sn IMCs were detected in the SnAg solder. For reflows at 280°C, nearly all of the SnAg solder is consumed, and the total IMC thickness reaches 10 μm. However, the large amount of IMC growth and solder consumption does not alter the bump contact resistance, even after five reflows at 280°C.

The changes in the IMC type and contact resistance after thermal aging are different from those resulting from multiple reflows. At the Cu column/SnAg solder interface, scallop-like Cu_6Sn_5 and dark, layered Cu_3Sn IMCs form. Additionally, (Cu, $Ni)_6Sn_5$ and CuNiAuSn quaternary IMCs form at the SnAg solder/electroless NiAu interface, whereas no Ag_3Sn IMCs were observed. The consumption rate of the SnAg solder is slower during thermal aging than during multiple reflows, but the formation of Kirkendall and linked voids leads to the deterioration of the electrical contact resistance. Due to Cu_3Sn formation, voids form inside the Cu_3Sn IMCs and along the Cu_3Sn/Cu column interface. The formation of these voids becomes more evident as the aging temperature and time increased. After aging at 150°C, the contact resistance of the Cu/SnAg double bumps increase slightly, and one of them underwent open-circuit failure.

In conclusion, Cu/SnAg double-bump flip-chip assemblies were found to have generally stable thermal reliability in spite of the formation of thick IMCs and excessive solder consumption, which results from its small solder volume. However, it was found that void formation, which can result in an increase in the electrical contact resistance, occurs during thermal aging at 150°C, and should be restricted.

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