

ZnO TFT Devices Built on Glass Substrates

J. ZHU,¹ H. CHEN,¹ G. SARAF,¹ Z. DUAN,¹ Y. LU,^{1,3} and S.T. HSU²

1.—Department of Electrical and Computer Engineering, Rutgers University, 94 Brett Road, Piscataway, NJ 08854, USA. 2.—Sharp Laboratories of America, Inc., 5700 NW Pacific Rim Boulevard, Camas, WA 98607, USA. 3.—e-mail: ylu@rci.rutgers.edu

ZnO thin-film transistors (TFTs) were built on glass substrates. The device with a top gate configuration operates in the depletion mode. The ZnO channel was grown by metalorganic chemical vapor deposition (MOCVD) on glass at low temperature. SiO₂ was used as the gate dielectric. The TFT has an on/off ratio of $\sim 4.0 \times 10^4$ and a channel field-effect mobility of $\sim 4.0 \text{ cm}^2/\text{V s}$. The average transmittance of the ZnO film in the visible wavelength is $\sim 80\%$. To compare the characteristics of the TFTs prepared by using a poly-ZnO and epitaxial-ZnO channel, an epi-ZnO TFT with the same configuration and dimensions was made on an r-Al₂O₃ substrate. The epi-ZnO TFT shows higher field-effect mobility of $\sim 35 \text{ cm}^2/\text{V s}$ and on/off ratio of $\sim 10^8$.

Key words: Thin-film transistor, ZnO, MOCVD

INTRODUCTION

As a wide-bandgap semiconducting material, zinc oxide (ZnO) has found promising applications in optoelectronics. Due to its intrinsic advantages, such as insensitivity to visible light and high electron mobility, ZnO-based thin-film transistors have attracted increasing interest as an alternative for Si-based TFT devices for active-matrix liquid-crystal displays (AMLCDs) and the transparent electronics.

Currently, most of the ZnO-based TFT devices have been fabricated on thermally oxidized Si and glass substrates by radiofrequency (RF) sputtering or pulse laser deposition (PLD).^{1–11} Hoffman et al. have reported transparent ZnO-based TFTs built on glass substrates.¹ The bottom gate TFT device consists of a sputtered indium tin oxide (ITO) bottom electrode, an aluminum-titanium oxide (ATO) gate insulator grown by atomic layer deposition, and a ZnO channel layer deposited by ion beam sputtering. The TFT working in *n*-type enhancement mode shows an on/off ratio of $\sim 10^7$. Threshold voltages and channel mobilities of devices range from $\sim 10 \text{ V}$ to 20 V and $\sim 0.3 \text{ cm}^2/\text{V s}$ to $2.5 \text{ cm}^2/\text{V s}$, respectively. Later, ZnO-TFTs² fabricated using a bottom

gate structure on thermally oxidized Si were also reported with an incremental mobility as high as $25 \text{ cm}^2/\text{V s}$ under V_{GS} of -5 V to 70 V and V_{DS} of 10 V . Masuda et al.³ reported bottom gate ZnO TFTs fabricated on glass and Si substrates with the ZnO channel layer deposited by PLD at 450°C . The TFT made on a thermally oxidized Si substrate operates in the enhance mode for the low carrier concentration ZnO channel with a field-effect mobility of $\sim 0.031 \text{ cm}^2/\text{V s}$, threshold voltage of $\sim 2.5 \text{ V}$, and on/off ratio of $\sim 10^5$. For the high carrier concentration ZnO channel, the device operates in the depletion mode and exhibits a field-effect mobility of $\sim 0.97 \text{ cm}^2/\text{V s}$, threshold voltage of $\sim -1.0 \text{ V}$, and on/off ratio of $\sim 10^2$. ZnO TFTs built on glass substrates operate in the depletion mode and the drain current is much higher than that of devices made on Si substrates. These TFTs show poor saturation current properties and do not reach cut off within the applied bias limit. This is attributed to the poorer crystallinity and higher background electron concentration in the ZnO channel layer on the glass substrate.

In ZnO TFTs, material properties of the ZnO channel, including the mobility, carrier concentration, and surface roughness, etc., have a critical impact on the device performance. The MOCVD technique enables low-temperature and high-quality ZnO growth on various substrates, particularly

(Received November 28, 2007; accepted March 19, 2008; published online May 2, 2008)

benefiting the development of high-performance ZnO thin-film transistors. So far, most reported ZnO TFTs have used the bottom gate configuration, where the coverage of the final passivation layer dynamically impacts on device performance by changing the surface status of the ZnO film.⁴ The top gate device structure can avoid the direct contact of the passivation layer with the ZnO channel, and thus limit this effect.

In this paper, we present results of ZnO TFTs with a top gate device configuration. The ZnO channel layer is deposited on a glass substrate by using the MOCVD technique. TFTs of the same dimension but with epitaxial ZnO channels were also made on the r-Al₂O₃ substrates. Device performance was evaluated and the results were also compared with that of ZnO TFTs built on glass substrates.

EXPERIMENTAL

The ZnO film growth was carried out in a vertical flow, rotating disc MOCVD reactor. Corning 7059 glass was used as the substrate. Diethylzinc (DEZn) and oxygen were used as the Zn precursor and oxidizer, respectively. The chamber pressure was kept at ~50 torr. The growth rates of ZnO in different crystalline directions follow the order: [0001] > [01 $\bar{1}$ 0] > [01 $\bar{1}$ 1] > [000 $\bar{1}$]. The as-grown ZnO film usually exhibits a columnar structure on glass substrates due to the fastest growth rate along the ZnO [0001] direction.¹² In ZnO TFT devices, such a columnar structure should be avoided, as it blocks the lateral current flow and presents the rough surface morphology for the device processing. The growth temperature plays a critical role in determining the morphology and electrical properties of the ZnO films. To obtain a dense ZnO film structure, the growth temperature was kept at ~400°C. At this low growth temperature, the zinc precursor and oxygen have lower kinetic energies and growth is controlled by surface kinetics, resulting in a dense film structure with smooth surface. For the growth of the epitaxial ZnO channel layer on r-Al₂O₃ substrates, the MOCVD growth temperature was maintained at 400°C to 500°C. The surface morphology of the as-grown ZnO films was examined using a Leo-Zeiss field emission electron microscope (FESEM). The X-ray scan of the ZnO film grown on glass was carried out using a Siemens D310 X-ray diffraction (XRD) system, while for the ZnO film grown on the r-Al₂O₃ substrate, high-resolution XRD analysis was carried out using a Bruker (Bruker AXS GmbH, Karlsruhe, Germany) D8-Discover four-circle X-ray system.

The ZnO TFTs in this study were defined as top gate depletion-mode metal insulator semiconductor (MIS) FET devices. The *n*-type semiconducting ZnO channel layer (70 nm to 100 nm) was grown on a glass substrate by MOCVD. The channel mesa was formed by the wet chemical etching by using

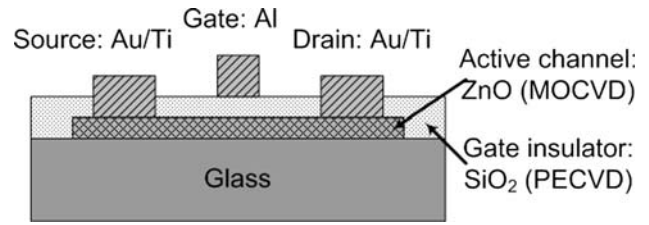


Fig. 1. Schematic representation of the ZnO TFT device on a glass substrate.

HCl:H₂O solution.¹³ A SiO₂ layer (~120 nm) deposited by plasma enhanced chemical vapor deposition (PECVD) was used as the gate dielectric. The source and drain windows were opened on SiO₂ using buffered oxide etch (BOE). Au/Ti metal scheme (50/100 nm) was used for the source and drain ohmic contacts, and the contact patterns were formed by the liftoff process. Al (150 nm) was used for the top electrode. The TFT dimensions were a 300 μ m channel width and 50 μ m channel length with a *W/L* ratio of 6. Figure 1 shows a schematic of the device structure. The ZnO TFT device characteristics were evaluated using an HP 4156C semiconductor parameter analyzer. The optical transmittances of the ZnO films grown on glass substrates were measured between wavelengths of 370 nm and 700 nm.

RESULTS AND DISCUSSION

The XRD measurement result of the ZnO film grown on a glass substrate is shown in Fig. 2. The inset shows the surface morphology of the sample characterized by FESEM. Multiple ZnO reflection peaks were observed from the coupled X-ray scan, indicating that the film is polycrystalline. This is expected due to the lack of epitaxial relationship between ZnO and the glass substrate.

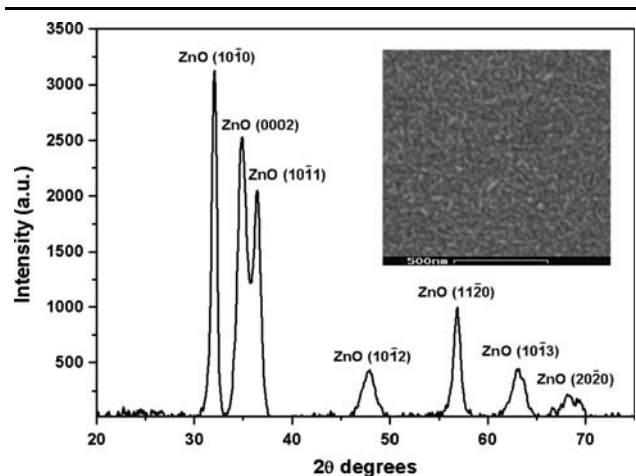


Fig. 2. X-ray θ - 2θ scan of the ZnO film grown on glass using MOCVD; the inset shows an SEM micrograph of a ZnO film deposited on a glass substrate.

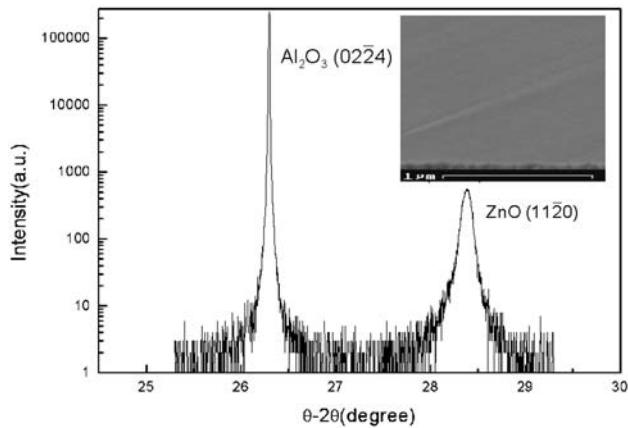


Fig. 3. X-ray θ - 2θ scan of the ZnO film grown on the r- Al_2O_3 substrate using MOCVD; the inset shows an SEM micrograph of a as-grown ZnO film.

Furthermore, the low deposition temperature to suppress columnar growth also leads to polycrystallinity in the ZnO film. From the SEM micrograph, it can be seen that the film is dense and uniform with nanoscale surface roughness.

Figure 3 shows the XRD θ - 2θ scan of the ZnO film grown on the r- Al_2O_3 substrate. The inset shows the SEM image of the ZnO film. The ZnO films are epitaxial and a-plane oriented, as seen from the coupled X-ray scan. The epitaxial relationships between the a-plane ZnO film and r- Al_2O_3 substrate are: $(11\bar{2}0)$ ZnO \parallel $(01\bar{1}2)$ Al_2O_3 , and $[0001]$ ZnO \parallel $[0111]$ Al_2O_3 . The SEM image exhibits a smoother surface morphology of the epitaxial ZnO layer in comparison to the film grown on the glass substrate. The transmission of the ZnO TFT built on the glass substrate was measured in the wavelength range from 370 nm to 700 nm by using a Beckman DU 530 spectrophotometer. The observed average transmittance was $\sim 80\%$.

Figure 4a and b shows the output and transfer characteristics of a ZnO TFT device built on the glass substrate, respectively. From Fig. 4a, it can be seen that the TFT shows saturation and cut off under proper biases. The device works in the depletion mode, as the source-drain current is non-zero when the gate bias V_{GS} is 0 V. The MOCVD-grown ZnO films have a carrier concentration of 10^{17} cm^{-3} to 10^{18} cm^{-3} . In Fig. 4a, the values of V_{GS} change from 0 V to -40 V, while V_{DS} increases from 0 V to $+15$ V. The I_{D} versus V_{GS} and transconductance plot are shown in Fig. 4b, where the device has an on/off ratio of $\sim 4.0 \times 10^4$ and a maximal transconductance g_{m} of $\sim 0.15 \text{ mS/mm}$. The subthreshold slope is determined to be $S = 3.56 \text{ V/decade}$ by linearly fitting to the I_{D} curve in the region with the maximum slope over a 500 mV range. The field-effect mobility of the device was obtained by the nonlinear fitting of the I_{D} versus V_{GS} curve under the gate voltage (-17 V), which corresponds to the

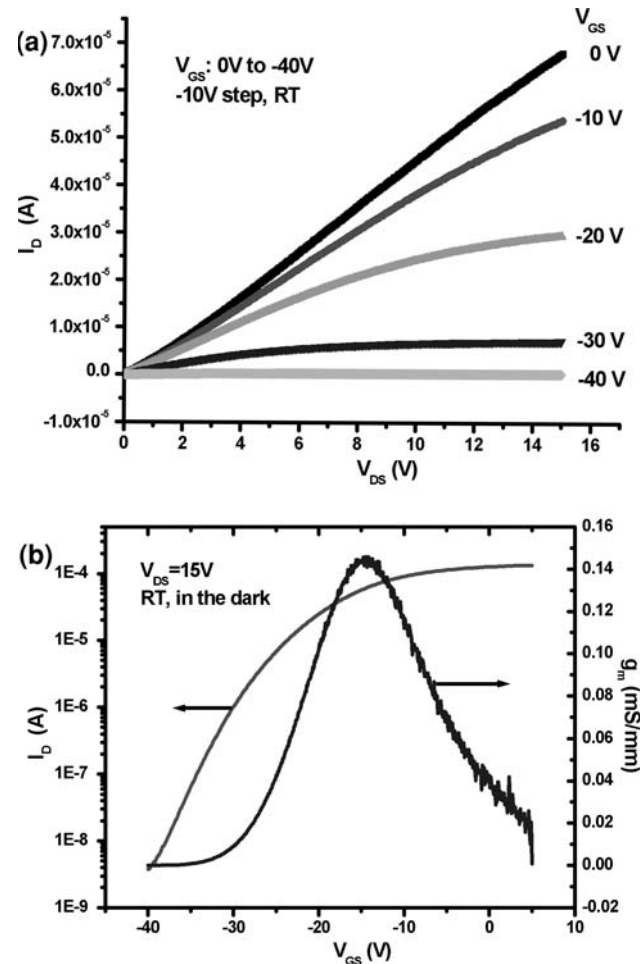


Fig. 4. ZnO TFT on glass substrate: (a) transistor output I_{D} versus V_{DS} curve. V_{GS} increases with -10 V/step ; (b) transfer characteristics for a gate sweep from $+5 \text{ V}$ to -40 V . The drain voltage was $+15 \text{ V}$.

maximum transconductance g_{max} . The curve fitting function used was:

$$I_{\text{D}} = \frac{W}{2L} \times C_{\text{i}} \times \mu_{\text{FE}} \times (V_{\text{GS}} - V_{\text{th}})^2,$$

where W is the channel width, L is the channel length, C_{i} is the capacitance per unit area of the gate insulator, V_{th} is the threshold voltage, and μ_{FE} is the device field-effect mobility. The extracted μ_{FE} value is $\sim 4.0 \text{ cm}^2/\text{V s}$ and V_{th} is $\sim -29.6 \text{ V}$.

For comparison, we also made TFTs with the same dimensions and configuration but grown epitaxially on the r- Al_2O_3 substrate. Figure 5a and b shows the measured output and transfer characteristics of a ZnO TFT built on an r- Al_2O_3 substrate. The device demonstrates better characteristics than that built on the glass substrate. The TFT has an on/off ratio of $\sim 10^8$. The determined subthreshold slope is 0.94 V/decade . The subthreshold difference between the TFT on glass and sapphire results from the rougher surface and poorer crystallinity of ZnO films on glass substrates. After the SiO_2 gate dielectric deposition, the higher interface state

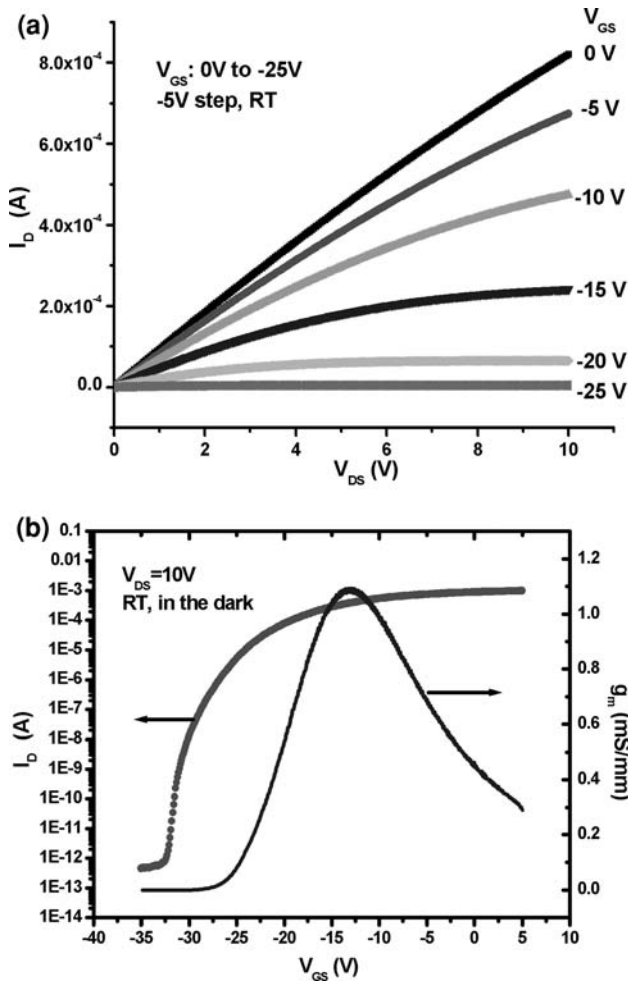


Fig. 5. ZnO TFT on the $r\text{-Al}_2\text{O}_3$ substrate: (a) transistor output I_D versus V_{DS} curve. V_{GS} increases with -5 V/step; and (b) transfer characteristics for a gate sweep from $+5$ V to -35 V. The drain voltage was $+10$ V.

density at the SiO_2/ZnO interface results in the larger subthreshold slope in the TFT devices on the glass substrate. The extracted field-effect mobility of ~ 35 $\text{cm}^2/\text{V s}$ and the threshold voltage of -25.4 V are obtained for the epitaxial ZnO TFT. In comparison to the polycrystalline ZnO TFT built on glass, the epitaxial ZnO TFT built on the $r\text{-Al}_2\text{O}_3$

substrate shows much better characteristics due to the superior material properties.

CONCLUSIONS

In summary, ZnO-based TFT devices with high electron field-effect mobility were fabricated on glass substrates. To suppress the columnar growth of the ZnO film on the glass substrate, low-temperature deposition was used during the MOCVD growth. The device parameters extracted from the measured transistor output and transfer characteristics correspond to an on/off ratio of $\sim 4.0 \times 10^4$ and a maximal transconductance g_m of ~ 0.15 mS/mm. The device field-effect channel mobility was determined to be on the order of ~ 4.0 $\text{cm}^2/\text{V s}$. In comparison, TFTs with the epitaxial ZnO channel built on $r\text{-Al}_2\text{O}_3$ substrates exhibited a higher on/off ratio of $\sim 10^8$ and field-effect mobility of ~ 35 $\text{cm}^2/\text{V s}$.

REFERENCES

1. R.L. Hoffman, B.J. Norris, and J.F. Wager, *Appl. Phys. Lett.* 82, 733 (2003). doi:10.1063/1.1542677.
2. R.L. Hoffman, *J. Appl. Phys.* 95, 5813 (2004). doi:10.1063/1.1712015.
3. S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, *J. Appl. Phys.* 93, 1624 (2003). doi:10.1063/1.1534627.
4. D. Hong and J.F. Wager, *J. Vac. Sci. Technol. B* 23, L25 (2005). doi:10.1116/1.2127954.
5. E.M.C. Fortunato, P.M.C. Barquinha, A.C.M.B.G. Pimentel, A.M.F. Gonçalves, A.J.S. Marques, R.F.P. Martins, and L.M.N. Pereira, *Appl. Phys. Lett.* 85, 2541 (2004). doi:10.1063/1.1790587.
6. H.S. Bae and S. Im, *Thin Solid Films* 469–470, 75 (2004). doi:10.1016/j.tsf.2004.06.196.
7. I.D. Kim, Y. Choi, and H.L. Tuller, *Appl. Phys. Lett.* 87, 043509 (2005). doi:10.1063/1.1993762.
8. P.F. Carcia, R.S. McLean, and M.H. Reilly, *Appl. Phys. Lett.* 88, 123509 (2006). doi:10.1063/1.2188379.
9. J. Siddiqui, E. Cagin, D. Chen, and J.D. Phillips, *Appl. Phys. Lett.* 88, 212903 (2006). doi:10.1063/1.2204574.
10. H.H. Hsieh and C.C. Wu, *Appl. Phys. Lett.* 89, 041109 (2006). doi:10.1063/1.2235895.
11. Y.L. Wang, F. Ren, W. Lim, D.P. Norton, S.J. Pearton, I.I. Kravchenko, and J.M. Zavada, *Appl. Phys. Lett.* 90, 232103 (2007). doi:10.1063/1.2746084.
12. M. Yan, H.T. Zhang, E.J. Widjaja, and R.P.H. Chang, *J. Appl. Phys.* 94, 5240 (2003). doi:10.1063/1.1608473.
13. J. Zhu, N.W. Emanetoglu, Y. Chen, and Y. Lu, *J. Electron. Mater.* 33, 556 (2004). doi:10.1007/s11664-004-0046-5.