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Fabrication of Strained-Si/Strained-Ge Heterostructures on Insulator

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Ultrathin strained-Si/strained-Ge heterostructures on insulator have been fabricated using a bond and etch-back technique. The substrate consists of a trilayer of 9 nm strained-Si/4 nm strained-Ge/3 nm strained-Si on a 400-nm-thick buried oxide. The epitaxial trilayer structure was originally grown pseudomorphic to a relaxed $Si_{0.5}Ge_{0.5}$ layer on a donor substrate. Raman analysis of the as-grown and final transferred layer structures indicates that there is little change in the strain in the Si and Ge layers after layer transfer. These ultrathin Si and Ge films have very high levels of strain (~1.8% biaxial tension and 1.4% compression, respectively), and are suitable for enhanced-mobility field-effect transistor applications.

Key words: Strained-Si, strained-Ge, heterostructure on insulator, UTB MOSFETs, high-mobility substrate, bond and etch-back

INTRODUCTION

Historically, geometric scaling of Si CMOS has fueled the progression from one technology node to the next. This scaling trend has enabled both a higher device packing density and a reduction in inverter delay. The need to continue performance improvement that is commensurate with geometric scaling has motivated the study of high-mobility channel materials and the use of ultrathin-body metal oxide semiconductor field-effect transistor (MOSFET) architectures. Strained-Si/strained-Ge heterostructure MOSFETs on bulk substrates have been investigated previously and show a ~10 times enhancement in effective hole mobility when the Ge is pseudomorphic to relaxed $Si_{0.5}Ge_{0.5}$.[1] The discontinuity in the valence band at the strained-Si/strained-Ge heterointerface confines carriers in the high-mobility strained-Ge buried layer. The significant mobility enhancement observed in the strained-Si/strained-Ge heterostructure provides incentives to explore the fabrication of these materials in ultrathin-body structures. In this work, for the first time, strained-Si/strained-Ge (Ge HOI) heterostructure on insulator substrates are fabricated. A low-temperature bond and etch-back process was utilized to fabricate these substrates. Low-temperature processing is required to avoid both strain relaxation and Ge diffusion. The diffusivity of Ge has been observed to be enhanced in Si/SiGe heterostructures when the SiGe layer is under compressive strain.[2] Raman analysis and X-ray diffraction (XRD) were conducted on blanket unpatterned substrates before and after bonding. XRD analysis was primarily utilized to determine the Ge content of the buried Ge layer (since some interdiffusion may be expected during wafer processing) and Raman analysis was used to estimate the level of strain in the structures.

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EXPERIMENTAL DETAILS

Substrate fabrication is illustrated in Fig. 1 and follows a sequence similar to that used by Aberg et al. for the fabrication of strained Si/SiGe (55% Ge) heterostructures on insulator.[3] The process begins with the epitaxial growth of an etch-back structure

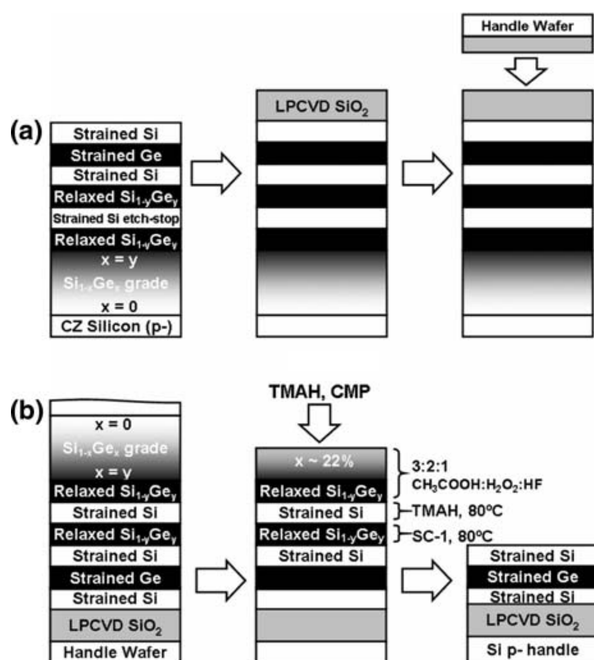

Fig. 1. Schematic illustration of the bond and etch-back process, including (a) epitaxial growth, planarization, and bonding, and (b) substrate grinding and etch-back. A series of chemical etches are utilized to remove SiGe grade, relaxed buffer, and etch-stops, providing the final Ge HOI substrate.

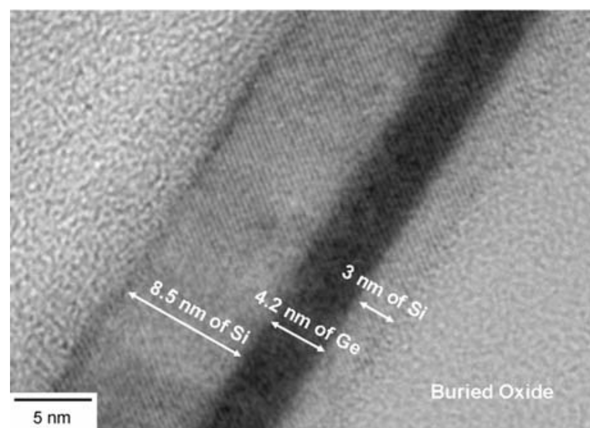

Fig. 2. Cross-sectional transmission electron microscopy image of the final Ge HOI substrate. The layers in this structure were grown to be pseudomorphic to relaxed $Si_{0.5}Ge_{0.5}$. An 8.5 nm strained Si cap is utilized to provide a high-quality dielectric interface to the structure. A 4.2 nm buried Ge layer serves as the high-mobility region for hole transport. The underlying 3 nm strained Si layer provides a high-quality dielectric interface with the buried oxide.

on 6-inch-diameter Si substrates in an Applied Materials Epi Centura LPCVD reactor.[3] The etch-back structure consists of a graded SiGe layer, a relaxed $Si_{1-y}Ge_y$ buffer, dual strained-Si/relaxed-SiGe etch-stop layers, and the stained-Si/strained-Ge/strained-Si heterostructure, as illustrated in Fig. 1a. Relaxed buffer layers using the grading technique are utilized,[4,5] with a final Ge content in the relaxed layer, y, of 0.5.

Once the etch-back structures are grown, the wafers are prepared for bonding. Low-temperature oxide (LTO) is deposited on the etch-back structure and densified for 2 h at 600°C. Chemical mechanical polishing (CMP) of the LTO was then conducted to reduce the crosshatch-induced roughness on the surface of the oxide. A handle wafer is also prepared by growing a thermal oxide on a p-CZ wafer. An oxide-to-oxide bond is utilized to fuse the two wafers together.[6] The bond process begins by cleaning the wafer pairs and then exposing them to an oxygen plasma. The wafers are then brought into forced contact and annealed to strengthen the bond. The post-bond annealing sequence consists of 3 h at 300°C, 30 min at 350°C, and a 15-min ramp to 550°C in nitrogen ambient. Wafer grinding is then conducted to remove most of the Si substrate on the etch-back structure.

After mechanical grinding is completed, the etch-back sequence begins by polishing the wafer surface to remove the scratches introduced during the grinding process. The remaining Si substrate, SiGe grade, relaxed buffer, and etch stops are chemically removed to expose the strained-Si/strained-Ge heterostructure on insulator.[3,7,8] Figure 1b illustrates the etch-back process and the final Ge HOI substrate. A high-magnification cross-sectional transmission electron micrograph of the strained-Si/strained-Ge heterostructure on insulator is shown in Fig. 2.

Raman analysis was conducted on a blanket unpatterned etch-back structure prior to bonding to quantify the level of strain prior to bond and etch-back. The etch-back structure is depicted in Fig. 1a where the Si and Ge layers are targeted to be pseudomorphic to a $Si_{0.5}Ge_{0.5}$ relaxed buffer. Raman spectra were collected from this structure using photons at wavelengths of 364 nm and 514.5 nm excitation. Figure 3 shows ultraviolet (UV) and visible Raman spectra for the Ge–Ge and Si–Si LO phonons from bulk crystals (dotted curves) and the as-grown etch-back structure (solid curve). The spectra are fitted with Lorentzian line shapes with strain calculations based on adjustable fit parameters. Plasma lines, not shown in this spectrum, were fitted using Gaussian profiles in order to account for the thermal drift of the spectrometer. Each spectrum is comprised of a Ge–Ge band near 300 cm^{-1} from the Ge layer and a Si–Si band near 520 cm^{-1} from the strained Si cap. Based on a Ge–Ge frequency shift of +7.69 cm^{-1} from bulk Ge and a strain shift coefficient of –415 cm^{-1},[9] the in-plane biaxial strain is –1.85%. When modeling the buried layer as pure Ge, the relaxation is near $\sim$16%.

High-resolution X-ray diffraction and modeling analysis were also performed on the samples. Figure 4 presents the (224) reciprocal space map (RSM) plotted in reciprocal lattice units taken around the Si(224) grazing exit (GE) asymmetric

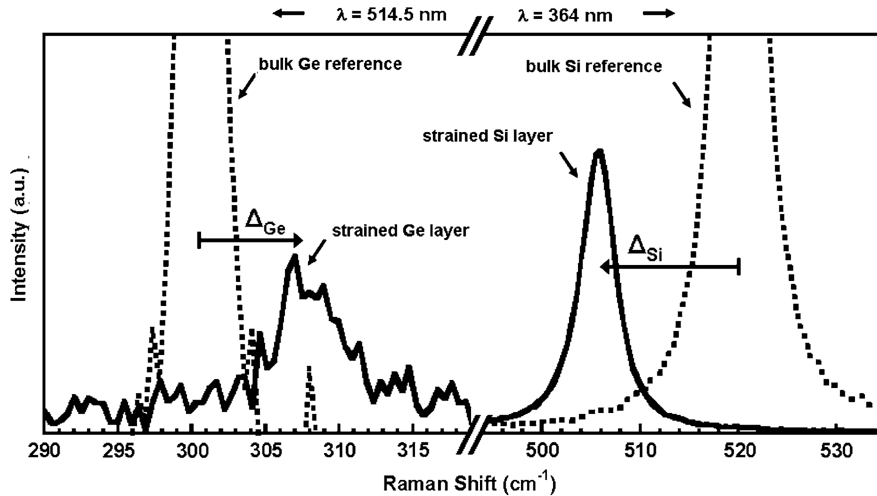

Fig. 3. Raman spectra from the as-grown etch-back structure using 364 nm and 514 nm excitation for the Ge–Ge and Si–Si LO phonons from bulk crystals (dotted black curves) and the as-grown etch-back structure (black solid curve). The spectrum is comprised of a Ge–Ge band near 300 cm^{-1} from the Ge layer, and a Si–Si band near 520 cm^{-1} from the strained Si cap. The measured Ge and Si bands are shifted due to compressive and tensile strain, respectively.

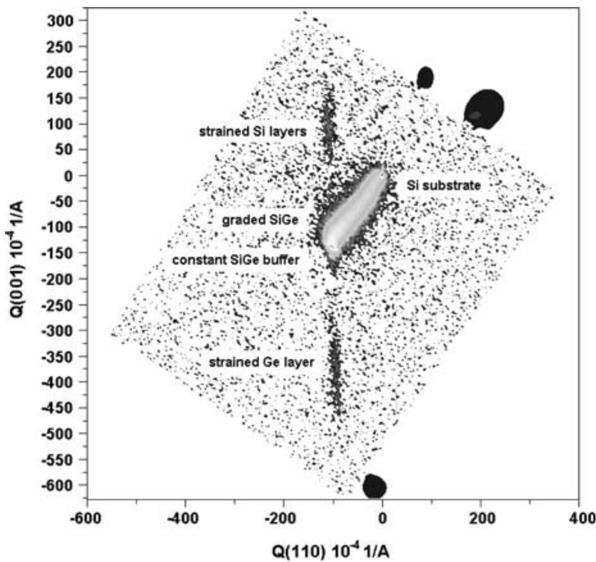

Fig. 4. XRD measurement of the as-grown etch-back structure. The Si and Ge layers are significantly tilted relative to the relaxed Si substrate due to tetragonal distortion of the lattice by strain. The strain and Ge content were determined based on line shape fits to the diffraction peaks in the reciprocal space map. The strain in the Si and Ge layers is +1.97% and –1.85%, respectively. The Ge content in the buried layer appears to be ~97 at.%.

reflection. The Si and Ge layers are tilted significantly relative to the relaxed Si substrate due to tetragonal distortion of the lattice by strain. Based on Gaussian line shape fits to the diffraction peaks, the angular coordinates for each layer uniquely define the layer's lattice parameters. For the most general case, the Ge layer was modeled as a Si-Ge alloy to account for potential Si and Ge interdiffusion. Using the calculated Ge layer lattice parameters, the relaxed lattice constant and corresponding composition was determined. A successive iteration between the composition, the compositionally dependent Poisson ratio, and the relaxed lattice constant converges for a given composition and relaxation. The data suggests as much as 3% to 4% interdiffusion between the Si and Ge layers.

RESULTS AND DISCUSSION

If the Ge layer is modeled as having a composition of $Si_{0.03}Ge_{0.97}$, the relaxation calculated from the measured Raman shift decreases to ~8%. Although the buried Ge layer was grown as a pure Ge layer, the subsequent growth of the Si cap layer at 600°C may have resulted in some Ge diffusion. The strained-Si layer has no measured relaxation with a strain shift of –14.67 cm^{-1}, corresponding to tensile strain of +1.97%.

After strained layer transfer onto a handle wafer, Raman analysis was conducted on a blanket unpatterned Ge HOI substrate, similar to the substrate depicted in Fig. 1b. These strain measurements were conducted on a Ge HOI substrate in which the Si and Ge layers were targeted to be pseudomorphic to a relaxed $Si_{0.5}Ge_{0.5}$ layer on the donor wafer. Raman spectra were collected from the substrate using the 364 nm and 514.5 nm Ar-ion excitation wavelengths. Figure 5 shows UV and visible Raman spectra for the Ge HOI substrate. Since the HOI structure is grown on a fully relaxed $Si_{0.5}Ge_{0.5}$ buffer, the Ge layer is modeled as being pseudomorphic to $Si_{0.5}Ge_{0.5}$. The buried Ge layer was initially modeled as a pure Ge layer assuming no interdiffusion. Based on a Ge–Ge frequency shift of +5.28 cm^{-1} from bulk Ge and a strain shift coefficient of –415 cm^{-1}, the in-plane biaxial strain is –1.27%, which represents a relaxation of ~40%.

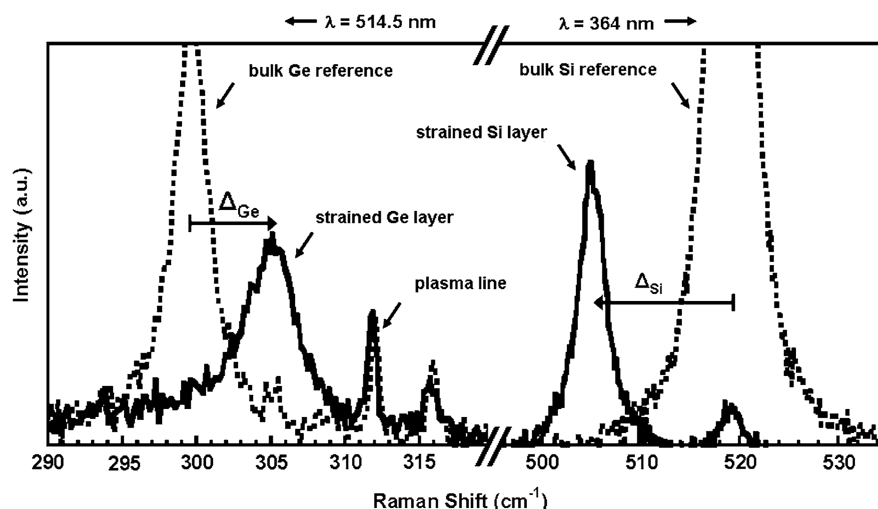

Fig. 5. Raman spectra from the Ge HOI substrate using 364 nm and 514.5 nm excitation to obtain signal from the Si cap and Ge buried layer, respectively. UV and visible Raman spectra are provided for the Ge–Ge and Si–Si LO phonons from bulk crystals (dotted black curves) and the Ge HOI substrate (black solid curve).

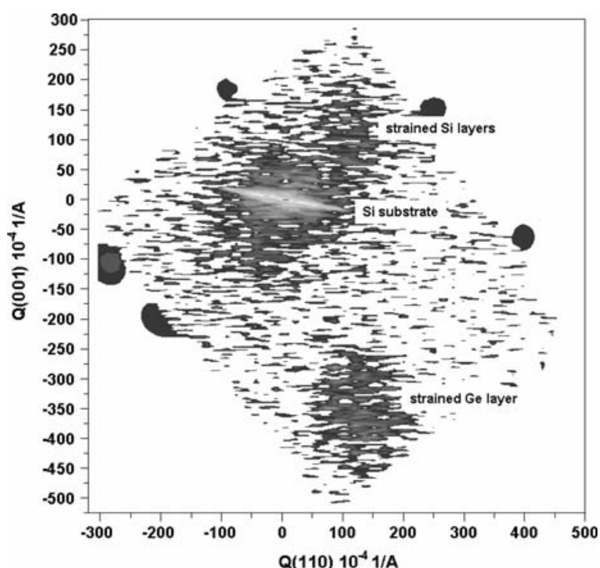

Fig. 6. XRD measurement of the Ge HOI substrate. The Si and Ge layers are tilted relative to the relaxed Si substrate due to tetragonal distortion of the lattice by strain. The strain and Ge content were determined based on line shape fits to the diffraction peaks in the reciprocal space map. The Ge content in the buried layer appears to be ~93 at.%.

Figure 6 shows the XRD (224) reciprocal space map (RSM) taken around the Si(224) grazing incidence (GI) asymmetric reflection. The GI geometry is used to enhance the sensitivity of the X-rays to the thin strained-Si and strained-Ge layers. The Si and Ge layers are tilted significantly relative to the substrate due to tetragonal distortion of the lattice by strain. In order to determine whether Si and Ge interdiffusion occurred, the Ge layer was modeled as a Si-Ge alloy which releases the constraint on the concentration. Using the peak position in the (224) RSM, the Ge content in the buried layer is estimated to be 93 at.%. The drop in Ge content of the buried Ge layer during HOI fabrication is conceivable, since the substrates undergo a significant thermal treatment during bonding (2 h at 600°C) which may cause interdiffusion between the Si and Ge. If this is taken into account and the Ge layer is modeled as a $Si_{0.07}Ge_{0.93}$ layer, then the relaxation calculated from the Raman shift is ~12%. The phonon width also yields information about the periodicity of the layer. In this case, the Ge mode is ~60% broader than the bulk peak, suggesting either some defects due to relaxation and/or some Si interdiffusion. Based on a Si–Si frequency shift of +14.09 cm^{-1} from bulk Si, the in-plane biaxial strain in the Si cap layer is +1.89%, which represents a relaxation of 3.4%. The Si cap phonon width shows only slight broadening at 11.1% over the bulk value, indicating excellent crystallinity.

CONCLUSIONS

This work exhibits fabrication of the first strained-Si/strained-Ge heterostructure on insulator. XRD reveals a drop in the peak Ge content to about ~97 at.% in the as-grown etch-back structure. Raman analysis of this structure reveals that the Ge layer is ~8% relaxed. Additional Si/Ge interdiffusion as well as relaxation in the Ge layer appears to occur during the bonding sequence. After layer transfer, the Ge content of the buried layer appears to drop to 93 at.% and the layer is about ~12% relaxed. Further optimization of the bond process is needed to limit the Si and Ge interdiffusion as well as the relaxation that occurs during substrate fabrication. The Si layers in the etch-back structure and final Ge HOI substrate are less than ~5% relaxed, indicating little change in the strained Si films upon layer transfer.

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