High-Quality Large-Area MBE HgCdTe/Si

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HgCdTe offers significant advantages over other similar semiconductors, which has made it the most widely utilized variable-gap material in infrared (IR) focal plane array (FPA) technology. HgCdTe hybrid FPAs consisting of two-dimensional detector arrays that are hybridized to Si readout circuits (ROIC) are the dominant technology for second-generation infrared systems. However, one of the main limitations of the HgCdTe materials system has been the size of lattice-matched bulk CdZnTe substrates, used for epitaxially grown HgCdTe, which have been limited to 30 cm^2 in production. This size limitation does not adequately support the increasing demand for larger FPA formats which now require sizes up to 2048 $\times$ 2048, and only a single die can be printed per wafer. Heteroepitaxial Si-based substrates offer a cost-effective technology that can be scaled to large wafer sizes and further offer a thermal-expansion-matched hybrid structure that is suitable for large format FPAs. This paper presents data on molecular-beam epitaxy (MBE)-grown HgCdTe/Si wafers with much improved materials characteristics than previously reported. We will present data on 4- and 6-in diameter HgCdTe both with extremely uniform composition and extremely low defects. Large-diameter HgCdTe/Si with nearly perfect compositional uniformity and ultra low defect density is essential for meeting the demanding specifications of large format FPAs.

Key words: Molecular-beam epitaxy (MBE), HgCdTe/Si, IRFPA, large-format

INTRODUCTION

The molecular-beam epitaxy (MBE) growth of HgCdTe on silicon substrates as large 6-in diameter is an extension of the 4-inch HgCdTe process developed at Raytheon Vision Systems (RVS, Goleta, CA). Shown in Fig. 1 is a photo of a 6-in HgCdTe/Si wafer. The 4-in HgCdTe/Si process is an adaptation of processes developed by HRL Laboratories (Malibu, CA) and other workers who have pioneered the methodology of growing both high-quality CdTe on smaller silicon substrates and subsequently HgCdTe on the CdTe/Si.[1–3] This entailed overcoming the sizable lattice mismatch between HgCdTe and silicon (~19%) and developing the proper buffer layer strategies to enable acceptable dislocation densities in the device layers. The current state-of-the-art dislocation densities for HgCdTe are in the mid-10^6 cm^{-2} range. Although this is an order of magnitude higher than that using bulk CdZnTe substrates, diodes fabricated from mid-wavelength MBE HgCdTe/Si substrates demonstrate comparable performance to mid-wave infrared (MWIR) diodes fabricated by either MBE or liquid-phase epitaxy (LPE) on bulk CdZnTe substrates.[4–6]

(Received November 7, 2005; accepted January 30, 2006)

ADVANTAGES OF LARGE-AREA HgCdTe/Si

The scale up of HgCdTe to 6-in diameter substrates offers many advantages over other infrared (IR) materials such as LPE HgCdTe, InSb, and even MBE HgCdTe on bulk CdZnTe substrates. Shown in Fig. 2 is a scale drawing of 6-in HgCdTe/Si, a 4-in substrate representing either InSb or 4-in HgCdTe/Si, and a 7 cm $\times$ 7 cm bulk CdZnTe substrate.

The primary benefit of 6-in HgCdTe/Si is its large size when compared to the other substrate materials. The larger size enables either the largest focal planes possible or greater numbers of smaller focal planes for reduced-cost production. The 6-in HgCdTe/Si substrates can also take advantage of automated silicon processing equipment for increasing efficiencies in device fabrication. The 6-in substrate possesses other unique advantages over bulk CdZnTe in terms of cost

Fig. 1. Photograph of a 6-in diameter HgCdTe/Si wafer.

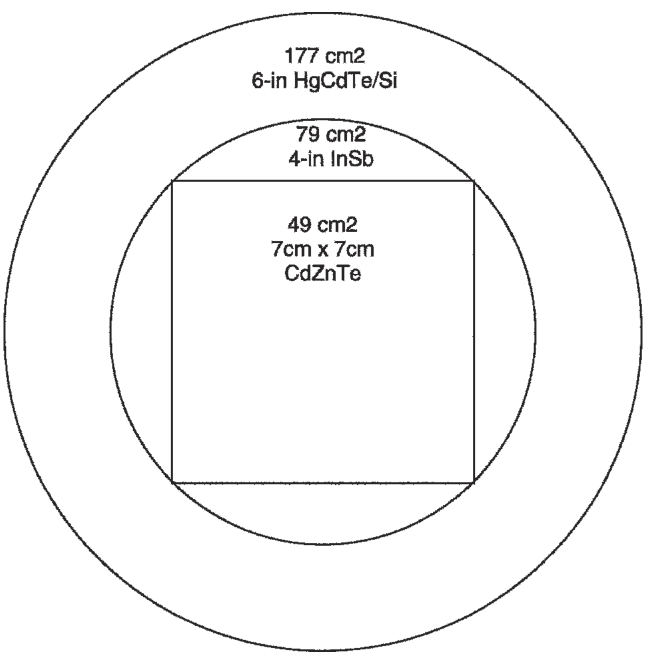

Fig. 2. Comparison of different substrate sizes.

and suppliers. The 7 cm × 7 cm bulk CdZnTe substrate is the largest commercially available, and it is unlikely to increase much larger than its present size. With the cost of 6-in Si substrate being ~$0.1 K vs. ~$10.0 K for the 7 cm × 7 cm, significant cost advantages of HgCdTe/Si are evident. Silicon is also a much more durable material than bulk CdZnTe, lending 6-in HgCdTe more likely to have greater yields in device fabrication by eliminating the breakage factor associated with CdZnTe.

EXPERIMENTAL PROCEDURES

HgCdTe/CdTe/ZnTe/Si Structure

At RVS, MBE HgCdTe has been grown on (211) silicon substrates as large as 6-in diameter in a 10-in VG Semicon V-100 system. Solid sources of CdTe, Te, and ZnTe are used in addition to a liquid Hg source. An HF-based process is used to prepare the silicon wafers for MBE growth. The growth of CdTe (~8 μm) is initiated with a 1-μm-thick ZnTe layer that has been shown to be essential in preserving the substrate orientation for the CdTe layer.[7] The HgCdTe device structure typically consists of an n-type 10-μm-thick layer doped with indium followed by p-type 2-μm layer doped in situ with arsenic. The entire structure is illustrated in Fig. 3. The growth of the HgCdTe is feedback-controlled in real-time using in situ spectroscopic ellipsometry (SE) to maintain the desired composition. The configuration of this structure is similar enough to our baseline LPE HgCdTe such that the processing of detectors on HgCdTe/Si wafers is able to take advantage of the standard detector fabrication processes developed for our second generation LPE HgCdTe detector production line. Figure 4 depicts the diode structure on HgCdTe/Si. A series of 4-in and 6-in wafers were grown, and their compositional uniformity, projected cutoff uniformity, and defect characteristics were examined.

RESULTS

Compositional Uniformity

A measure of the quality of an MBE grown HgCdTe/Si wafer is the radial compositional uniformity of the HgCdTe. The x value is measured by Fourier transform infrared (FTIR) on 5-mm centers with the center designated as the zero position.

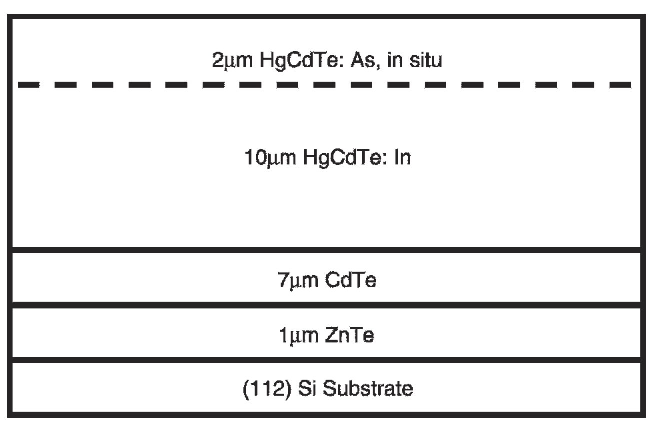

Fig. 3. Cross section of MBE-grown HgCdTe/CdTe/Si structure.

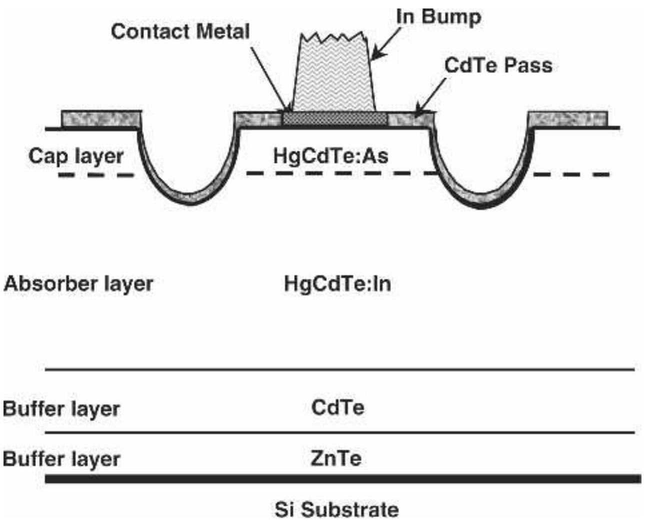

Fig. 4. Cross section of MBE HgCdTe/Si device structure.

The x-value data were normalized by dividing the x value at every location on the wafer by the x value at the center of the wafer. The result of this is that the center point assumes a value of 1.0, and all other data points deviate from that based on their nonuniformity. Figure 5 is a plot of the radial normalized x value for both 4-in and 6-in MWIR HgCdTe wafers. In general, compositional uniformity is determined by comparing the center point with the outermost point. In the case of a 4-in wafer, it is 45 mm from the center, and for a 6-in wafer it is 70 mm from the center. The 4-in wafer demonstrates nearly perfect uniformity with a center-to-edge deviation of only 0.01%. The 6-in wafer shows a greater center-to-edge deviation of 0.07%. The excellent uniformity is attributed to proper matching of the CdTe and Te effusion sources and thermal uniformity of the wafer during growth. The plot in Fig. 6 is the normalized center-to-edge x-value uniformity for a series of MWIR HgCdTe/Si growths. The majority of wafers have uniformities in the range of 0.0% to −0.5%. For the minority of wafers that deviate from that range, the mechanisms are not understood. Potential causes may include potential variability substrate mounting to the platen, potential differences between the platens themselves, or occasional variability in source characteristics.

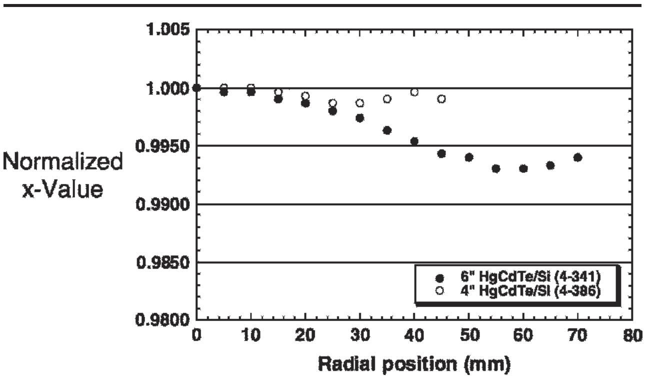

Fig. 5. Normalized radial x value for a 4- and 6-in HgCdTe/Si wafer.

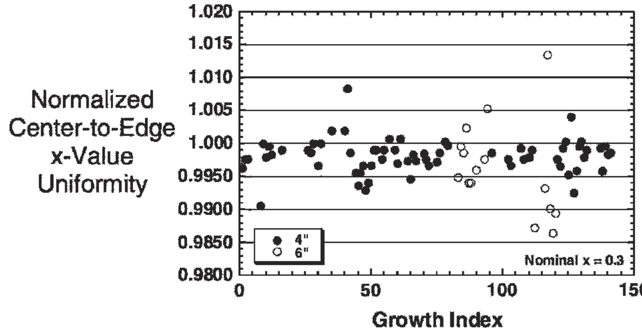

Fig. 6. Normalized center-to-edge x-value uniformity for a series of 4- and 6-in HgCdTe/Si wafers.

Projected 78-K Cutoff Uniformity

The direct result of excellent compositional uniformity is correspondingly excellent projected cutoff uniformity at 78 K. Figure 7 shows the expected cutoff (in μm) at 78 K for the same wafers from Fig. 6. The expected center-to-edge deviation in cutoff for the 4-in wafer is 0.01 μm. The 6-in wafer shows a greater deviation at 0.07 μm.

The plot in Fig. 8 is the center-to-edge delta in projected cutoff for the same series of wafers from Fig. 7. The majority of wafers lie in a range from 0.00 μm to 0.05 μm. The repeatability of the excellent cutoff uniformity is essential for manufacturing uniform FPAs from the same wafer or maintaining the uniformity of a large format FPA.

Growth Defects

Figure 9 shows the total void plus microvoid defect density for the same series of HgCdTe wafers. Growth defects are generally radially distributed on HgCdTe/Si grown at RVS. Both voids and microvoids are counted on 5-mm centers starting in the center of the wafer and progressing to the edge (45 mm for 4-in wafer, 70 mm for 6-in wafer), and the whole-wafer average for total defect density is determined. As seen in the plot, we have obtained sub-100-cm^{-2} defect densities on several occasions. In general, we expect to be below 500 cm^{-2}. Values above 500 cm^{-2} indicate that the growth process is deviating from the optimum HgCdTe, CdTe, or

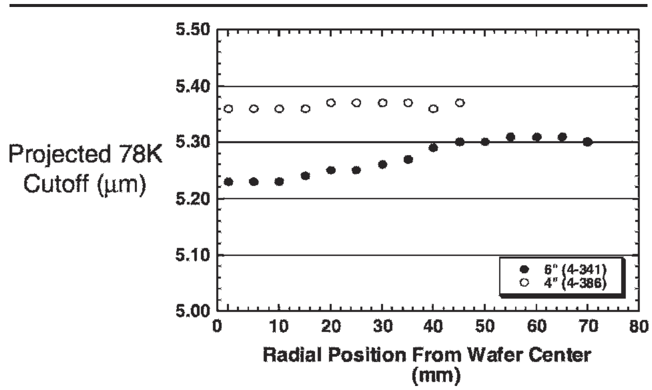

Fig. 7. Radial projected 78-K cutoff for a 4- and a 6-in HgCdTe/Si wafer.

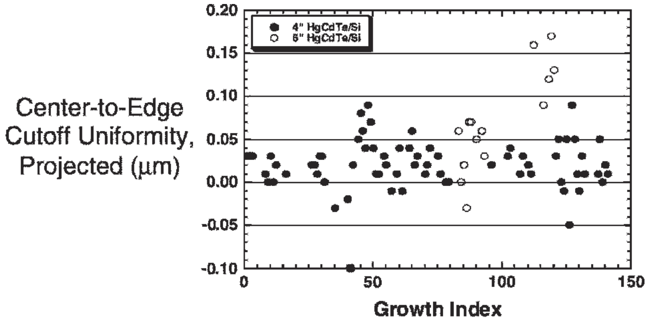

Fig. 8. Projected center-to-edge cutoff uniformity for a series of 4- and 6-in HgCdTe/Si wafers.

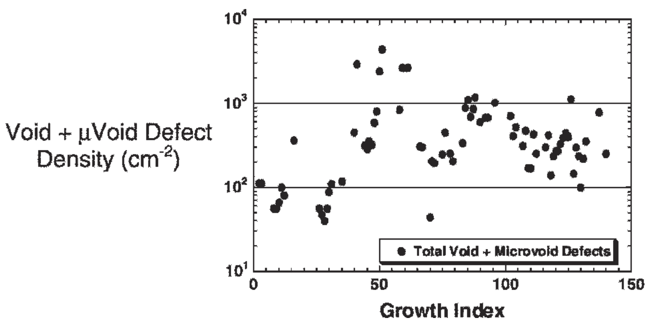

Fig. 9. Total void + microvoid defect densities for a series of 4- and 6-in HgCdTe/Si wafers.

ZnTe growth conditions. Because HgCdTe is grown on CdTe/ZnTe/Si without removing the wafer from the chamber beforehand, it is possible for growth defects to have their nucleation in either the CdTe or ZnTe layers. The low defect density HgCdTe/Si attained in the VG V100 enables FPAs with very high operabilities. The goal is to be able to achieve sub-100-cm^{-2} material routinely such that MBE growth defects are a negligible factor concerning FPA operability.

Doping

Indium is used for n-type doping, and arsenic is used for p-type doping for MBE-grown HgCdTe/Si devices. Figure 10 shows the radial doping concentration as measured by secondary ion mass spectrometry (SIMS) for both indium and arsenic for a single 6-in HgCdTe/Si wafer. The data were acquired by taking five samples from different radial positions from the same 6-in and submitting them for SIMS analysis. No significant nonuniformity is observed in the radial distribution of the indium concentration across a 6-in HgCdTe/Si wafer. An increase in the As concentration can be observed in the sample at the edge of the wafer. From an MBE growth perspective, three factors influence the incorporation of As in MBE grown HgCdTe. As understood at RVS, the primary factor is substrate temperature, with incorporation being enhanced at lower temperature and hindered at higher temperature. A relatively small change in substrate temperature of 5°C can greatly impact incorporation of As. A secondary factor that can influence As incorporation is the x value of the HgCdTe, with lower higher x value enhancing incorporation. In review of the x-value profile of this particular wafer, the x value decreases slightly at the edge of the wafer, which would have slightly inhibited the As incorporation at the wafer edge. The third factor would be the uniformity in the radial distribution of the As beam itself, and sudden changes in flux uniformity in 15 mm radially are not considered likely due to the large size of the MBE system. In considering these three factors the increase in As concentration at the edge of the wafer is interpreted as being likely due to a slight temperature decrease at the edge of the wafer.

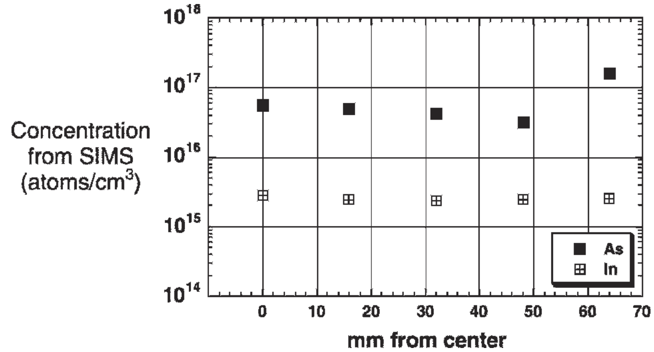

Fig. 10. Radial In, As doping concentration as measured by SIMS for a 6-in HgCdTe/Si wafer.

SUMMARY

The growth of high-quality large-area HgCdTe/Si up to 6-in diameter with exceptional cutoff uniformity of less than 0.1 μm and extremely low defect densities below 100 cm^{-2} has been both demonstrated and numerously repeated in the VG V100 MBE growth system. Large-area, low-defect, high-uniformity HgCdTe/Si is essential for meeting the needs of large-format applications that cannot be met on smaller wafer approaches, such as HgCdTe on bulk CdZnTe or 4-in InSb substrates.

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