Self-Assembly of Metal Nanocrystals on Ultrathin Oxide for Nonvolatile Memory Applications

CHUNGHO LEE,[1] JAMI METEER,[1] VENKAT NARAYANAN,[1] and EDWIN C. KAN.[1,2]

1.—Cornell University, School of Electrical and Computer Engineering, Ithaca, NY 14853. 2.—E-mail: kan@ece.cornell.edu

The self-assembly of metal nanocrystals including Au, Ag, and Pt on ultrathin oxide for nonvolatile memory applications are investigated. The self-assembly of nanocrystals consists of metal evaporation and selective rapid-thermal annealing (RTA). By controlling process parameters, such as the thickness of the deposited film, the post-deposition annealing temperatures, and the substrate doping concentration, metal nanocrystals with density of $2–4 \times 10^{11}$ cm^{-2}, diameter less than 8.1 nm, and diameter deviation less than 1.7 nm can be obtained. Observation by scanning-transmission electron microscopy (STEM) and convergent-beam electron diffraction (CBED) shows that nanocrystals embedded in the oxide are nearly spherical and crystalline. Metal contamination of the Si/SiO_2 interface is negligible, as monitored by STEM, energy dispersive x-ray spectroscopy (EDX), and capacitance-voltage (C-V) measurements. The electrical characteristics of metal, nanocrystal nonvolatile memories also show advantages over semiconductor counterparts. Large memory windows shown by metal nanocrystal devices in C-V measurements demonstrate that the work functions of metal nanocrystals are related to the charge-storage capacity and retention time because of the deeper potential well in comparison with Si nanocrystals.

Key words: Nonvolatile memories, nanocrystals, direct tunneling, work function, self-assembly

INTRODUCTION

In conventional, electrically erasable programmable read-only memory (EEPROM), scaling of tunneling-oxide thickness to the direct-tunneling regime ($\leq$3 nm) enables fast and low voltage operations but is limited by charge loss in the continuous floating gate. The discrete floating gate in Fig. 1 is one promising way to achieve high-speed operation and high scalability with ultrathin tunneling oxide.[1–3] For semiconductor nanocrystal memories, the role of traps and defects inside or at the surface of nanocrystals can explain the experimental observation of long-term retention,[4] which makes their operational principle similar to trap-based storage.[5] The control of trap levels and density is thus critical for consistency in long retention time. This is, however, difficult because of the high sensitivity of trap formation and annihilation during the annealing process. Although Si or Ge nanocrystal metal-oxide semiconductor (MOS) memories exhibit rather long retention time because of deep trapping at the surface, the charge storage capacity is rather small with a direct-tunneling oxide barrier mainly because the energy band structures of the substrate and the nanocrystals are the same. On the other hand, work function engineering in metal nanocrystals[6] makes it possible to increase the storage capacity and the retention time. The larger work function in selected metal nanocrystals creates a deeper potential well to enhance retention without sacrificing injection efficiency. In addition, because traps at the nanocrystals/oxide interface are mostly screened out by the high density of carriers in the metal, metal nanocrystal memories are more controllable during the fabrication process and exhibit more stable device characteristics.[7]

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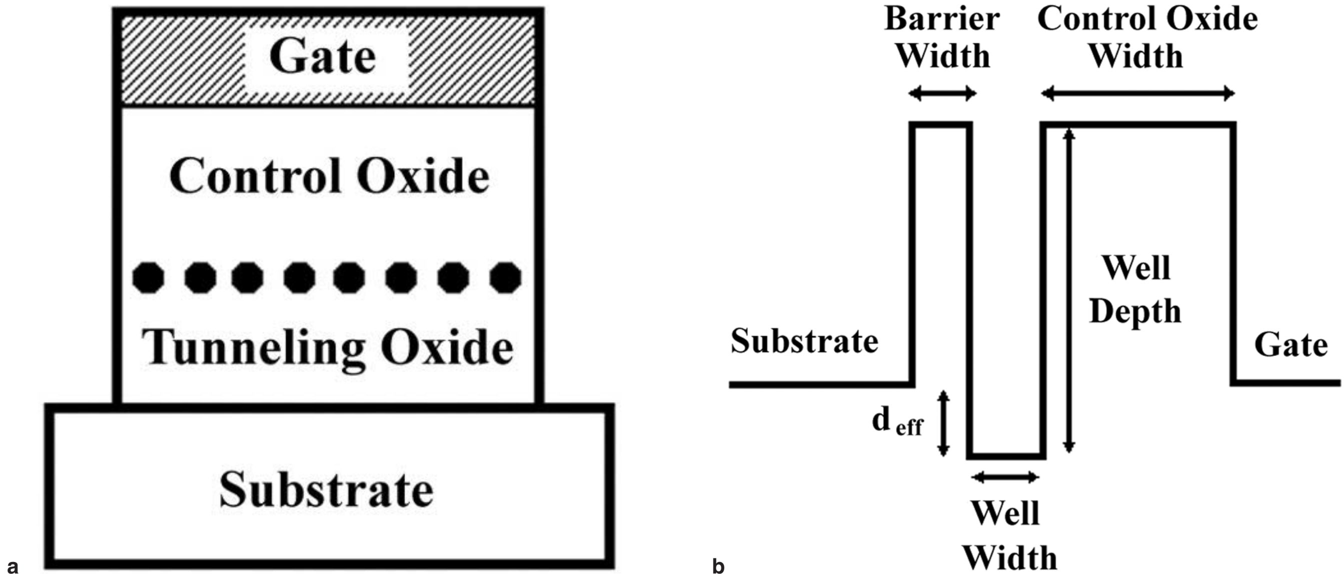


Fig. 1. (a) A nanocrystal memory schematic and (b) a representative band diagram. The d_{eff} is effective well depth (barrier height).

Metal nanocrystals can be formed by various methods including colloidal suspension, aerosol deposition, ion implantation, and direct-deposit self-assembly. The colloidal method results in good size distribution, but associated chemicals can cause contamination.[8] The aerosol method uses gas-phase condensation, which has complications with size selection and particle delivery.[9] The ion implantation method has spatial controllability problems.[10] On the other hand, the direct-deposit self-assembly[11] is a simple and complementary MOS friendly method that involves the spontaneous formation of nanocrystals to achieve a local minimum energy. In this paper, we investigate process characteristics of direct-deposit self-assembly, metal nanocrystal formation, and the physical characterization of metal nanocrystal memories. In addition, we demonstrate the advantages of metal nanocrystals over semiconductor nanocrystals by work function engineering from the electrical characterization of nanocrystal memories.

FABRICATION OF THE TUNNELING OXIDE

There are three charging mechanisms in conventional EEPROM: hot carrier injection, Fowler-Nordheim (F-N) tunneling, and direct tunneling.[12] Hot carrier injection depends more strongly on the barrier height fixed at the Si/SiO_2 interface rather than the barrier thickness. The F-N tunneling results from the applied vertical field reducing the effective barrier thickness and is a strong function of the oxide field. The F-N tunneling is important for thicker barriers and can be readily adapted for programming and retention trade-off. When the barrier width is reduced to less than around 3 nm, the direct-tunneling mechanism becomes more dominant because tunneling probability rises exponentially with the barrier thickness reduction.

The direct-tunneling-regime oxide barrier between nanocrystals and the substrate is fabricated on a <100> p-type substrate of 14–22 Ω·cm resistivity. Trichloroethane dry oxidation for the tunneling-oxide growth is performed at 750°C with 6 L/min total flow rate of 10% oxygen and 90% nitrogen. Low-temperature oxidation provides sufficient control of the oxide thickness with a growth rate of ~2.7 Å/min. The interface of Si/SiO_2 is usually required to be atomically flat for high mobility and low tunneling current.[13] However, low-temperature oxidation can be prone to produce rather rough interfaces and high defect densities. We performed scanning-transmission electron microscopy (STEM) using a VG HB501UX (VG microscopes Ltd., UK) with a cold-field emission source to examine the interface

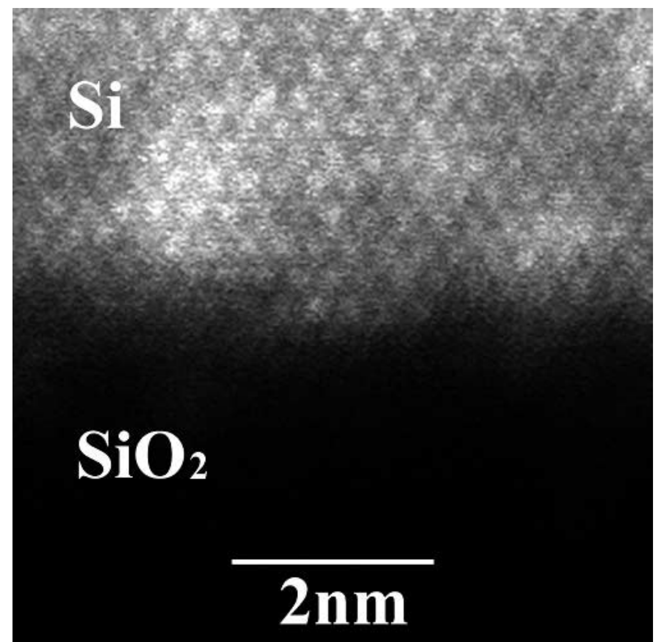


Fig. 2. The STEM dark-field cross-sectional image of the Si/SiO_2 interface before postannealing.

Table I. Tunneling-Oxide Thickness Measured Using Various Methods

Measurements	Methods	Average T_{ox} (nm)
Physical measurements	STEM	2.72
	Ellipsometry (n = 1.46)	2.66
Electrical measurements	C-V extraction	3.39
	I-V extraction	3.20

roughness. Figure 2 shows a cross-sectional STEM image where the roughness of two or three atomic layers is observed. For actual device fabrication, subsequent annealing at 900°C in N_2 ambient for 5 min is performed to produce better smoothness and quality. The oxide quality issues, such as charge trapping on defects and Si/SiO_2 interfacial traps, are always major concerns in non-volatile memory operations.[14] The effective thickness is extracted from both capacitance-voltage (C-V) and current-voltage (I-V) measurements,[15] while the physical thickness is measured by ellipsometry and STEM as listed in Table I. The effective oxide thickness is usually larger than physical thickness because of the quantum repulsion and possible gate depletion.[16]

METAL NANOCRYSTAL FORMATION

Metals are deposited on ultrathin oxide by electron-beam evaporation. Unlike the aerosol method,[9] very little gas-phase condensation occurs during transport of evaporated metal atoms because of the high vacuum of 2×10^{-6} torr and very low partial pressure in the chamber. Film thickness and deposition rate are determined by a quartz crystal monitor around 1–2 nm and 1 Å/sec, respectively. Rapid thermal annealing (RTA) by AG Heatpulse 610 (AG Associates, USA) is selectively performed for further nanocrystal formation control. We will show only exemplary process characteristics because of length constraints. For nanocrystal formation analysis, we use a Zeiss 982 scanning electron microscope (Carl Zeiss, Germany). Its specified resolutions are 1.2 nm at 20 KV and 4 nm at 1 KV, even though the practical resolution is lower. Figure 3 shows the plane view of scanning electron microscopy (SEM) images of Pt nanocrystals with various annealing temperatures. After 1.2-nm Pt deposition on the oxide, the Pt film went through RTA at 800°C, 850°C, 900°C, or 950°C for 10 sec. The as-deposited Pt film forms very small size nanocrystals not distinguishable by SEM (but can be verified with STEM), while distinct nanocrystals can be observed after 800°C annealing under SEM observation. Increasing the temperature further produces larger and sparser nanocrystals. Nanocrystal formation is the process in which the nonequilibrium state clusters reshape, attempting to obtain a local minimum energy state. It is conjectured that the as-deposited Pt film at room temperature does not have enough energy to overcome the energy barrier of reshaping. Thus, the thermal energy from annealing helps the Pt film form more stable clusters by increasing surface diffusion. Stress relaxation, the dispersion force, and the electrical double layer can also influence the nanocrystal formation process.[12] As the temperature increases, the clusters grow larger at the nucleation sites. The size analysis is performed by higher magnification SEM images (not shown) and an image processing tool. The histogram and the graph of nanocrystal size in Fig. 4 shows a dispersive distribution toward larger sizes as the clusters grow, although annealing below 850°C produces rather uniform size. There are two mechanisms of nanocrystal growth:[17,18] Ostwald ripening, in which the larger nanocrystals grow at the expense of smaller nanocrystals, and coalescence, in which two small nanocrystals combine into a large nanocrystal. The high annealing temperature increases the mean size of clusters and dispersion of the size distribution but decreases the density of clusters because of mass conservation. However, the as-deposited films of Au and Ag appear to be non-wetting. Metals have higher surface energy than oxide. Hence, the as-deposited metals tend to ball up on the oxide because metals need larger energy to make a surface than oxide.[19] The solid phases of Ag, Au, and Pt have surface energy densities of 1,140 ergs/cm^2, 1,410 ergs/cm^2, and 2,340 ergs/cm^2, respectively.[20] The higher surface energy of Pt suggests that the as-deposited Pt film consists of the smallest size clusters with further cluster growth limited at room temperature. This is also consistent with the result that the mean size of Au nanocrystals is smaller than Ag ones. Heat treatment near the eutectic temperature does not show much difference from as-deposited Ag and Au. Nanocrystals already reach close to the critical size without annealing and go through sintering during the thermal process in 550–600°C. In addition to the annealing temperature, the annealing time at the given temperature can also affect the nanocrystal formation by surface migration, but the dependence is rather weak because of the slow migration process.[21]

The initial film thickness is another important parameter for size control in nanocrystal formation. As an illustration, Ag nanocrystal formation with various initial thicknesses is shown in Fig. 5. The in-situ crystal monitor measures initial thicknesses of 1.2 nm, 2.2 nm, and 3.2 nm. As the initial thickness increases, the nanocrystal size clearly increases, and the density decreases. While post-deposition annealing increases surface mobility and, therefore, allows the formation of more distinct nanocrystals, the increased initial thickness actually makes the clusters grow larger during film deposition. In the thicker film, the shape of the nanocrystals is not spherical. This indicates that the growth is surface-mobility-limited around 25°C. Surface migration of nuclei is also limited at this temperature. The circular shape of nanocrystals in thinner films, however, indicates nucleation

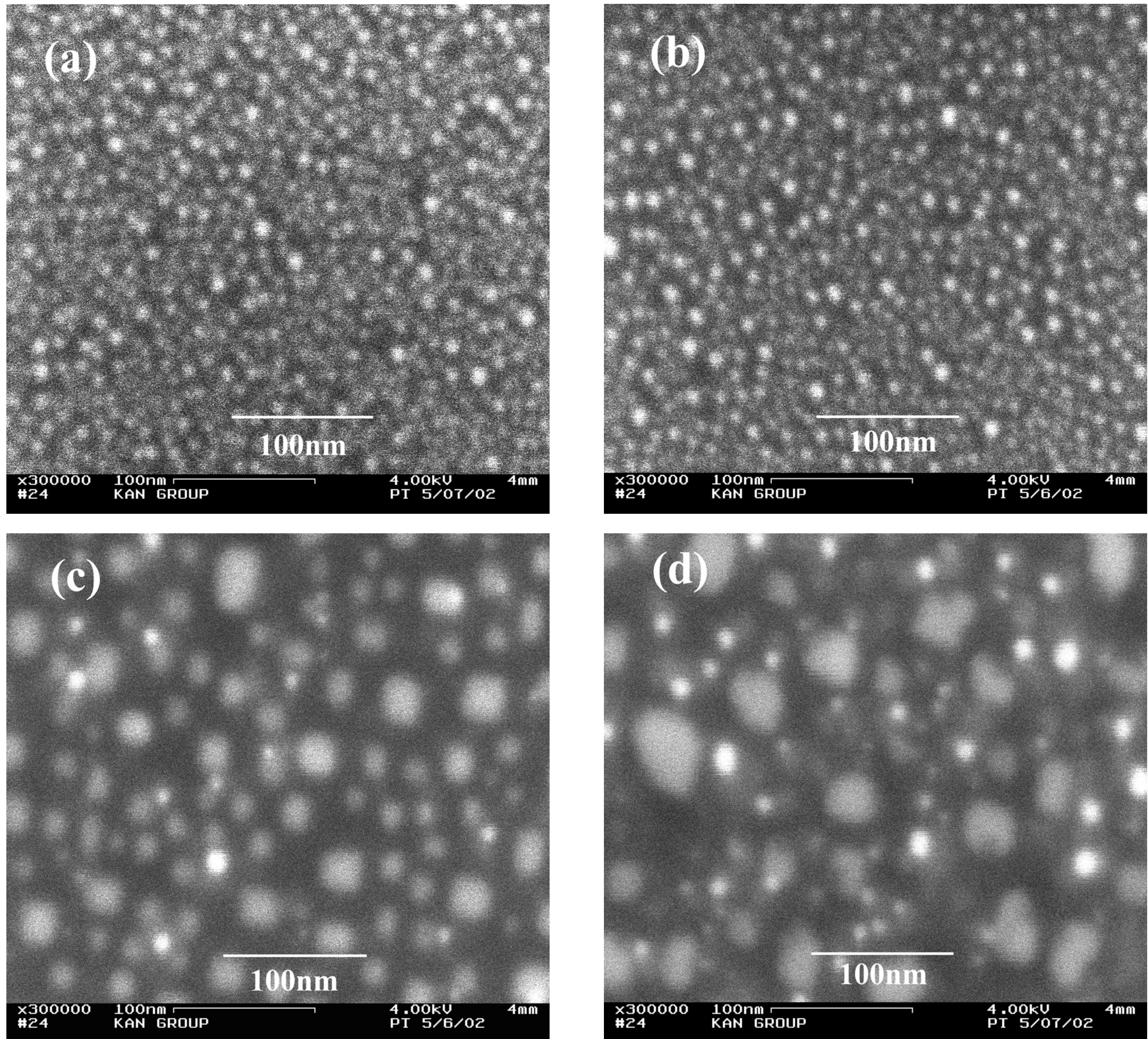
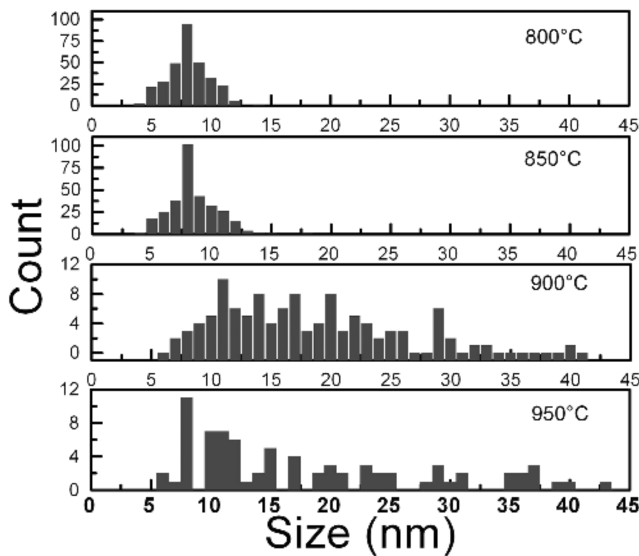


Fig. 3. The annealing temperature effect. The SEM plane-view images of Pt nanocrystals. Nanocrystals are annealed at (a) 800°C, (b) 850°C, (c) 900°C, and (d) 950°C for 10 sec. Nanocrystals are formed on 3-nm thermal oxide with 10^{17} cm^{-3} p-type substrates.

growth before significant ripening and coalescence processes. Therefore, the size change of nanocrystals in the thinner film is more definite than the density change. The initial film-thickness effect of Au nanocrystal formation also showed the same characteristics.[22]

In equilibrium, the work function difference between metals and semiconductors can cause band bending in semiconductors and charge transfer through the thin oxide. The charging of nanocrystals by work function difference affects nanocrystal formation through Coulombic repulsion. Band bending is determined by oxide thickness and substrate doping. Test samples of Au nanocrystals were formed on ~3-nm oxide grown on substrates with three different doping levels. The substrates were prepared by phosphorus ion implantation into p-type wafers with a background boron concentration of 10^{15} cm^{-3}. The 1.2-nm Au was evaporated with a 0.2 Å/sec deposition rate. If the work function of Au is assumed to be close to the Fermi level of the 10^{15} cm^{-3} p-type substrate, the work function difference is around 0.69 eV for 10^{17} cm^{-3} surface n-type doping and around 0.8 eV for 10^{19} cm^{-3}. A larger substrate charging effect causes stronger repulsion between charged nanocrystals. Figure 6 shows more distinct and denser nanocrystals as the work function difference becomes larger. Table II shows an optimal recipe for Au, Ag, and Pt nanocrystal formation according to the process parameters of annealing temperature, initial film thickness, and substrate doping concentration.



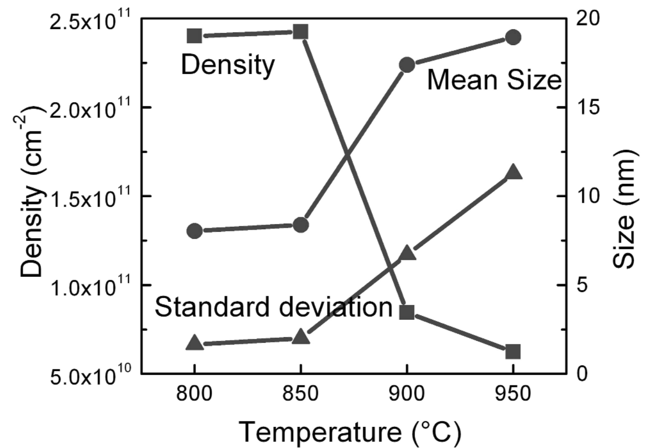


Fig. 4. Size distribution of Pt nanocrystals. Nanocrystals are annealed at 800°C, 850°C, 900°C, and 950°C for 10 sec.

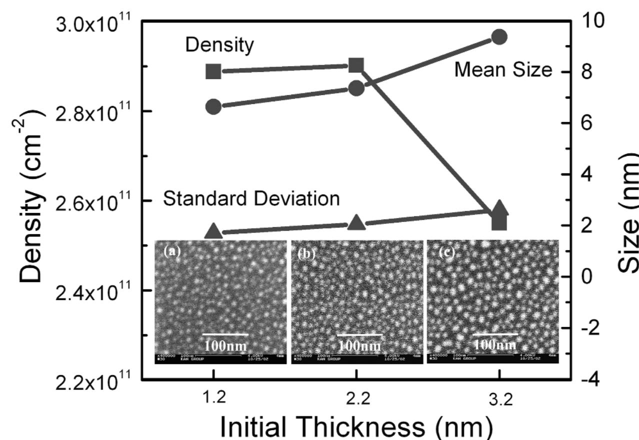


Fig. 5. The initial film-thickness effect. Mean size, size distribution, and number density of Ag nanocrystals. Insets are plane-view SEM images. Nanocrystals are formed with 1.2-nm, 2.2-nm, and 3.2-nm initial film thickness.

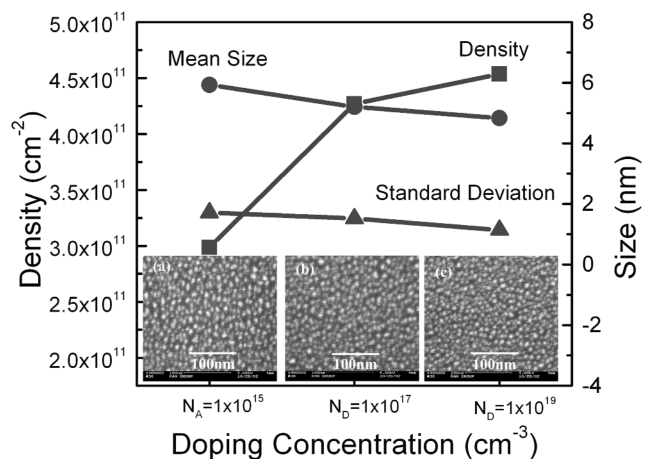


Fig. 6. The substrate doping effect. Mean size, size distribution, and number density of Au nanocrystals. Insets are plane-view SEM images. Nanocrystals are formed on the substrate of $N_A = 1 \times 10^{15}$ cm^{-3}, $N_D = 10^{17}$ cm^{-3}, and $N_D = 10^{19}$ cm^{-3}.

PHYSICAL CHARACTERIZATION OF NANOCRYSTALS

As a first example, Au nanocrystals are self-assembled on the tunneling oxide by 1.2-nm initial layer deposition followed by 575°C annealing for 10 sec. On top of the nanocrystals, the subsequent 36-nm control oxide is deposited by plasma-enhanced chemical vapor deposition (PECVD). Figure 7 shows the cross-sectional STEM pictures of Au nanocrystals embedded in SiO_2. The spherical shape of Au nanocrystals is observed. In general, spherical nanocrystals are preferred for nonvolatile memory cells because the three-dimensional symmetry results in the best charge confinement and physical stability from surface energy minimization. By STEM observation, the average diameter of nanocrystals is 4.7 nm and the thickness of the tunneling oxide is 2.7 nm. The convergent-beam electron diffraction (CBED) pattern of Au nanocrystals in Fig. 7 confirms the crystalline lattice, although it is unclear if the nanocrystal is single crystalline. The CBED images of the Si substrate and amorphous

Table II. Recipes for Nanocrystal Formation

Species	Annealing Temperature (°C)	Initial Thickness (nm)	Mean Size (nm)	Size Distribution (nm)	Density ($\times 10^{11}$ cm^{-2})
Au	Room temperature	1.2	6.26	1.45	4.08
Ag	Room temperature	1.2	6.63	1.70	2.88
Pt	800	1.2	8.04	1.65	2.40

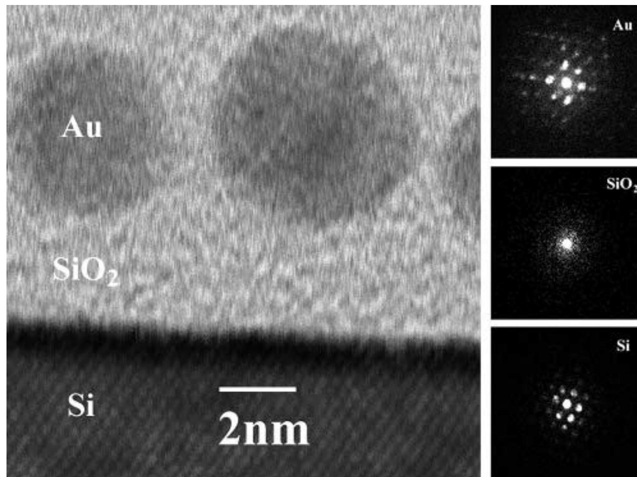
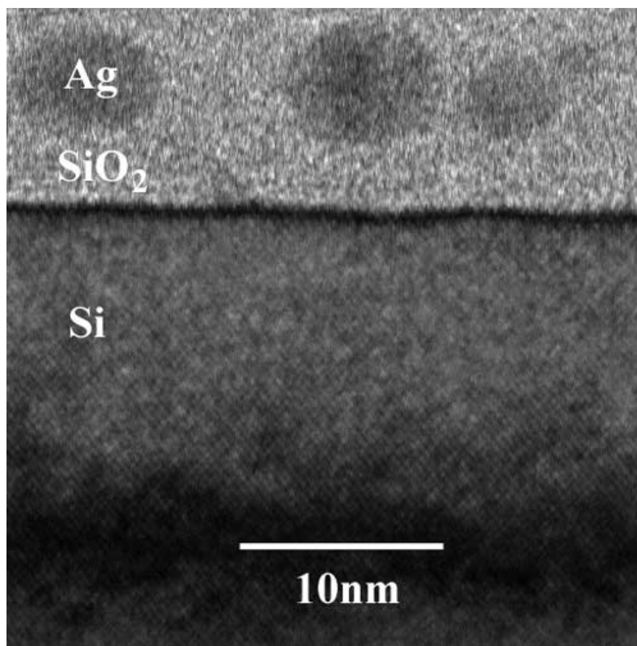


Fig. 7. A STEM bright-field cross-sectional image of Au nanocrystals embedded in SiO_2 and CBED patterns of a single Au nanocrystal, the gate oxide, and the Si substrate. The Au nanocrystals are formed by 1.2-nm evaporation followed by RTA at 575°C for 10 sec.

oxide in the same sample are also shown for comparison. The STEM and CBED images of Ag and Pt nanocrystals yield similar results. Various magnification cross-sectional STEM images are shown in Fig. 8.

For elemental identification, energy dispersive x-ray spectroscopy (EDX) is performed on a single nanocrystal in Fig. 9. Detection of metals (Au, Ag, and Pt), Si, O, and other polishing materials identifies the nanocrystal as metal nanocrystals embedded in the oxide. The EDX analysis at the Si/SiO_2 interface gives no evidence of metal contamination by metal diffusing to the substrate. In summary, we have shown that high-quality nanocrystals, in the sense of shape and crystallinity, can be produced by the self-assembly process. Nanocrystal formation stabilizes the atomic cluster in a spherical shape at a minimum energy state, instead of allowing diffusion through the thin oxide. The electron-beam size for STEM imaging and CBED is around 3 Å at 100 KeV. For EDX, it is around 10 Å. The sample thickness is estimated to be less than 50 nm.

The charge storage capacity and retention of nanocrystals on a direct-tunneling oxide are characterized by the nanocrystal potential-well depth and width, which depend on the work function and size of the nanocrystals, respectively. The shallow potential well, for example, Si nanocrystals paired with a Si substrate, can only hold charges for a relatively short time because of direct-tunneling back to the substrate.[6] However, metal nanocrystals of large work functions can make use of the deep potential wells to hold electrons for longer time. Figure 10 shows the energy band diagrams of nanocrystal MOS memories with a 10^{17} cm^{-3} boron-doped substrate and a chromium control gate. For illustration, average work functions[23,24] are assumed as 4.46 eV for Ag, 4.94 eV for Au, 4.95 eV for Pt/Si, and 4.5 eV for Cr, even though work functions vary according to crystallographic planes and measurement methods.[25] Silver has a work function of $\sim$4.46 eV where the Fermi level is around the midgap of the substrate. Gold has a work function of $\sim$4.94 eV where the Fermi level is near the valence band edge. However, the electrical characteristics of Pt nanocrystal memory devices demonstrate a lower work function ($\sim$4.95 eV) than its bulk values (5.3–5.7 eV), which is likely due to silicide formation in the nanocrystals. Work function reduction of Pt



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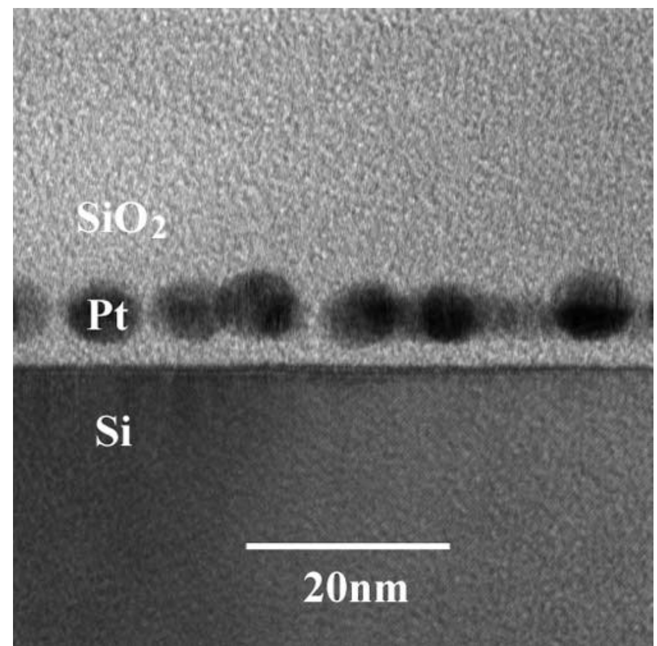

b

Fig. 8. The STEM bright-field cross-sectional images of (a) Ag and (b) Pt nanocrystals embedded in SiO_2. The Ag and Pt nanocrystals are formed by 1.2-nm evaporation without post-annealing and with RTA at 800°C for 10 sec, respectively.

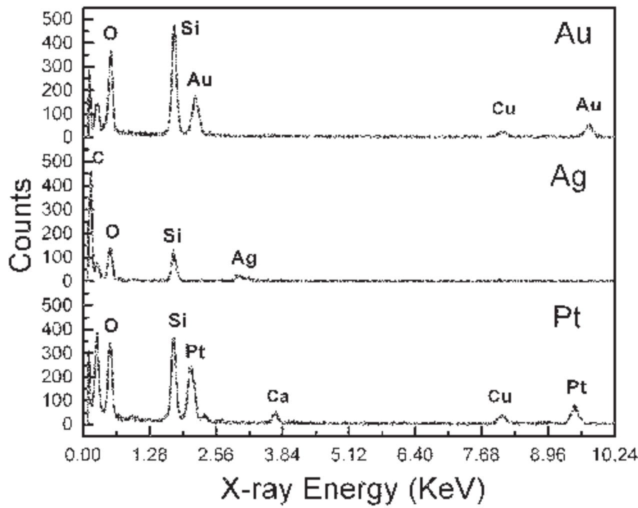

Fig. 9. The EDX spectra of single Au, Ag, and Pt nanocrystals embedded in SiO_2.

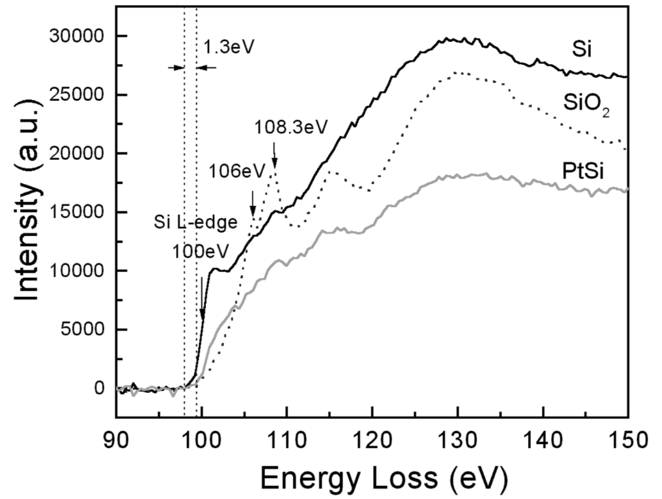

Fig. 11. The EELS spectra of Si L_{23} edges. Locations of the focused e-beam are at the Si substrate, the gate oxide, and a single Pt nanocrystal. The background was subtracted by a power-law function.

has been previously reported and attributed to impurities at the metal/oxide interface[26] and interface states at a metal/high-k dielectric interface.[27] For further confirmation of Pt silicide formation, EDX and electron energy loss spectroscopy (EELS) analyses were performed. First, EDX confirms the existence of two major elements, Pt and Si, from Pt nanocrystals. Then, the EELS spectra of the Si L_{23} edge at three different locations including the Si substrate, the tunneling oxide, and Pt nanocrystal are acquired, as shown in Fig. 11. The electron beam size is around 3 Å. The Si L edge or midpoint of the edge onset at the Si substrate region is clearly shown around 100 eV.[28] In the tunneling-oxide region, edge maxima at 106 eV and 108.3 eV shows amorphous SiO_2 features of an energy loss near-edge structure.[28] In the Pt nanocrystal region, Si L edge shifts by 1.3 eV from the Si L edge at the Si substrate. This indicates the chemical reaction between Pt and Si because a small shift is usually related to an interaction energy change of the chemical bonds.[29] It also suggests that the reaction between Pt and Si to form Pt silicide is preferred because oxidation is not plausible with Pt. Rather strong adhesion of Pt to SiO_2 at the high-temperature nanocrystal formation[30] can be also explained by Pt silicidation.

A lower annealing temperature is preferred to prevent metal nanocrystals from diffusing vertically, which would contaminate the Si/SiO_2 interface. In particular, the ultrathin oxide between nanocrystals and the substrate is more vulnerable to contamination. Even without thermal annealing, discrete and spherical metal nanocrystals can be assembled; although subsequent low-temperature processes, such as 275°C PECVD, control oxide deposition on top of nanocrystals, they can affect the nanocrystal formation. In contrast to low-temperature RTA in Fig. 8, Fig. 12 shows Pt contamination by high-temperature

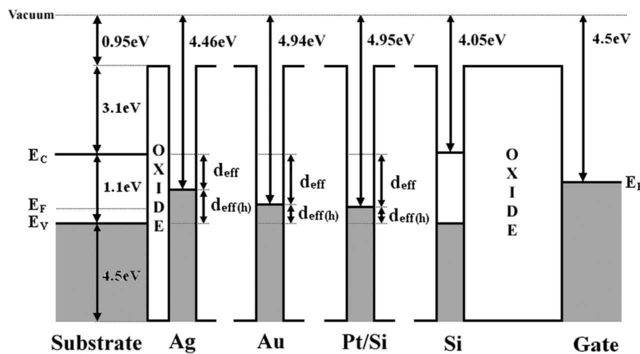

Fig. 10. Energy band diagrams for Ag-, Au-, Pt/Si-, and Si-nanocrystal MOS memories with Cr gate at the flat band state. The d_{eff} and $d_{eff(h)}$ are effective potential-well depths for electrons and holes, respectively. The dimension is not drawn to scale to magnify the critical comparison.

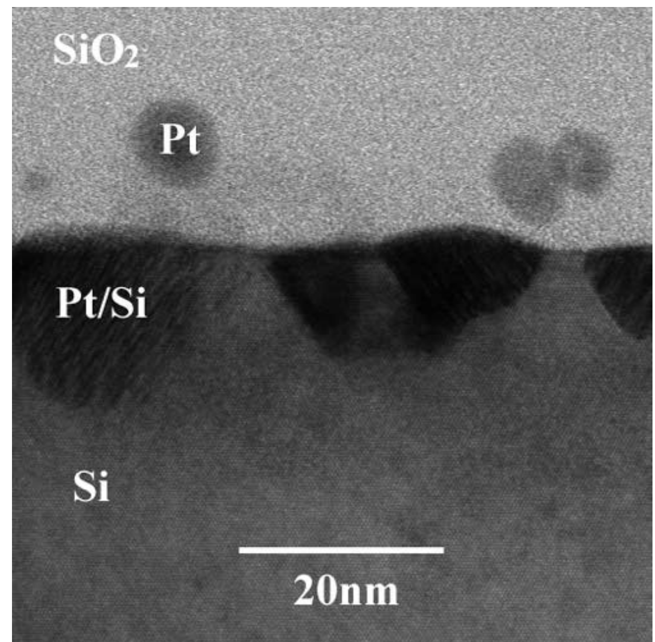

Fig. 12. A STEM bright-field cross-sectional image of Pt metal contamination by high-temperature annealing above 900°C.

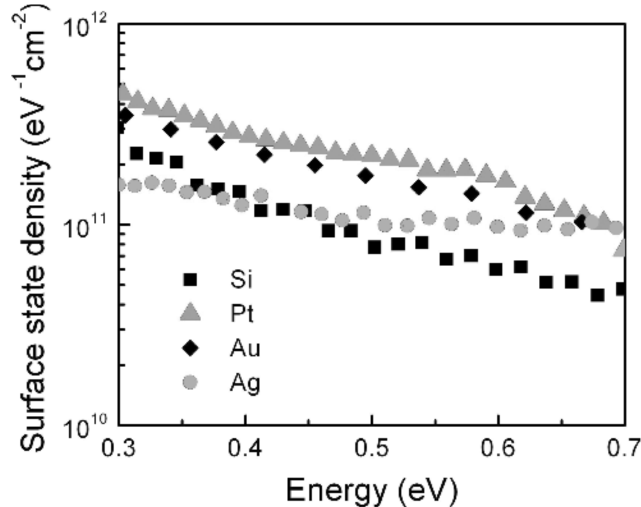

Fig. 13. Interface trap density of Au-, Ag-, Pt-, and Si-nanocrystal MOS capacitors. The doping concentration of the p-type substrate is around 10^{17}cm^{-3}.

annealing above 900°C, where most of the Pt diffuses to the substrate interface, though the rest of Pt forms the spherical nanocrystals. The EDX analyses also confirm the metal contamination by detecting the Pt element at the interface. The Pt was not detected in the low-temperature annealed sample in Fig. 8. However, not all of the EDX measurements are shown here because of length constraints. In addition to physical monitoring by STEM and EDX, electrical monitoring is performed by extraction of interface trap densities. Extraction is based on the comparison of high-frequency C-V measurements and theoretical calculations, performed using the Terman and Kuhn method.[31,32] Comparing with nonmetal nanocrystals of Si, as shown in Fig. 13, all metal nanocrystal memories show sufficiently low, interface trap density and negligible metal contamination. The C-V measurement setup will be described in detail in the next section.

ELECTRICAL CHARACTERIZATION OF NANOCRYSTAL MEMORIES

The MOS capacitors with Au, Ag, Pt, and Si nanocrystal floating gates are fabricated on p-type substrates. Metal nanocrystals are self-assembled with a density of 2.4–4.1 $\times$ 10^{11} cm^{-2} on ~3-nm tunneling oxide, electrically measured by control samples of MOS capacitors. The device design is targeted to use direct tunneling as the main programming mechanism. To ensure that tunneling occurs through only one oxide barrier, a relatively thick control oxide of 32 nm is adopted to minimize any charge transport through this oxide layer. A final, top Cr gate is deposited by e-beam evaporation. An overview of nanocrystal memory structure was previously shown in Fig. 1.

Figure 14 shows 1-MHz C-V characteristics in nanocrystal MOS capacitors. The write and erase operations are carried out by applying voltage to the top control gate for 5 sec before each voltage sweep while the backside substrate contact is grounded. The positive voltages range from 2–5 V, while negative voltages are from -4 V to -7 V. This range of the write/erase voltage is a considerable reduction from the programming voltage of F-N tunneling devices.[6] A large flat band voltage (V_{FB}) shift is observed between forward and backward sweeps in the metal-nanocrystal MOS capacitors, but Si ones show very small memory windows. In Fig. 14a, an Au-nanocrystal MOS capacitor shows a 7-V memory window when sweeping between 5 V and -7 V, and a V_{FB} shift in either direction depending on the polarity of the writing voltage. For positive voltage writing, Au nanocrystals have a d_{eff} of 0.89 eV, which can hold around eight electrons (from Coulomb charging) in each effective potential well. Here, we have assumed nanocrystals of 6.2-nm diameter (d) give 1.35-aF self-capacitance ($C_{self} \sim 2\pi\varepsilon_{ox}d$) and 0.1 eV Coulomb charging energy gap (e^2/C_{self}). According to $\Delta V_{FB} \sim Q_{nc}/C_{control_oxide}$, where Q_{nc} is the total charge in nanocrystals per cm^2 and $C_{control_oxide}$ is the capacitance with control oxide as the insulator, one electron in each nanocrystal can shift the flat band voltage by $\Delta V_{FB} \sim 0.6$ V, and eight electrons can give $\Delta V_{FB} \sim 4.8$ V. Estimation of electron storage capacity for the effective potential wells of metal nanocrystals is listed in Table III. Figure 14b shows the limit of charge storage in the Ag nanocrystal MOS capacitor for positive voltage writing. Silver has a small memory window of 4.5 V with saturation in the positive gate-bias swing. The saturation of V_{FB} can be explained as high tunneling probability after filling the effective potential well. The deepest potential well of Pt nanocrystals in Fig. 14c shows the largest memory window of 9.2 V, and no saturation of charge storage is observed. In comparison to metal nanocrystal capacitors, H_2-annealed, Si-nanocrystal MOS capacitors with zero effective-potential depth result in very small memory windows in Fig. 14d. In our previous work,[6] where F-N tunneling oxide is used, memory windows are easier to observe in Si nanocrystals because the oxide field in the tunneling oxide alone provides significant difference in injection and retention time characteristics. The inset graph shows the H_2-annealing effect on Si-nanocrystal MOS memories, which is performed at 450°C for 10 min in the Ar/H_2 ambient. By annealing in H_2, passivation of the interface and oxide traps associated with Si nanocrystals reduces the memory window from 0.57 V to 0.15 V. The fixed oxide charge is also reduced by the annealing, where a parallel shift in V_{FB} of about 2.3 V is observed. This clearly indicated that the role of traps at the interface and inside of nanocrystals is critical for semiconductor nanocrystal memories. Lower write/erase efficiency caused by a voltage drop across semiconductor nanocrystals and non-optimum, Si-nanocrystal formation can also reduce the memory window of Si-nanocrystal MOS capacitors.

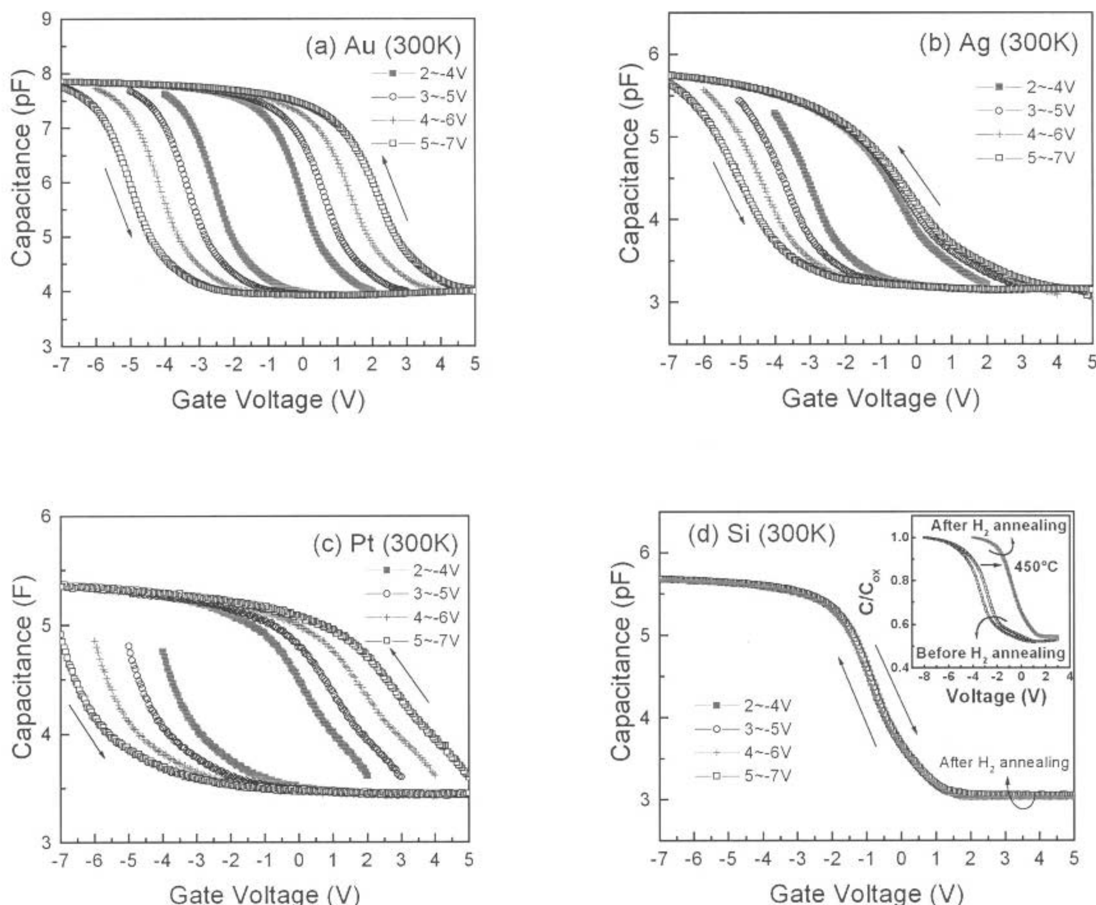

Fig. 14. High-frequency C-V characteristics of (a) Au-, (b) Ag-, (c) Pt-, and (d) Si-nanocrystal MOS memories at 1 MHz. The capacitor area is 90 μm × 90 μm.

Figure 15 shows the comparison of V_{FB} shifts by positive and negative voltage writing in 100 μm × 100 μm nanocrystal MOS capacitors. The principle of work function engineering is clearly demonstrated when electrons are injected into nanocrystals by positive voltage writing. While Si-nanocrystal MOS memories have very small V_{FB} change because of minimal d_{eff}, Au- and Pt-nanocrystal MOS capacitors show almost a linear change of V_{FB} in the positive voltage. For Ag nanocrystals, the small d_{eff} limits the storage capacity for electrons. However, negative voltage writing for all the metal-nanocrystal MOS capacitors does not show any saturation in the given voltage range. This is mainly due to the low tunneling probability of holes and band bending in the p-type substrate in this low voltage range. The different V_{FB} slopes ($\Delta V_{FB}/V_{write}$) of nanocrystals indicate that sizes and number densities of nanocrystals as well as d_{eff} are also responsible for the V_{FB} shifts. Further proof of work function engineering in metal nanocrystals can also be observed from the retention characteristics in Fig. 16, where the deep d_{eff} of Au and Pt gives longer retention.

If the size of nanocrystals is small enough to have Coulomb energy, $E = e^2/2C_{nc}$, where C_{nc} is the nanocrystal capacitance, much larger than the thermal energy (kT) and the tunneling oxide is thin enough for carriers to effectively tunnel through, the Coulomb blockade effect of single electron charging can be observed by electrical measurements.[33] Tight nanocrystal size distribution is an important factor because the stepwise V_{FB} shift caused by single carrier charging can be smeared because of several values of energy spacing from various nanocrystal

Table III. Calculation of Charge Storage Capacity for Effective Potential Well

Parameters	Au	Ag	Pt/Si
Effective potential-well depth	0.89 eV	0.41 eV	0.9 eV
Mean size of nanocrystals	6.26 nm	6.63 nm	8.04 nm
Estimated number of electrons	8	4	10
Coulomb energy gap (e^2/C)	0.118 eV	0.111 eV	0.092 eV
ΔV_{FB} by one electron	~0.60 V	~0.42 V	~0.35 V

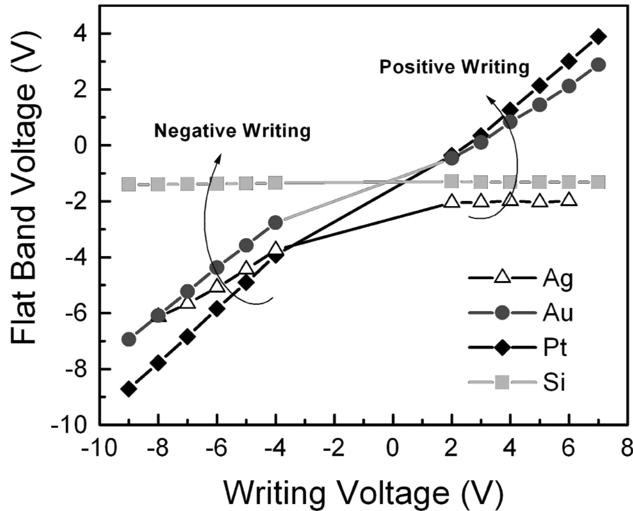

Fig. 15. The V_{FB} shift of nanocrystal MOS memories extracted from Fig. 14.

sizes. Figure 17 demonstrates step-by-step the Coulomb blockade effect caused by electron charging in Au-nanocrystal MOS memories at 77 K. The measured devices are square capacitors with an area of 100 μm × 100 μm. The 100-KHz C-V is performed to measure the V_{FB} shift. For electron charging, the writing voltage is applied from 1.2–2.8 V in 0.1-V increments before the gate voltage is swept from inversion to accumulation. The room temperature C-V measurement shows equal amount of V_{FB} shift of ~0.07 V, which corresponds to average charging of ~0.11 e, as writing voltage increases by 0.1-V step. Thermal fluctuation as well as the size of nanocrystals makes it difficult to observe the Coulomb blockade effect at room temperature. With measurements at 77 K, the nonuniform V_{FB} shift is evidence of quantization. Two additional cryogenic-temperature effects, the kink effect, caused by dopant freeze-out,[34] and deep depletion, caused by minimal thermal generation of minority carriers, are also observed. This will be further investigated later. While V_{FB} at room temperature increases linearly with the gate voltage, plateaus are observed at 77 K. From average values in Table III, a V_{FB} shift of 0.6 V is expected for one electron charging per Au nanocrystal. However, between the 0.6-V steps, smaller steps from the nonuniform size distribution of nanocrystals are observed. The different Coulomb energy spacings (e^2/C_{nc}) are caused by the different sizes of nanocrystals. Larger nanocrystals can be charged with a different number of electrons than smaller nanocrystals at one writing voltage. The inset graph in Fig. 18 shows a ΔV_{FB} of ~0.2 V will be most frequently observed with the given Au-nanocrystal size distribution.

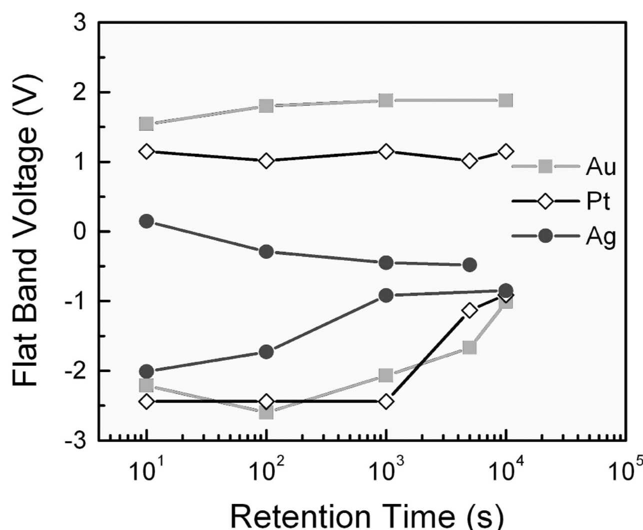

Fig. 16. The retention characteristics of Au-, Ag-, and Pt-nanocrystal MOS memories. The initial write/erase conditions are ±4 V for 8 sec. Capacitance at 100 KHz is monitored at a constant bias of 0 V. The capacitor area is 150 μm × 150 μm.

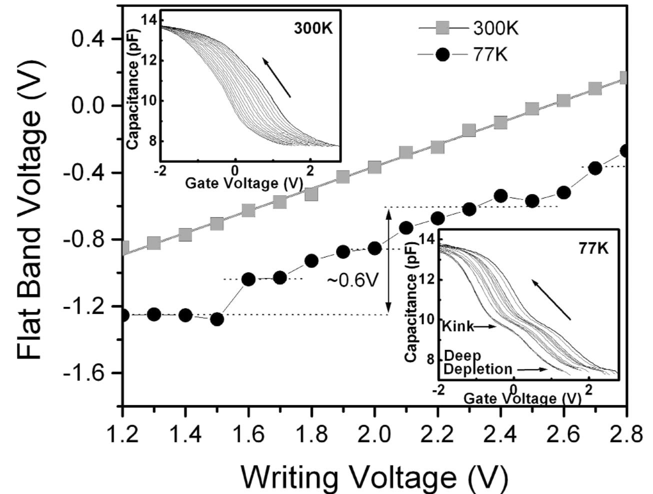

Fig. 17. The Coulomb blockade effect in Au-nanocrystal memories for positive voltage writing. The C-V is measured at 300 K and 77 K. The flat band voltage is expressed as a function of the writing voltage.

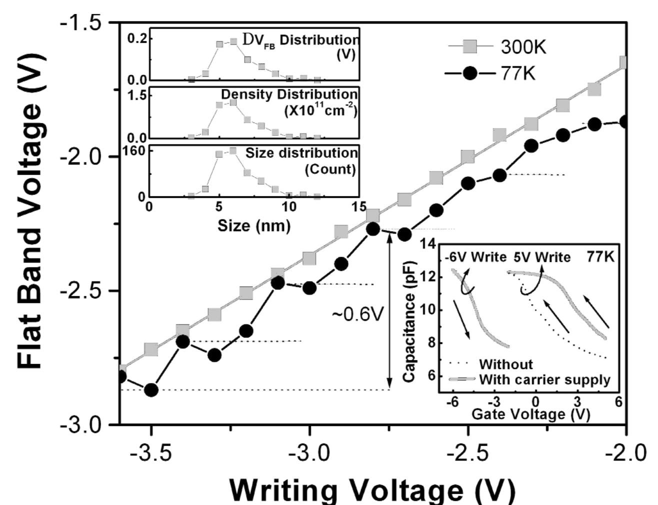

Fig. 18. The Coulomb blockade effect in Au nanocrystal MOS memories for negative voltage writing. The flat band voltage is expressed as a function of the writing voltage. The ΔV_{FB} distribution in the upper inset graph is calculated from the number density and size distribution of Au nanocrystals. The freeze-out effect on Au-nanocrystal MOS capacitors at 77 K is in the lower inset graph. Additional carriers are selectively supplied by photogeneration. The C-V is measured at 100 KHz.

The participation of holes in memory operation is evident from the result of the parallel shift of capacitance in the negative direction by negative voltage writing. The Coulomb blockade effect corresponding to holes is measured at 77 K in Fig. 18. The writing voltage increment of 0.1 V from −2 V to −3.6 V is applied for hole injection. Capacitance is measured from accumulation to inversion regions during the control gate-voltage sweeps. A steady increase of $V_{FB} \sim 0.06$ V for every 0.1 V at room temperature, and no quantization is observed. Similar to the case for electrons, the low-temperature C-V shows V_{FB} plateaus from the quantization effect with the same 0.6-V major steps and 0.2-V minor steps. The kink effect was not observed in hole injection. At cryogenic temperatures, the freeze-out effect will influence the C-V curves and can be used to explain the different trends between hole and electron charging. The freeze-out effect on carrier injection is further illustrated in the lower inset graph in Fig. 18. When excess minority carriers are supplied by photogeneration of electron-hole pairs during writing, C-V kinks caused by freeze-out are not observed for electron injection. For hole injection, surface band bending by the gate voltage ionizes the acceptors and electrically supplies holes, whose amount is sufficient to fully charge nanocrystals at −6 V writing, and hence, no C-V kinks exist even without photogeneration.

CONCLUSIONS

The fabrication of metal nanocrystal memories in the aspects of potential-well depth and width was investigated. Oxide in the direct-tunneling regime is chosen for fast write/erase and low voltage operations. The Au, Ag, and Pt nanocrystals are formed to compare potential wells of different work functions and to demonstrate long retention and large storage capacity. Small mean size, small size distribution, and high density of nanocrystals are achieved by controlling process parameters including annealing temperature, initial deposited-film thickness, and substrate doping.

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