Fabrication and Characterization of 4H-SiC P-N Junction Diodes by Selective-Epitaxial Growth Using TaC as the Mask

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Selective nitrogen doping of 4H-SiC by epitaxial growth using TaC as the high-temperature mask has been demonstrated. Nomarski optical microscopy and scanning electron microscopy (SEM) were used to characterize selective growth of SiC. In addition, 250-μm, square-shaped, p-n junction diodes by selective n-type epitaxial growth on a p-type epilayer were fabricated. The refilled fingers with different width were designed to vary the periphery/area (P/A) ratio. The effects of P/A ratio on the current-voltage (J-V) characteristics have been investigated. The ideality factor extracted from J-V characteristics is ≈2 at a temperature range of 25–275°C, which indicates that the Shockley–Read–Hall recombination is the dominant mechanism in the conduction region. The reverse leakage current does not show dependence on P/A ratio for trench-refilled diodes. The room-temperature reverse leakage-current density at 100 V is less than 3.5×10^{-7} A/cm^2 for all diodes. Also, the reverse leakage current does not increase significantly with temperature up to 275°C. The breakdown voltages measured at room temperature are about 450 V and 400 V for diodes without and with fingers, respectively.

Key words: 4H-SiC, selective-epitaxial growth, junction diodes, chemical-vapor deposition

INTRODUCTION

Silicon carbide (SiC) is expected to be a promising material for high-voltage semiconductor devices. Properties, such as high avalanche electric breakdown field ($\sim 2 \times 10^6$ V/cm), large bandgap (~3 ev), and high thermal conductivity (~3–4 W/cmK) make it attractive for high-voltage applications. There has been significant progress in the epitaxial growth and device processing of SiC for use in high-power and high-temperature electronics in recent years. Several epitaxial and implanted junction rectifiers have been reported.[1–3] However, currently ion implantation is the only viable means to realize selective area doping of SiC, as dopant diffusion is extremely slow even at high temperature (>1,800°C) and fabrication of junctions using epitaxial technology followed by mesa etching compromises surface planarity. A subsequent process of high-temperature annealing is required to reduce resulting lattice damage and to electrically activate implanted dopants. Some defects remain stable even after 1,700°C annealing.[4,5] Anisotropic diffusion during the high-temperature annealing[6] also makes accurate control of the doping profile difficult. An alternative method of doping of SiC is via diffusion.[7,8] Recently, Soloviev et al.[9] and Gao et al.[10,11] demonstrated successful local planar-doped regions in a SiC substrate by diffusion from a vapor phase using a graphite mask. Because very high temperature (1,800–2,100°C) is required for this process, an equilibrium vapor ambient in the crucible needs to be well controlled to avoid sublimation evaporation of SiC during diffusion. Also high-temperature lateral diffusion under the mask is not fully understood yet, which makes it difficult to control the doping profile of the selectively doped region by diffusion.

Selective-epitaxial growth of SiC could provide better quality layers, and it is possible to tailor the doping profile for device specification. However, because a relatively high temperature (~1,500°C) is required to obtain high-quality growth, a high-temperature

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mask is needed to achieve selective growth/doping. Recently, we have reported selective growth of SiC using TaC as the mask.[12] In this paper, we demonstrate the local planar-doped regions in a SiC substrate by epitaxial growth using TaC as the mask. Trench-refilled 4H-SiC p-n junction diodes have also been fabricated using the selective-epitaxial growth technique. Cross-sectional SEM was used to study the trench-refill process. The J-V analysis has been carried out to evaluate the electrical performance of the trench-refilled p-n junction diodes.

EXPERIMENTAL CONDITIONS

A commercial, 8° off (0001) Si-face, p-on-p^+ 4H-SiC wafer was used as the starting material. The nominal thickness and Al doping concentration of the p epilayer are 12 μm and 9×10^{15} cm^{-3}, respectively. The Ta film of 600–800-Å thickness was deposited by electron beam evaporation and patterned using standard photolithography. The SiC and Ta film were etched by reactive ion etching (RIE) using CHF_3/O_2 plasma, and the etched trenches are about 1.5-μm deep. Epitaxial growth of SiC was carried out in a conventional, horizontal cold-wall reactor at temperatures in the range of 1,500–1,600°C and reactor pressure of 80 torr. Silane, propane, and nitrogen are used as the precursors with hydrogen as the carrier gas. The flow rates of silane, propane, nitrogen, and hydrogen were kept at 2.2 sccm, 3.7 sccm, 8 sccm, and 12.5 slm, respectively. The Ta film was converted to TaC by exposing the wafer to 150-ppm propane in hydrogen ambient at 1,300°C for 15 min.[12] The RIE-etched trenches were refilled by nitrogen-doped, n-type epitaxial films grown by selective epitaxy. After the growth, the TaC mask was removed by etching in a 1:1:1 = HNO_3:HF:H_2O wet etchant. The surface looks smooth under optical microscopy after etching, though residual TaC or Ta-SiC reaction products on the surface may still be present but will not be detected by J-V measurements if the residual products are not continuous on the surface. The nominal planar doping is about 4.9×10^{16} cm^{-3} as determined by the mercury-probe capacitance-voltage measurement shown in Fig. 1.

A diode structure, as shown in Fig. 2, was fabricated by standard photolithography. The SiO_2 provides edge termination of the diode metal contact. A shallow phosphorus implantation using five successive implants with varying energies and total dose of 4×10^{15} atoms/cm^2 was applied to form an n^+ ohmic-contact layer. The Ti/Ni/Al ohmic contact to the n^+ layer was formed by a lift-off technique. The Al/Ni/Al stacking layers were employed to form a large-area back-side contact to the p^+ substrate. Both contacts were annealed at 1,050°C for 5 min in Ar ambient, and Ti/Mo metals were used as the interconnect metal.

RESULTS AND DISCUSSION

Figure 3 shows the optical microscope top views and cross-sectional SEM of the diodes after selective

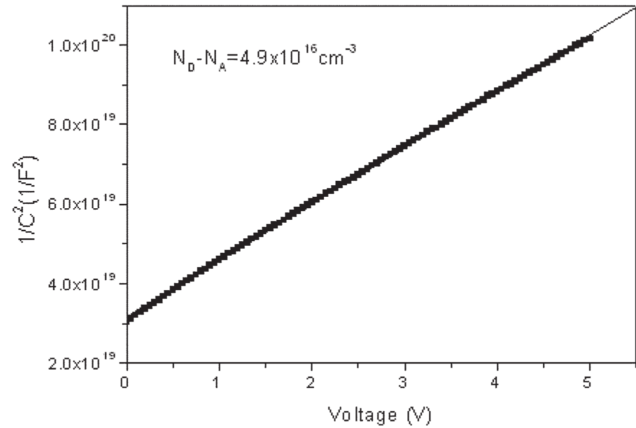

Fig. 1. Room-temperature capacitance-voltage characteristics of a layer grown on a non-patterned substrate.

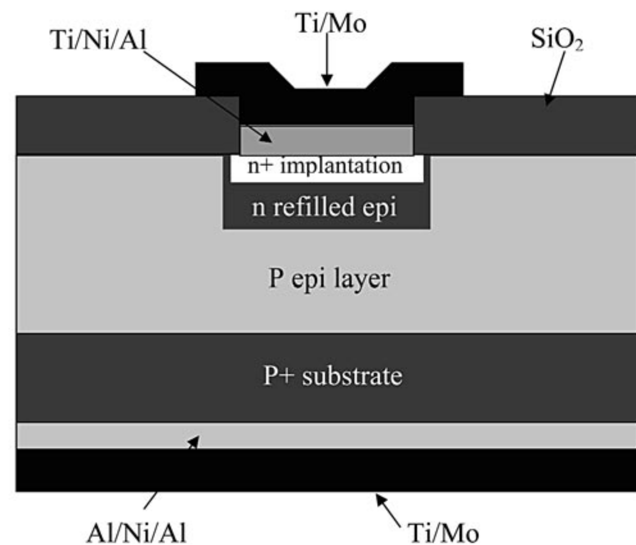

Fig. 2. Schematic structure of the trench-refilled p-n diode.

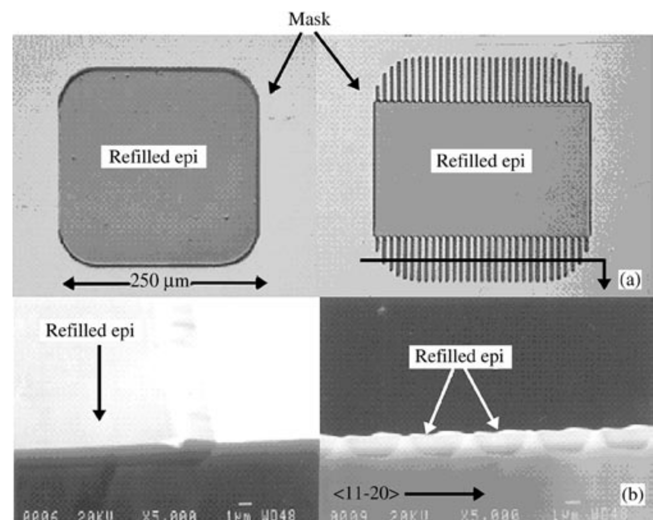

Fig. 3. (a) Microscope top views and (b) cross-sectional SEM views of the diodes after selective growth.

growth. In this set of devices, the fingers are oriented along <1–100>. Because of the different dopants in p and n epilayers, the SEM contrast is different for p and n layers. Cross-sectional SEM was used to study the refill process. On the basis of the cross-sectional SEM images, we have direct evidence that the n-type epilayer was regrown in the RIE-etched trenches. From this and other unpublished data, we conclude that the regrown epitaxial layer fills in the trenches smoothly, and no visible voids are observed at the interface of the junction when the aspect ratio (w/h) is >1. We believe that the propane/hydrogen pre-etching before the epi growth, which is used to eliminate the defects on the substrate surface,[15] could also cure the defects left by RIE etching. As shown in Fig. 3, the selective growth was controlled in such a way that the growth occurs only in the trenches, and the refilled epilayer surface is at the same level as the original surface. Therefore, planar selective doping of SiC is achieved by epitaxial growth when the orientation of the trenches are along <1–100>. When the orientation of the trenches are along <11–20>, a non-planar surface with a significant amount of edge growth was observed, as shown later in Fig. 10. The TaC mask was then removed after selective growth using a mixture of a 1:1:1 = HNO_3:HF:H_2O wet etchant.

The forward and reverse J-V of a square (250 μm × 250 μm) trench-refilled diode without fingers were compared to that of a mesa-etched PIN circular diode. The schematic of the two diodes and the J-V characteristics for these two diodes are shown in Fig. 4a and b, respectively. Similar J-V characteristics were observed for both diodes, indicating that damages caused by RIE etching might have been cured during the epitaxial growth, and the junction interface is as good as a PIN diode fabricated by planar epitaxial growth. The difference of the forward J-V at higher current is possibly due to the higher series resistance of the p-type base of the trench-refilled diode.

To investigate the effects of the periphery and trench-bottom-etched surface on the electrical performance of the diodes, two sets of diodes were fabricated. Both of them are of square shape with side length of 250 μm. One is a blanket square-refilled diode without fingers, the other is square diodes with varied finger width (Fig. 3). The 250 μm × 150 μm contact metal was deposited on the center of the diodes. The series resistance will be different for

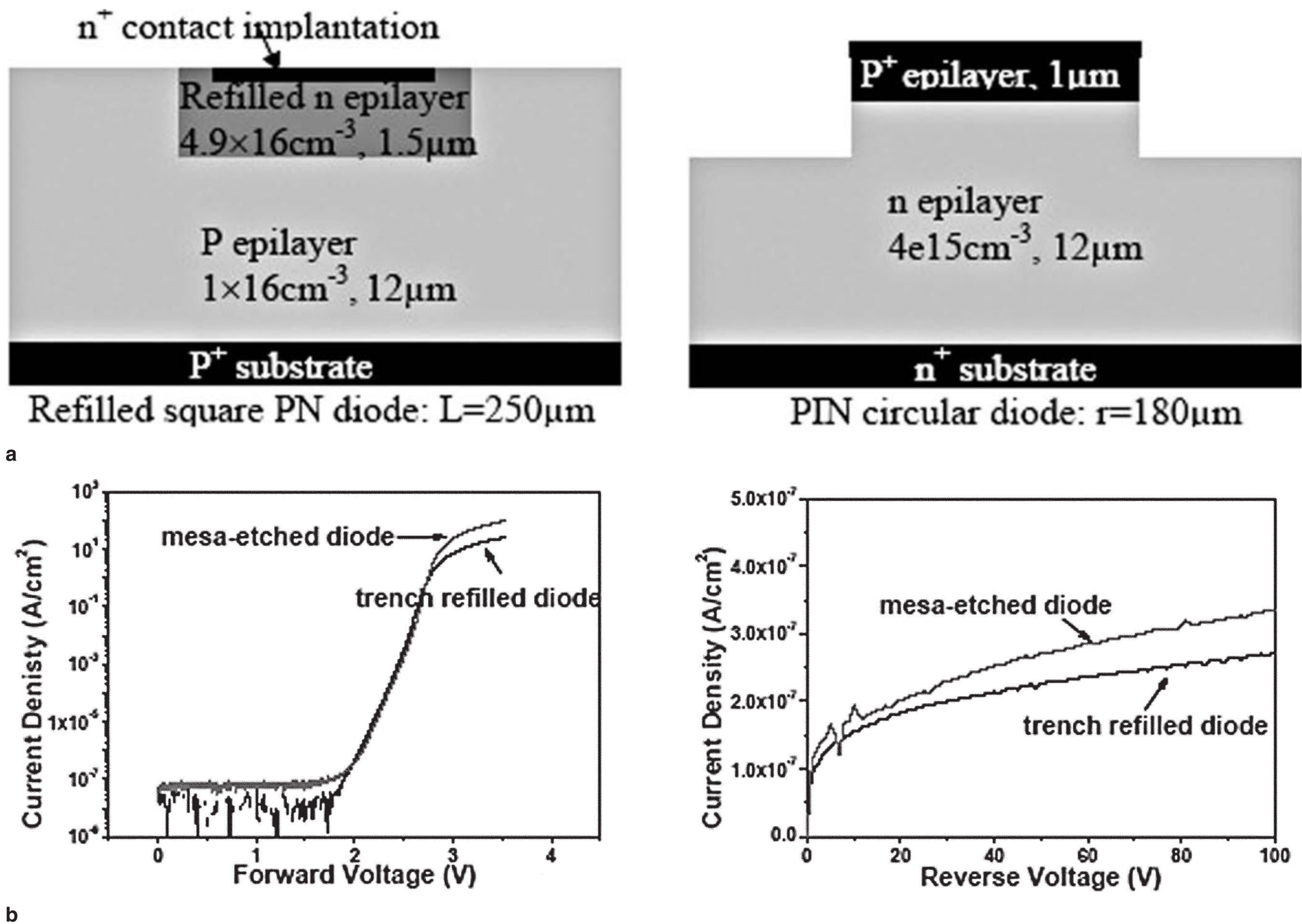

Fig. 4. (a) Schematic of trench-refilled square diode and mesa-etched PIN circular diode and (b) forward and reverse J-V characteristics of trench-refilled square diode and mesa-etched PIN circular diode.

diodes with varied finger width and mask width. However, the exponential conduction region of the forward J-V characteristics is the focus of the study rather than the series resistance region, and hence, the series resistance has less or no effects on evaluating diode performance. Two groups of variations are designed to change either the periphery or the trench bottom area. One variation is to keep the ratio of refill window width/mask width equal to 1 and vary the window (and the mask) width from 2 μm to 6 μm. Because the side length of the diodes is fixed, the total trenched bottom area is 50% of the total areas covered by fingers for all diodes in this group. However, the width of the repeat unit (as depicted in Fig. 5) changes from 4 μm to 12 μm; therefore, periphery varies with repeat-unit width. The other group of variations is to keep the total repeat-unit width equal to 8 μm and vary the refill window width and mask width from 2 μm to 6 μm. Periphery is the same in this group of variations as the number of the repeat unit is fixed, and trench bottom area varies with refill window width. As can be seen in Fig. 6, the trench-refilled 4H-SiC diodes exhibit classical forward-bias characteristics. Because very similar J-V characteristics are present,

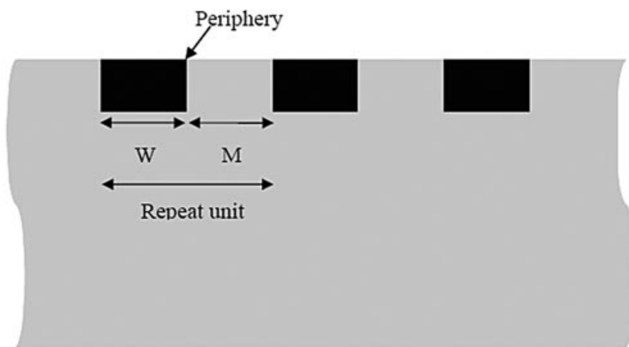

Fig. 5. Schematic of cross section of fingers with varied width. W and M are varied for different diodes.

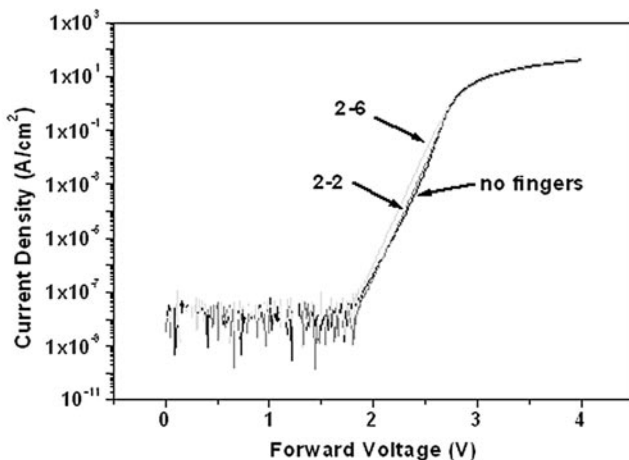

Fig. 6. Forward J-V characteristic of typical diodes with and without fingers (2–2 corresponds to 2-μm refill window width, 2-μm mask width; 2–6 corresponds to 2-μm refill window width, 6-μm mask width, and so on).

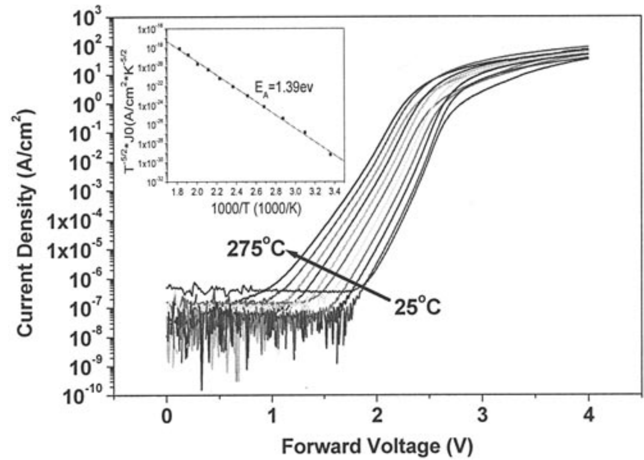

Fig. 7. Forward J-V characteristics of the diode without fingers at different temperatures (the insert shows the Arrhenius plotting for the thermal activation energy).

only three typical curves are shown. The distinctive exponential region was observed, and it is the most useful for extracting the electrical parameters for junction diodes. The diodes with different finger-width variations have similar J-V characteristics compared to the diodes without fingers, and no significant differences are observed. The forward J-V characteristics at different temperatures (J-V-T) from 25°C up to 275°C were also measured. The typical J-V-T characteristic of a diode without fingers is shown in Fig. 7. The ideality factor, n, was extracted to be 1.94–2.08 at different temperatures, which indicates that Shockley–Read–Hall recombination is the dominant mechanism in the conduction region. The activation energy, E_A = 1.39 eV, is obtained from an Arrhenius plot of $\ln(J_0)$ versus 1,000/T using the best linear fit to the expression $J_0 \propto T^{5/2} \exp(-E_A/kT)$.[13] Similar J-V-T characteristics were obtained for diodes with varied finger width. The same analysis was carried out, and the extracted activation energy E_A was found to vary from 1.36 eV to 1.50 eV for diodes with different finger width. Note that there is no trend to indicate the correlation between the difference of activation energy and P/A ratio variations. The reverse leakage current up to 100 V did not show significant differences between diodes with varied P/A ratios, as shown in Fig. 8. The room-temperature reverse leakage-current density at 100 V is less than 3.5×10^{-7} A/cm^2. Figure 9 clearly shows little change of leakage current up to 275°C, indicating that less or no thermally active generating centers are presented in these trench-refilled 4H-SiC p-n diodes that was reported for some SiC p-n junction diodes fabricated by ion implantation.[13,14] The breakdown voltages at room temperature for diodes with and without fingers are 400 V and 450 V, respectively. The lower breakdown voltage for the diode with fingers may be due to sharp junction corners presented in fingers. When the trenches are aligned parallel to <11–20>, edge overgrowth ("rabbit ears") is observed (Fig. 10), as

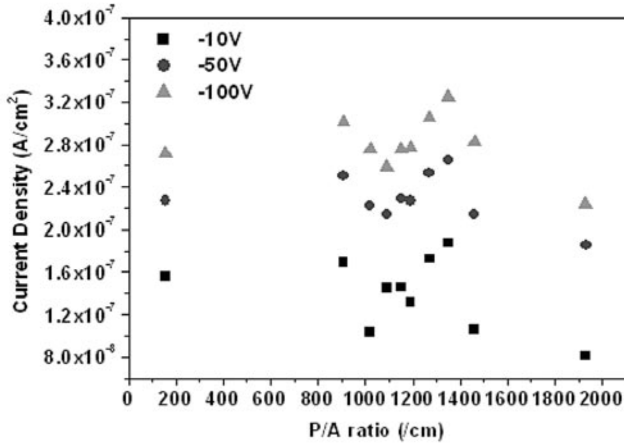

Fig. 8. Plot of reverse leakage-current density versus P/A ratio at −10 V, −50 V, and −100 V.

described elsewhere.[12] The refilled window perpendicular to <11–20> is preferred to maintain planarity of the wafer surface, although both types of devices did not show degrading J-V performance in our study.

As shown in Fig. 11, polycrystal deposition on the mask was observed for part of the 1/4 2-in. wafer, and they can not be completely removed by wet etching as described previously. This may be due to the nonuniform growth conditions in the reactor. Higher leakage current was measured for these diodes (Fig. 12), indicating that surface quality of the mask region is critical for the J-V performance of the trench-refilled diodes.

CONCLUSIONS

Planar-selective nitrogen doping of 4H-SiC by epitaxial growth using TaC as a high-temperature mask has been demonstrated. No voids at the interface between the refilled epitaxial layer and substrate were observed. P-n junction diodes by selective, n-type epitaxial growth on a p-type epilayer were fabricated. Current-voltage measurements were carried out to evaluate the electrical performance of the refilled junction diodes. All diodes exhibited classical J-V characteristics. Similar J-V was observed for a trench-refilled junction diode and for a mesa-etched PIN diode. The ideality factor

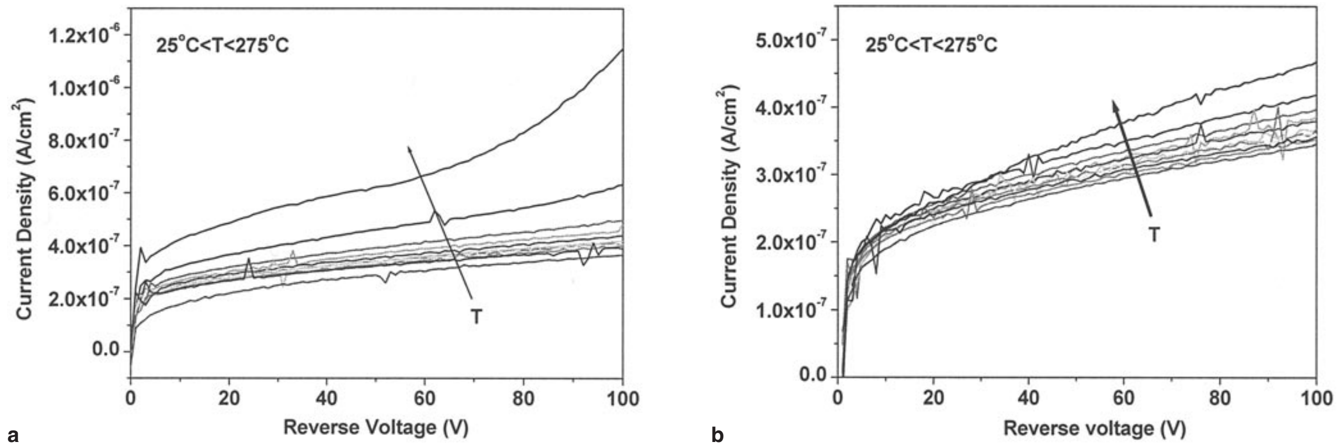

Fig. 9. Reverse J-V characteristics of the diodes at different temperatures (a) without fingers and (b) with 2–2-μm fingers.

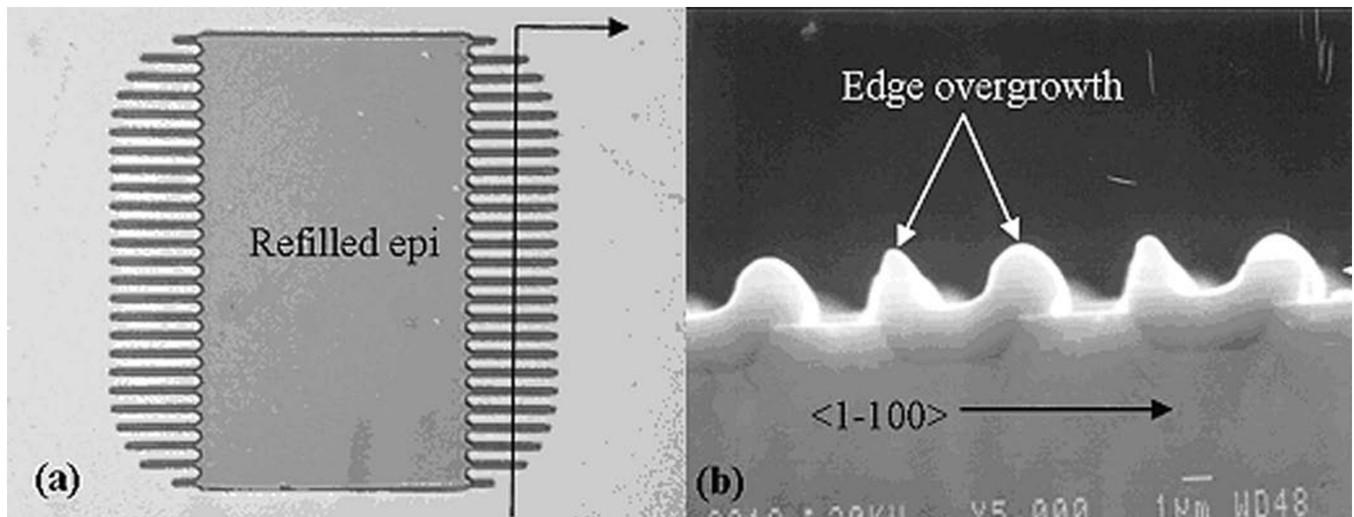

Fig. 10. (a) Microscope top view and (b) cross-sectional SEM view of the diode after selective growth when the trenches are parallel to <11–20>.

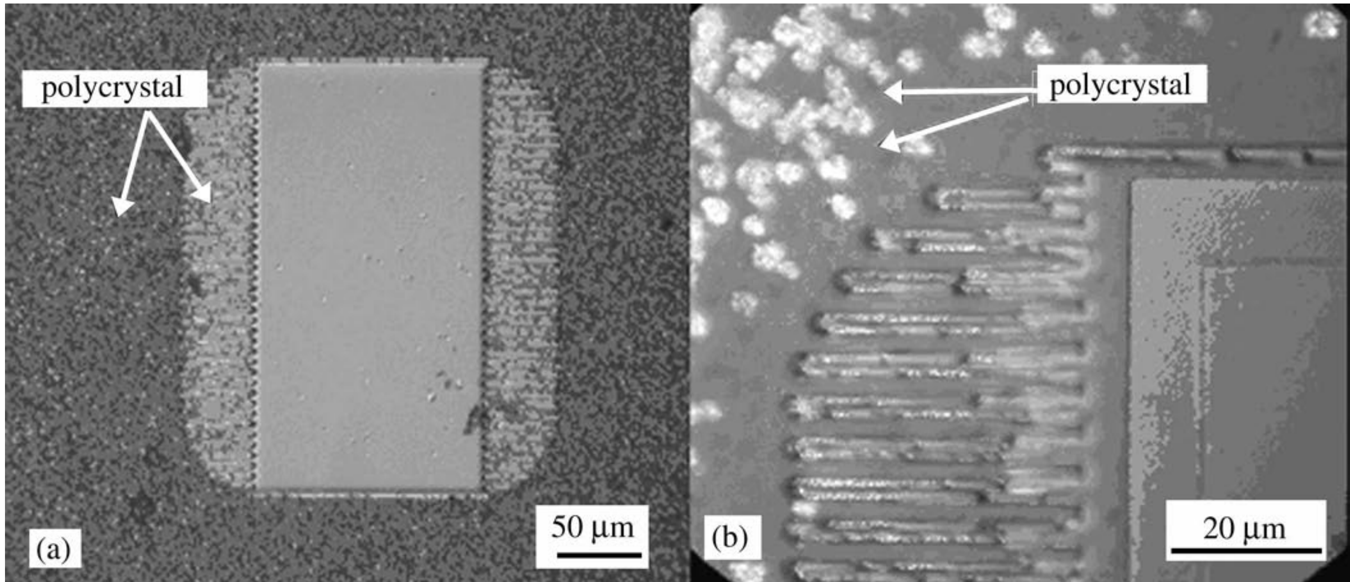

Fig. 11. Microscope top views of the diodes with polycrystal deposition: (a) after growth and (b) after wet etching and metal deposition.

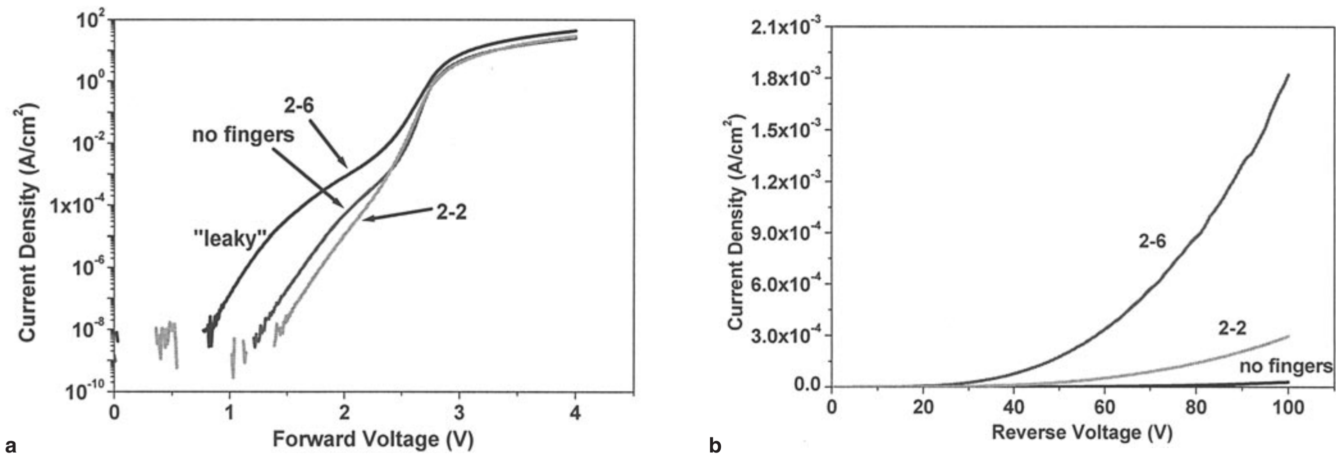

Fig. 12. (a) Forward and (b) reverse J-V characteristics of typical diodes grown under non-optimum selective growth conditions (2–2 corresponds to 2-μm refill window width, 2-μm mask width; 2–6 corresponds to 2-μm refill window width, 6-μm mask width, and so on).

extracted from J-V characteristics was found to be ≈2 at a temperature range of 25–275°C, which indicates that Shockley–Read–Hall recombination is the dominant mechanism in the conduction region. Both forward and reverse J-V characteristics did not show dependence on P/A ratio for trench-refilled diodes. The room-temperature reverse leakage-current density at 100 V was found to be less than 3.5×10^{-7} A/cm^2 for all diodes. The reverse leakage current did not increase significantly with temperature up to 275°C. Surface quality of the mask region was found to be critical for the J-V performance of the trench-refilled diodes.

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