Textural and Microstructural Transformation of Cu Damascene Interconnects after Annealing

JAE-YOUNG CHO,[1,3] HYO-JONG LEE,[2] HYOUNGBAE KIM,[1] and JERZY A. SZPUNAR[1]

1.—Department of Mining, Metals and Materials Engineering, McGill University, Montreal, PQ, H3A 2B2, Canada. 2.—School of Materials Science and Engineering and Research Institute of Advanced Materials, Seoul National University, Seoul 151-744, Korea. 3.—E-mail: jcho@po-box.mcgill.ca

Influence of annealing on the textural and microstructural transformation of Cu interconnects having various line widths is investigated. Two types of annealing steps have been considered here: room temperature over 6 months and 200°C for 10 min. The texture was determined by x-ray diffraction (XRD) of various cross-sectional profiles after electropolishing, and the surface, microstructure, and grain boundary character distribution (GBCD) of Cu interconnects were characterized using electron backscattered diffraction (EBSD) techniques. In order to analyze a relationship between the stress distribution and textural evolution in the samples, microstresses were calculated with decreasing line widths at 200°C using finite element modeling (FEM). In this investigation, it was found that the inhomogeneity of stress distribution in Cu interconnects is an important factor, which is necessary for understanding textural transformation after annealing. A new interpretation of textural evolution in damascene interconnects lines after annealing is suggested, based on the state of stress and the growth mechanisms of Cu electrodeposits.

Key words: Cu damascene interconnects, texture, microstructure, stress, grain boundary character distribution (GBCD), electron backscattered diffraction (EBSD)

INTRODUCTION

As the feature sizes of integrated circuits (ICs) are scaled down to submicron dimensions, device manufacturers need new technology to meet performance and reliability requirements in the interconnect processes. According to these technology demands, the damascene copper interconnect process has become an important issue in the IC industry since it permits a decrease in resistance and capacitance (RC) delay, reduces the number of processing operations, and increases the lifetime of the interconnect lines.[1]

Since the Cu damascene process has been introduced in the manufacture of ICs, significant research on the relationship between texture and reliability of copper interconnects has been undertaken.[2–5] It is well known that strong (111) texture increases the resistance of electromigration failure and this failure can be correlated with the frequency of the occurrence of coincidence site lattice (CSL) boundaries or low or high diffusivity boundaries and the strength of {111} texture in aluminum thin films.[6] However, such relationships for Cu have not been firmly established and the driving forces that can affect the textural and microstructural transformation during annealing have not been clearly identified until now.[7–11]

In this study, the details of textural and microstructural transformation will be explained using x-ray diffraction (XRD) and electron backscattered diffraction (EBSD) techniques. The stress contribution on the evolution of texture and microstructure during annealing will be discussed. A new model for the texture transformation based on the state of stress and growth mechanisms of Cu electrodeposits

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will be proposed for decreasing line widths after annealing.

EXPERIMENTAL PROCEDURE

Two samples, one as-deposited and another annealed, having a different cross-sectional profile, as shown in Table I, were used for x-ray texture measurements. Both samples were fabricated using the same process conditions and were kept at room temperature for 6 months. TaN, 400-Å thick, was deposited on the surface of the Si (100) wafer as the barrier layer, and a copper seed layer was deposited on the barrier layer. The trenches were then filled with copper by electroplating in a sulfuric acid bath using current density of 24 mA/cm^2. To remove the overburden of Cu interconnects, the samples were electropolished for 120 sec and 130 sec, respectively, in a H_3PO_4 solution using 17 mA/cm^2 current density. The samples were annealed at 200°C for 10 min in a vacuum furnace to avoid oxide formation on top of Cu interconnects. Each sample has different line widths from 0.14 μm to 2 μm and every line has the same trench depth of 0.7 μm. After electropolishing for 120 sec (Table I), the top surface area of the trench was analyzed using the EBSD method.

In order to obtain quantitative information from the sample surface, the crystallographic texture of copper interconnects was measured using a Siemens (Munich, Germany) D500 x-ray goniometer with a copper tube. Pole figures were obtained using the reflection technique, up to a maximum tilt of the specimen of 80° in 5° intervals. The orientation distribution function (ODF), the {111} fiber texture, and the percentage of different texture components were calculated using TexTools, a commercial software for texture analysis.[12] The orientation imaging microscope mounted on a Philips XL30 FEG-SEM (Eindhoven, the Netherlands) was used to identify the orientation of each grain and the type of grain boundaries in the copper interconnects. The coincidence site lattice (CSL) grain boundaries were identified from the electron backscattered pattern. The frequency of occurrence of these boundaries up to Σ29 was calculated. The stress distribution in interconnects was calculated by finite-element method (FEM) modeling using FEMLAB, a commercial software.[13]

RESULTS

Through-Thickness Inhomogeneity of Texture in Copper Interconnects

In order to acquire quantitative information on the crystallographic texture of copper interconnects, XRD and EBSD techniques were used in this study. Since the XRD method has a wide-range scan area, it was used only to obtain average through-thickness information about texture, and EBSD was used for the detailed analyses of texture, microstructure, and grain boundary character distribution (GBCD) of copper interconnects on the surface area for a different line width.

To obtain quantitative information about the through-thickness inhomogeneity of texture, three pole figures were measured and the ODFs were calculated, as shown in Table II. This table shows an ODF at $\varphi_2 = 45°$ section and illustrates the intensity changes of {111} fiber texture for each profile of Cu electrodeposits: weak fiber texture was found after electroplating; however, its intensity becomes stronger at a higher depth of Cu interconnect in the as-deposited sample. After annealing, it was noticed that its intensity varies and some other texture components developed depending on the cross-sectional profile of Cu electrodeposits. Plots of {111} fiber at each cross-sectional profile are shown in

Table I. Schematic of the Cross-Sectional Profile of Cu Interconnects

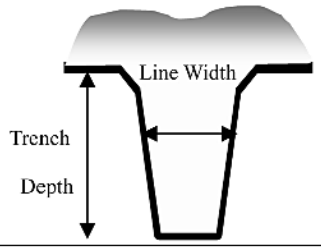
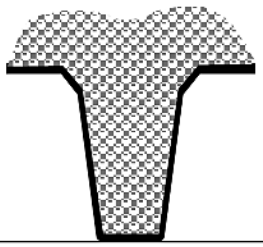
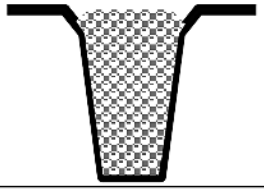
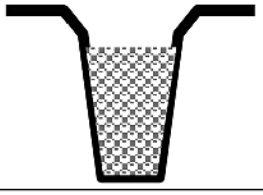
	Overburden ▲ (after electroplating)	After Electropolishing	
		Top surface (120 sec) ■	Inside of trench (130 sec) ●
As-deposited			
Annealed			

Table II. Sections of ODFs for $\varphi_2 = 45°$ at a Different Cross-Sectional Profile of Cu Interconnects after Electropolishing

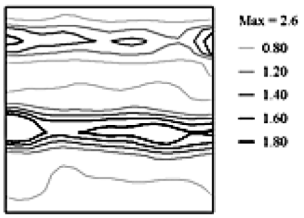
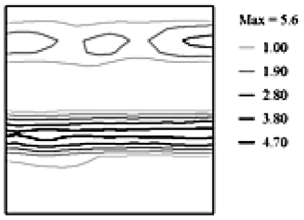
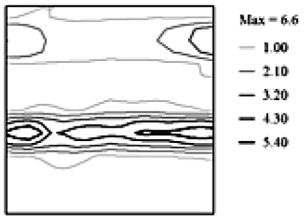
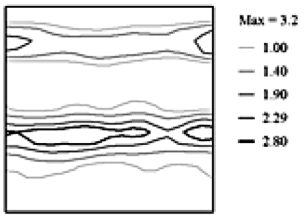
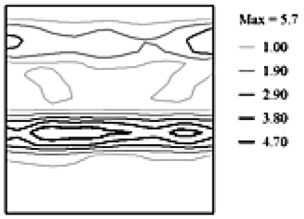
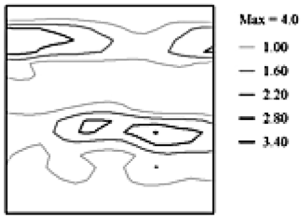
	Overburden▲ (after electroplating)	Electropolished	
		120 second■	130 second●
As-deposited			
Annealed			

Fig. 1 to describe these through-thickness intensity changes for {111} fiber texture.

The texture of the as-deposited sample shows weak {111} fiber. However, after removing the overburden layer of copper by electropolishing, the fiber intensity increased. After annealing, the texture of the overburden layer does not change much. However, textures of the trench under this layer are transformed. At first, after electropolishing for 120 sec, specific directions on the {111} texture are developed, as indicated by arrows (Fig. 1b). After electropolishing for 130 sec, which means a half-depth of the trench, the {111} fiber texture is decreased and a weak (111) [110] texture is developed. This is due to the increasing constraints generated by the sidewall at the bottom of the trench, which may affect the directional texture development of copper in the trench. The obtained results demonstrate the large through-thickness inhomogeneity of the texture in the trench after annealing. Possible effects of stress, which are related to the sidewall constraints on the directional texture development of Cu interconnects, will be discussed later.

In addition, a minor texture component described by {115} fiber is detected, as shown in Fig. 2. In this figure, it is demonstrated that the intensity of {115} fiber after annealing increases at (115)[1$\bar{1}$0], (115)[0$\bar{5}$1], and (115)[$\bar{2}\bar{3}$1] orientations, as indicated

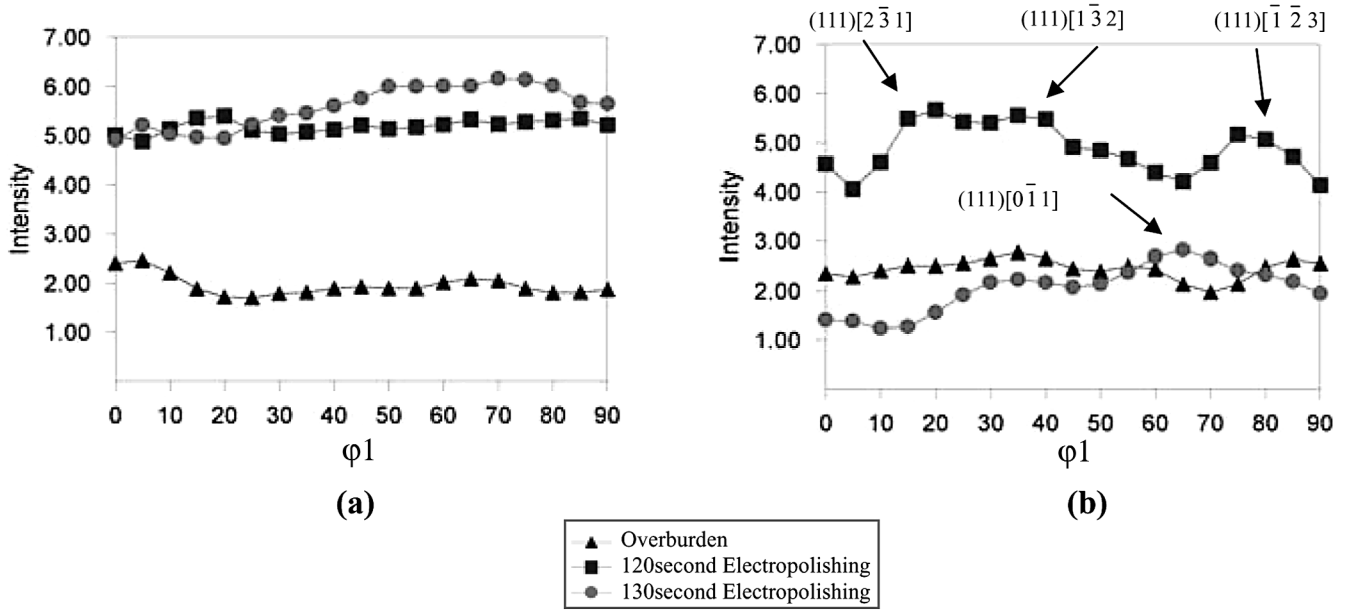


Fig. 1. {111} fiber plots at different cross-sectional profiles of Cu interconnects: (a) as deposited and (b) after 200°C annealing.

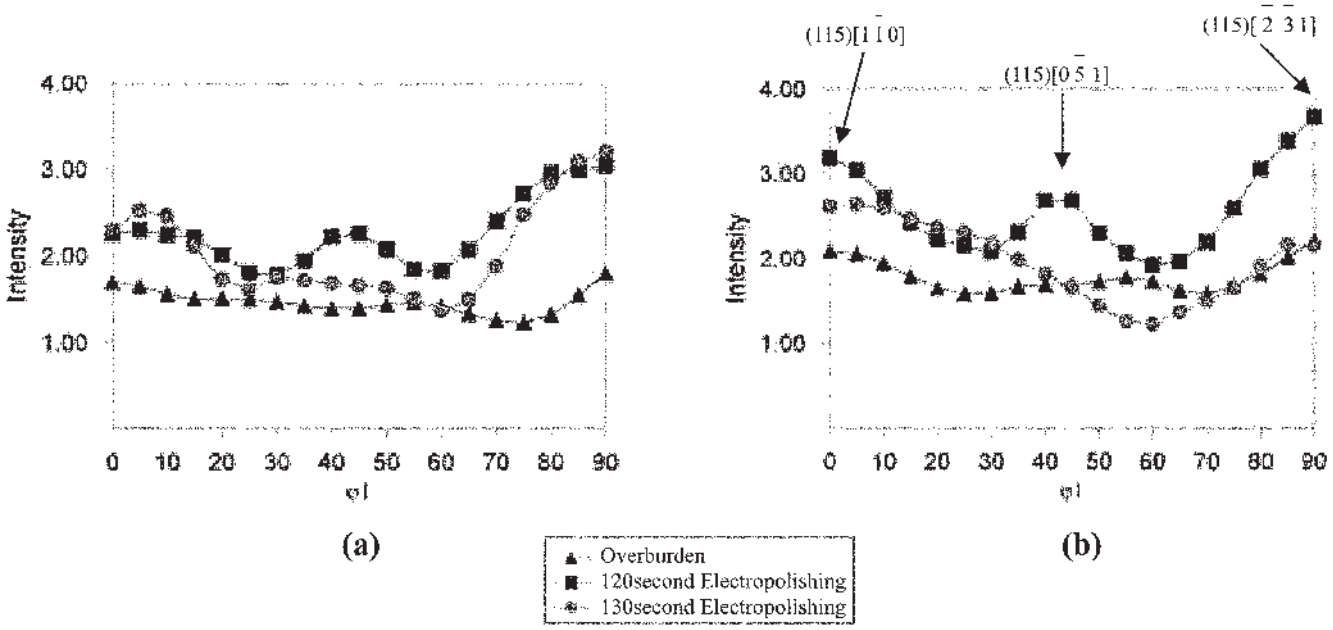


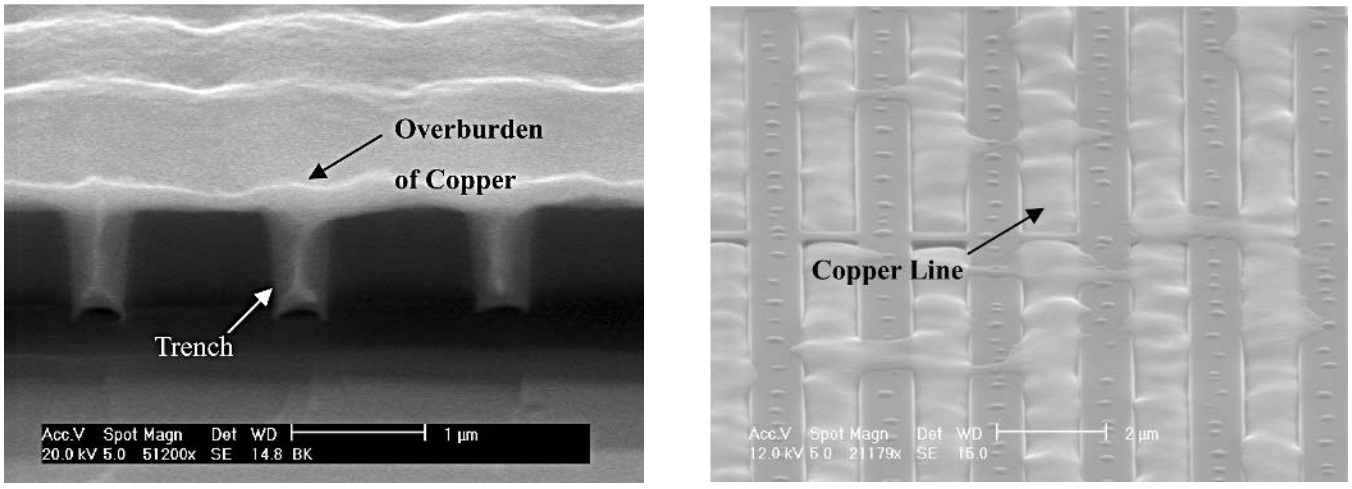
Fig. 2. {115} fiber plots at different cross-sectional profiles of Cu interconnects: (a) as deposited and (b) after 200°C annealing.

by arrows in Fig. 2b. All the minor components that have {115} plane parallel to the specimen surface can develop as a result of twin formation during annealing. This finding is supported by EBSD measurements. The obtained results demonstrate that the through-thickness texture of Cu interconnects after annealing is different from the as-deposited specimen.

Texture, Microstructure, and GBCD on the Top Surface Area of Copper Interconnects

After filling the trench by Cu electroplating, irregular surface morphology is generated, as shown in Fig. 3a. To remove the overburden of copper and make the surface smooth, chemical-mechanical polishing is performed in the semiconductor industry. In this study, electropolishing is used to make a smooth surface of Cu interconnects and the EBSD technique is used to analyze the surface microstructure, the orientation of each grain, and the types of grain boundaries in the copper interconnects. However, the results from a 130 sec electropolishing are not reliable since it produces significant charging from the oxide layer and cannot be interpreted accurately. Therefore, in this study, only a 120 sec electropolished sample, which comes from the top surface area of Cu interconnects, was analyzed (Fig. 3b).

To obtain quantitative information about texture, three pole figures were measured from the top surface of Cu interconnects using the EBSD technique. The results presented in Fig. 4 indicate that {111}<110> textures exist in all samples. However, they become fiberlike textures as the line width increases. Compared to the as-deposited sample, the



a b

Fig. 3. SEM photos: (a) cross-sectional profile of Cu interconnects after electroplating and (b) top view after 120-sec electropolishing to remove overburden of Cu.

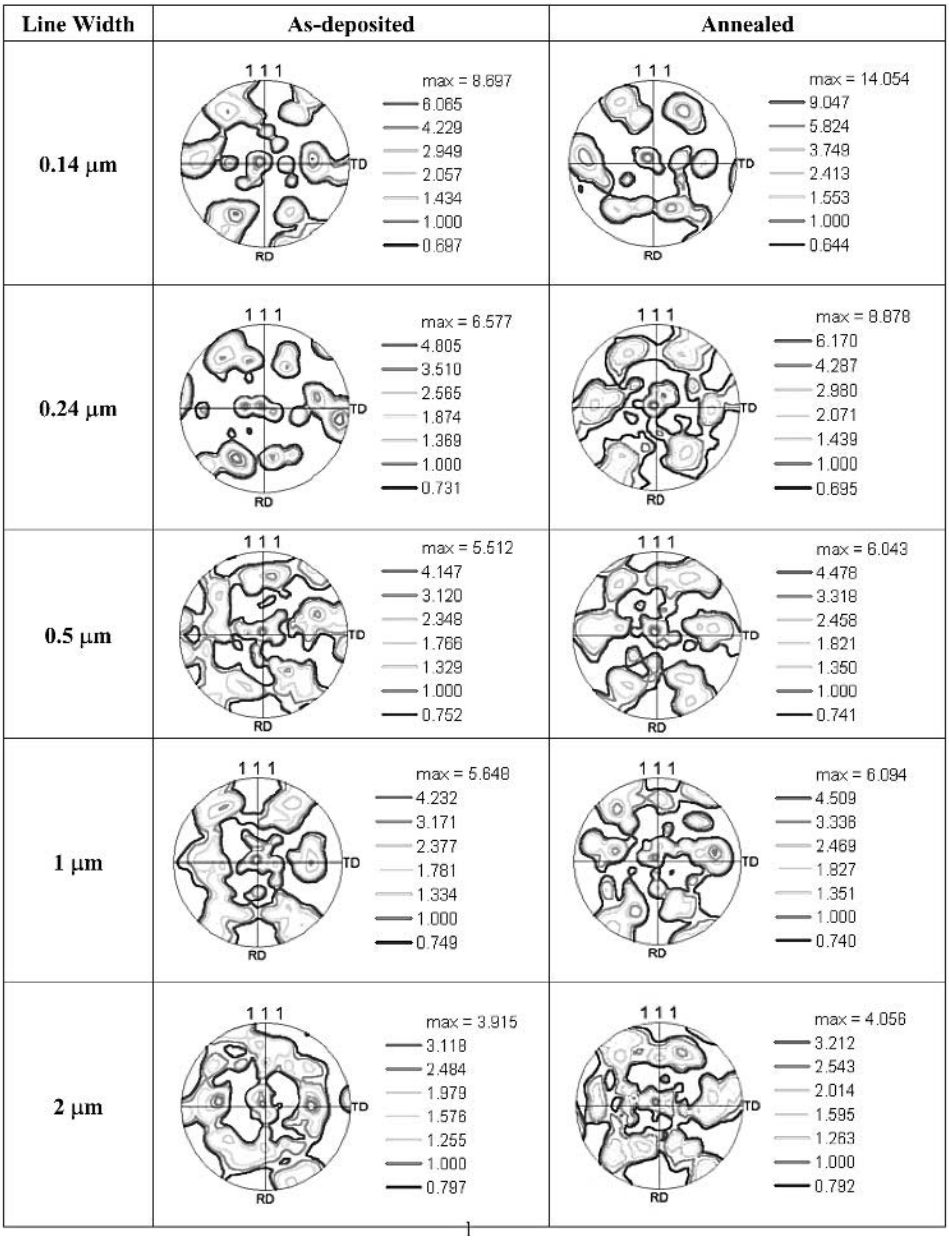


Fig. 4. {111} Pole figures of copper interconnects having a different line width: as-deposited and annealed samples.

texture of the annealed sample become larger after annealing. As shown in Fig. 5, maximum intensity is the strongest in the narrowest line and it decreases as the line width increases. The difference between the as-deposited and annealed sample in intensity is highest for the narrow lines and it decreases as the line width increases. In addition, a weak {111} sidewall component in the narrow lines, such as 0.14, 0.24, and 0.5 μm line width, is found as shown in Fig. 4. The intensity of the sidewall {111} component is plotted in Fig. 6. This figure shows that the strength of the sidewall {111} component changes as the line width increases. The strongest intensity is found at the narrowest lines, and it decreases when the line width increases up to 1 μm and then it increases up to the 2-μm line width in both specimens. The intensities of the as-deposited sample are always higher than the annealed sample. It seems that the annealing process minimizes the sidewall contribution to overall texture in Cu interconnects.

To analyze microstructural evolution after electropolishing, the orientation of grains and types of grain boundaries on the top area of the Cu interconnect is measured by EBSD technique, as shown in Fig. 7. These inverse pole figure maps demonstrate that the so-called bamboo structure is found in the 0.14-μm line and the semibamboo structure is observed in 0.24-μm and 0.5-μm line width samples. However, 1-μm and 2-μm lines show a polycrystalline microstructure with a mixture of large and small grains. Regardless of the difference in line width, every Cu interconnect that is investigated

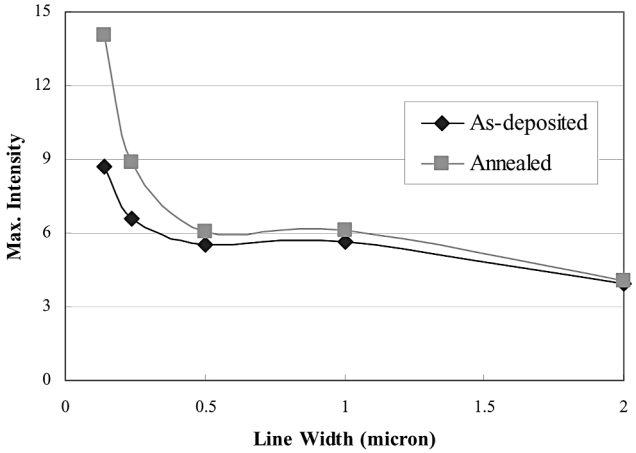


Fig. 5. Changes in maximum intensity of as-deposited and annealed samples as function of line width.

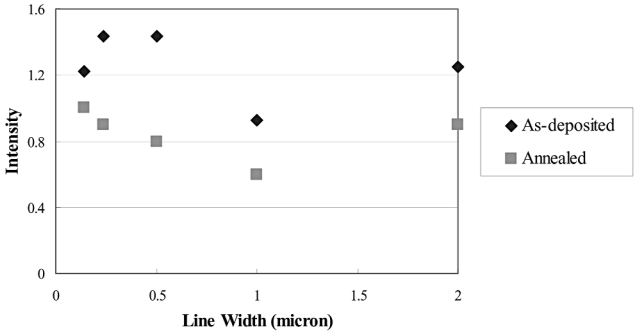


Fig. 6. Intensity of sidewall {111} texture component from transverse direction inverse pole figures of the as-deposited and annealed samples as a function of line width.

shows a large number of twin boundaries. After annealing, it seems that the microstructure of Cu interconnects contains less twin boundaries and the grains are larger. The frequency of CSL boundaries as measured by the EBSD technique is shown in Fig. 8. The results obtained demonstrate that the fraction of Σ3 boundaries increases as the line width increases. Also, a higher fraction of twin boundaries is observed in the 2-μm line. However, after annealing, this fraction decreases, especially in the 0.14-μm line width interconnect sample. From these results, it can be concluded that the annealing process enhances the grain growth of Cu interconnects consuming the twin boundaries. In addition, the grain growth in Cu interconnects after annealing supports the x-ray diffraction results, which show the directional development of the {115} texture.

Twin boundaries cannot be responsible for the textural and microstructural transformation, since they have a low mobility.[14] Therefore, it is possible that the stress or strain energy might be the most important factor for the textural and microstructural evolution during annealing. In order to examine the stress distribution in the trench and overburden area, FEM was used (Fig. 9). In this calculation, it is assumed that the finite-element mesh can expand freely along the normal direction (ND) when Cu

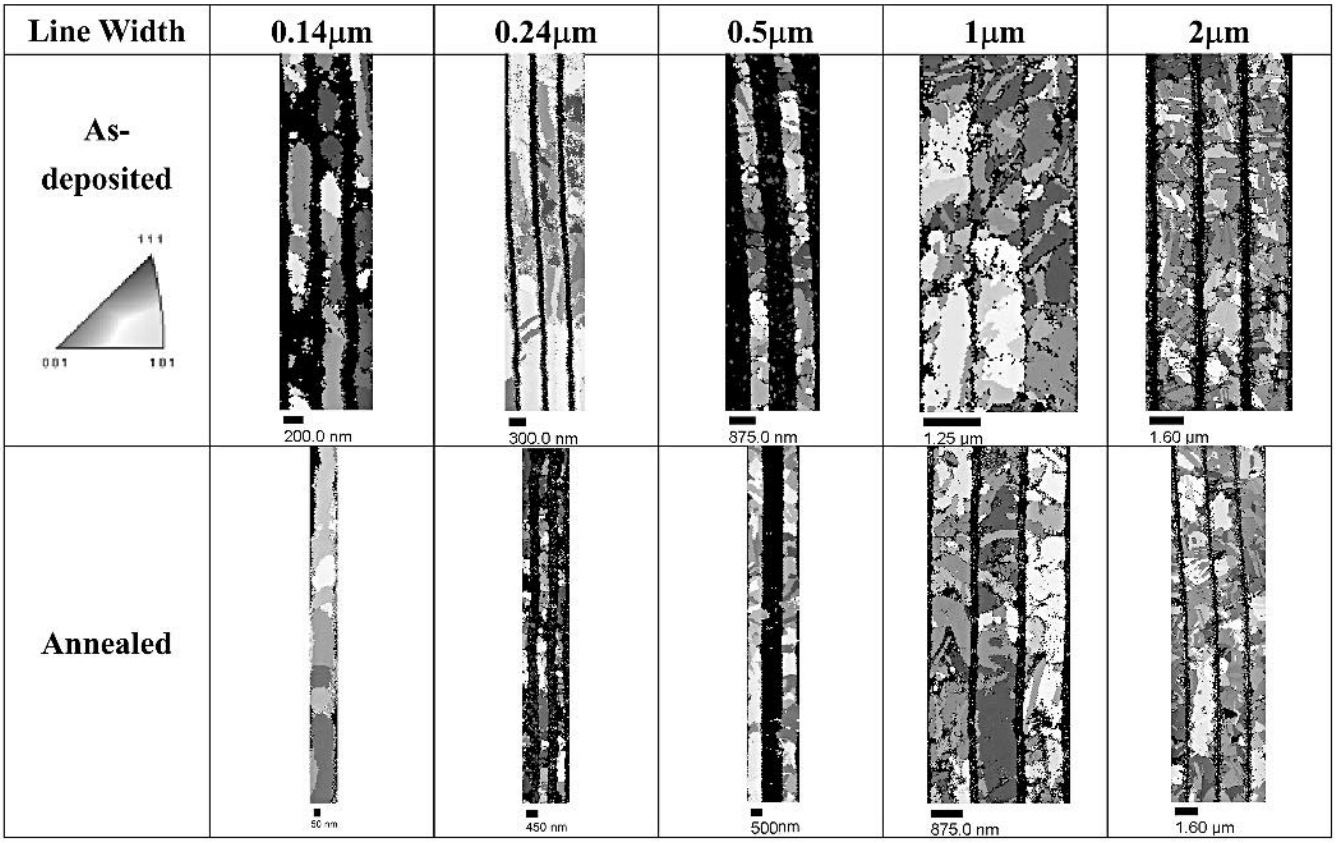


Fig. 7. OIM map representing orientation of planes parallel to the surface of the interconnect lines after electropolishing.

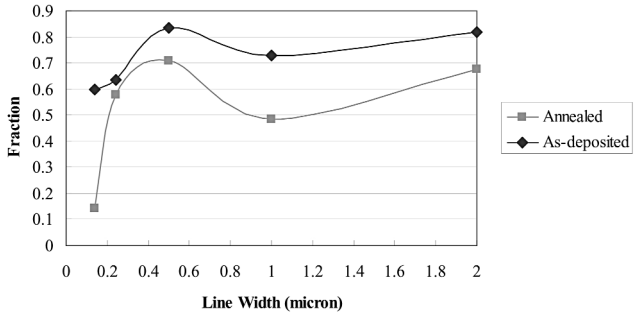


Fig. 8. Fraction of Σ3 CSL boundaries in Cu interconnects lines having a different line width after annealing.

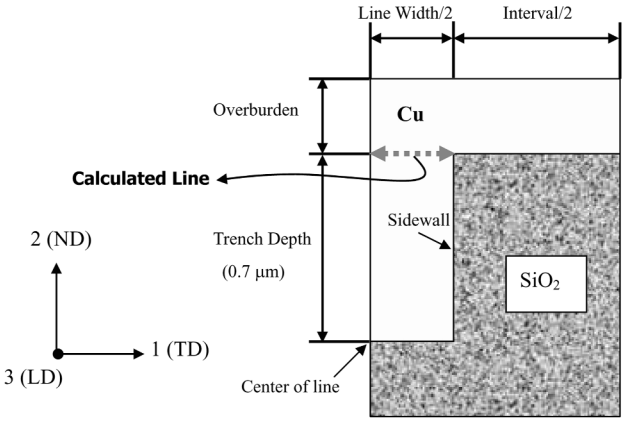


Fig. 9. Cross-sectional schematic diagram of Cu interconnects for calculation of stress distribution by FEM.

interconnect with overburden is annealed at 200°C. Since the mirror symmetry is applied along the ND and the line direction, only half of the Cu interconnect line was modeled in this investigation. To calculate the thermal stress (S_{11}) distribution in damascene copper with a different line width at 200°C, it is also assumed that the copper interconnect has isotropic mechanical properties and the expansion coefficients of surrounding silicon oxide are comparable to those of copper. Therefore, the data obtained from this modeling should only be considered as a qualitative representation of the stress changes at high temperature.

Figure 10 shows the stress distribution along width S_{11} from the center of the Cu line to the sidewall on the top surface area (Fig. 9) at 200°C. From the data in Fig. 10, one can see that the thermal stresses change across the line width and the location of the maximum value of S_{11} moves from the corner (sidewall) of the trench to the middle as the line width decreases. To characterize these stress distributions, the average stress is calculated and plotted in Fig. 11. This figure shows that the absolute magnitudes of the stresses along the trench width are the largest in the 0.14 and 2 μm line width and the smallest in 1 μm line width. From these results, it can be concluded that the stress distribution as well as the total amount of stress in each Cu interconnects line is important. Therefore, the stress state can be a reason for textural and microstructural transformation.

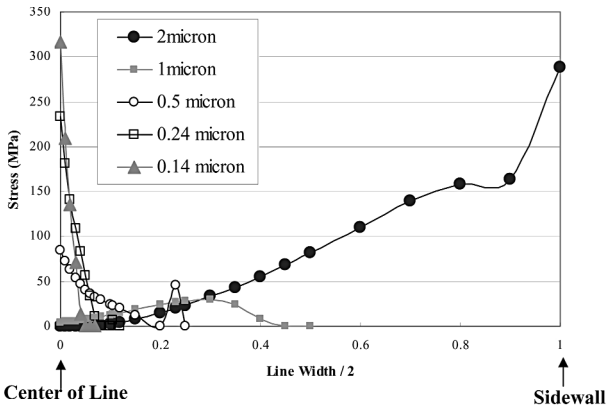


Fig. 10. S_{11} stress distribution from center of Cu line to sidewall on top surface area (Fig. 9) at 200°C.

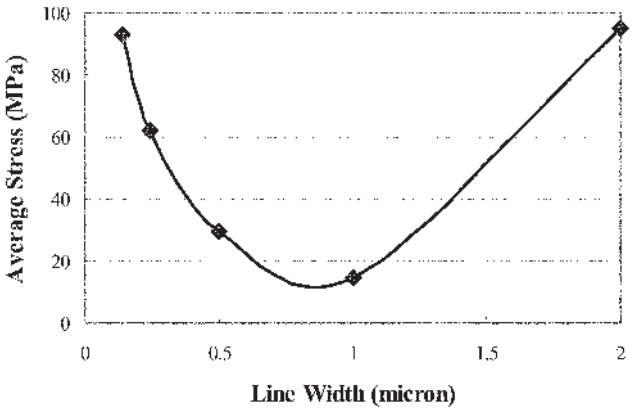


Fig. 11. Average S_{11} as a function of line width at 200°C.

DISCUSSION

In this investigation, two different kinds of samples were used: as-deposited and annealed at 200°C. Both samples are kept at room temperature for over 6 months, which is a sufficient amount of time for recrystallization to occur. Therefore, comparing both samples will permit the observation of the grain growth mechanism that takes place during the annealing process. In addition, to investigate the textural changes after annealing, two different characterization techniques are used: XRD and EBSD techniques. Using XRD, three different cross-sectional profiles of Cu interconnects are studied. The obtained XRD results demonstrate strong differences in the texture of the overburden area and inside the trench after electroplating and annealing (Fig. 2). The difference in texture of 120-sec and 130-sec electropolished samples indicates the constraint by the sidewalls, which generates stress during annealing and is an important factor for evolution of the texture. The constraints at a higher depth are larger than in the upper (surface) region since Cu can expand more freely along the ND. Therefore, it can be concluded that stress distribution along the trench depth is important in the textural and microstructural evolution as well as in determining the average stress.

The importance of stress on the evolution of texture in Cu damascene interconnects has been emphasized by several researchers since differences in the thermal expansion coefficients of copper and dielectric (silicon dioxide) generate stress in the interface area between different layers.[9–11] However, the mechanism of textural transformation imposed by stress in damascene copper interconnects remains unclear. Lee et al.[15–17] have suggested that the strain energy can be minimized when the absolute maximum principal stress direction is parallel to the direction of the minimum Young's modulus.[16,17] The minimum Young's modulus direction of copper is the <100> direction. However, the <100> orientations are not on the {111} plane. It is most probable that grains having <112> direction, which is on the {111} plane and is at the smallest angle with the <100> direction, will grow favorably.[18] Therefore, the texture is likely to approach the texture of the {111}<112>// trench width direction, which is the {111}<110>// trench length direction.

The average stress value at 200°C on the top surface of the trench shows the higher value at 0.14-μm and 2-μm line width. This result can be used to explain the driving force for the textural evolution after annealing, as shown in Figs. 5 and 6. In the narrow line, the stresses generated from the constraint of sidewalls and the difference in thermal expansion coefficients between layers help grains to align and grow in the {111}<110> orientation and decrease the sidewall {111} component. However, in spite of the high value of stress from the difference of the thermal expansion coefficient between layers, the intensity of {111} texture decreases since it has less of a constraint in the 2-μm line width and generates a high number of twin-type boundaries and a fiberlike texture component develops. Another important finding in this study is that the stress distribution along the trench width influences textural and microstructural evolution. Figure 10 indicates that the highest value of stress is found near the sidewall in the 2-μm line width. However, in the 0.14-μm line width, the highest value is found in the middle of the trench width. Therefore, both stress distributions along the trench depth and width are important in the textural and microstructural evolution since they can produce a different texture inside the trench. The difference between x-ray and EBSD results supports this explanation.

Another important factor that explains the textural and microstructural evolution in damascene Cu interconnects after annealing is the growth mechanism of the copper electrodeposits in the trenches. It has been reported in the literature that narrow Cu trenches can be completely filled during electroplating using a super-conformal filling.[18,19] To eliminate possibilities of void formation in the trench, this electroplating technique assures that the growth from the bottom of the trench is dominant over the growth from the sidewall,[19] as illustrated in Fig. 12. Several bodies of research[20–23] have reported that the importance of the sidewall {111} component is increased in the narrow lines and the intensity of the overall texture can be minimized. However, in super-conformal filling conditions where the bottom growth is much more dominant than the sidewall growth, such an observation is questionable. In our investigation, weak sidewall components were found on the top surface area of the as-deposited sample in the narrow line because the relative volume fraction of the sidewall versus the bottom increases as the line width decreases. However, it decreases after the annealing process. Therefore, it can be concluded that the contribution of the sidewall component is negligible and stress influences textural evolution during annealing.

CONCLUSIONS

Influence of stress distribution in the trench on textural and microstructural evolution of Cu damascene interconnects has been studied: the stress enhances the {111} <110> texture component and decreases the {111} sidewall components. The proposed model of texture evolution after annealing

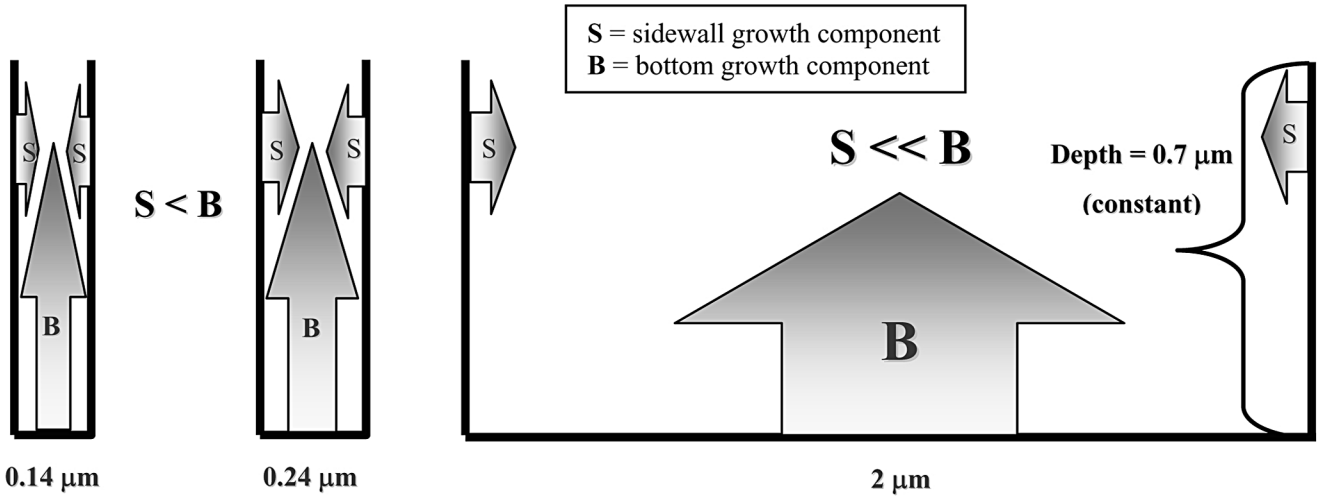


Fig. 12. Schematic illustration of texture evolution as line width decreases in copper trench according to condition of super-conformal filling.

assigns an important role to differences in the stress state, but also demonstrates that the texture of copper electrodeposits can be affected by the growth mechanism in the copper electrodeposits. However, the effect of the sidewall component on the overall texture of Cu interconnects is negligible if stress dominates the textural evolution during annealing. A bamboo-type structure was found in the 0.14-μm line width; however, the 2-μm line width Cu interconnects have a polycrystalline structure. The fraction of the Σ3 boundaries increases as the line width increases. However, it decreases after annealing because the Cu interconnects are dominated by grain growth.

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