Molecular Beam Epitaxy Grown Long Wavelength Infrared HgCdTe on Si Detector Performance

M. CARMODY,[1,4] J.G. PASKO,[1] D. EDWALL,[1] R. BAILEY,[1] J. ARIAS,[1] S. CABELLI, J. BAJAJ,[1] L.A. ALMEIDA,[2] J.H. DINAN,[2] M. GROENERT,[2] A.J. STOLTZ,[2] Y. CHEN,[3] G. BRILL,[3] and N.K. DHAR[3]

1.—Rockwell Scientific Company, Camarillo, CA 93012. 2.—U.S. Army RDECOM CERDEC NVESD, Ft Belvoir, VA 22060-5806. 3.—Army Research Laboratory, Adelphi, MD 20783-1197. 4.—E-mail: mcarmody@rwsc.com

The use of silicon as a substrate alternative to bulk CdZnTe for epitaxial growth of HgCdTe for infrared (IR) detector applications is attractive because of potential cost savings as a result of the large available sizes and the relatively low cost of silicon substrates. However, the potential benefits of silicon as a substrate have been difficult to realize because of the technical challenges of growing low defect density HgCdTe on silicon where the lattice mismatch is ~19%. This is especially true for LWIR HgCdTe detectors where the performance can be limited by the high ($\sim 5 \times 10^6$ cm^{-2}) dislocation density typically found in HgCdTe grown on silicon. We have fabricated a series of long wavelength infrared (LWIR) HgCdTe diodes and several LWIR focal plane arrays (FPAs) with HgCdTe grown on silicon substrates using MBE grown CdTe and CdSeTe buffer layers. The detector arrays were fabricated using Rockwell Scientific's planar diode architecture. The diode and FPA and results at 78 K will be discussed in terms of the high dislocation density ($\sim 5 \times 10^6$ cm^2) typically measured when HgCdTe is grown on silicon substrates.

Key words: HgCdTe, MBE, Si substrates

INTRODUCTION

The highest quality LWIR HgCdTe layers are grown by molecular beam epitaxy (MBE) on near-lattice-matched CdZnTe substrates. Rockwell Scientific has helped pioneer this epitaxial growth technology. However, the relatively high cost and size limitation of CdZnTe substrate wafers have prompted a search for a low-cost alternative substrate that is suitable for high-volume, large-format production.[1] Silicon wafers offer many advantages due to their low cost, large available sizes, high mechanical strength, industrial maturity, and ability to thermally match the read-out integration chip.[1–4] Several materials-related challenges have, thus far, prevented the realization of this potential. First, the lattice-parameter mismatch between Si and HgCdTe is ~19% (a_{Si} = 5.43 Å, a_{CdTe} = 6.48 Å, a_{HgTe} = 6.453 Å). Second, the thermal expansion coefficient (α) mismatch between Si and HgCdTe is significant ($\alpha_{Si} = 2.6 \times 10^{-6}$ K^{-1}, $\alpha_{CdTe} = 5.35 \times 10^{-6}$ K^{-1}). These thermal and lattice mismatch differences result in a high density of threading dislocations when HgCdTe is grown epitaxially on silicon substrates. Epitaxial layers of ZnTe, CdTe, and CdSeTe have been grown on Si wafers prior to growth of HgCdTe to buffer the interfacial strains that result from the lattice-parameter misfit between the epitaxial layer and the silicon substrate. Nevertheless, typical HgCdTe epitaxial layers grown by MBE at Rockwell Scientific on CdTe/Si have threading dislocation densities ~10^6–10^7 cm^{-2}. Fabrication of high-performance, long wavelength infrared (LWIR) detectors from epitaxial HgCdTe represents a significant technical challenge because diode dark currents can be dominated by material defects located in the metallurgical junction region of the diode. These defect-generated dark currents result in reduced R_oA products and "soft" reverse bias diode characteristics in the diode I-V curves. R_oA values for LWIR HgCdTe photodiodes begin to

(Received October 7, 2004; January 25, 2005)

decrease at temperatures below 78 K when dislocation densities are $>5 \times 10^5$ cm^{-2}.[5–7] The MWIR and SWIR layers with these high dislocation densities can be used for some applications where the detector is operated at relatively high temperatures (>77 K) because the mechanisms limiting diode performance are generally not controlled by the dislocation density. For LWIR and VLWIR applications, defect states in the narrow bandgap of the HgCdTe can help facilitate defect-assisted tunneling currents (particularly when detectors are operated at 40 K), resulting in higher dark currents and significantly reduced R_oA products, thus degrading the operability of focal plane arrays (FPAs).[5–7] Therefore, the technical challenge of using Si as a substrate alternative for LWIR and VLWIR HgCdTe growth is one of reducing the dislocation density, preferably to the mid-10^5 cm^{-2} level or below.

Here, we report the performance of LWIR (cutoff wavelength $\lambda_c \sim 10$ μm) diodes and FPAs fabricated on Si substrates at Rockwell Scientific. Silicon substrate wafers with ZnTe/CdTe buffer layers and CdSeTe buffer layers were provided by the Army Night Vision and Electronic Sensors Directorate (NVESD) and the Army Research Laboratory, respectively.

HgCdTe LAYER GROWTH AND CHARACTERIZATION

ZnTe/CdTe buffer layers were grown at NVESD on (211) Si wafers by molecular MBE. The details of the buffer layer growth process have been published previously.[5,6] ZnTe/CdSeTe buffer layers were fabricated at Army Research Laboratory using a DCA MBE system equipped with a 3.25-in. substrate heater. The details of the growth has been described elsewhere.[7,8]

The LWIR HgCdTe layers were deposited on these buffered Si wafers at Rockwell Scientific by MBE. The cutoff of each layer was controlled during MBE growth by in-situ spectroscopic ellipsometry measurements of the Cd composition of the $Hg_{1-x}Cd_xTe$ epitaxial layer. Real-time variations in the Cd composition during growth were used in a feedback loop to control the CdTe and Te source temperatures to maintain a uniform composition during epitaxial layer growth.[12] The composition and thickness of each grown HgCdTe layer were measured at room temperature using a Nicolet Fourier transform IR spectrometer. The nominal thickness of each HgCdTe layer as determined by the interference fringe spacing was ~10 μm. The HgCdTe layers were intentionally doped n-type with indium during MBE growth. The carrier concentration and mobility of each layer were measured at 77 K using the van der Pauw technique at a magnetic field of 2,000 Gauss. Void and microvoid defect densities were measured using optical microscopy techniques. The dislocation density of each HgCdTe layer was determined by counting the triangular etch pits revealed by immersing a small side piece of each layer in a dislocation-revealing etch solution.

Small samples from two representative HgCdTe layers were annealed for lifetime measurements. The samples were annealed in a Hg-saturated atmosphere. The details of the anneal process have been reported previously.[16] The anneal recipe was chosen to approximate conditions similar to those used during the diode formation process. The surface of each annealed lifetime sample was passivated using a thin CdTe layer. The minority carrier lifetime was measured using the photoconductive decay method.[13] Lifetime measurements were performed at multiple temperatures from 77 K to 200 K.

Rockwell Scientific's standard double-layer planar heterostructure (DLPH) architecture was adopted as the baseline architecture.[14] This consists of a HgCdTe absorber layer doped n-type with indium and a wider bandgap cap layer. The formation of the p-on-n junction diode is achieved by selective area ion implantation of arsenic through a photoresist window followed by high-temperature annealing for cap layer diffusion and carrier activation. The structure is passivated with a CdTe layer.

A performance evaluation chip (PEC) consisting of diodes with a variety of junction areas is fabricated on each layer to evaluate the layer quality and its suitability for FPA fabrication. Current-voltage (I-V) characteristics and zero bias impedance resistance products (R_oA) for various diode junction sizes were measured at 78 K for each PEC. The spectral response was measured using a modified Nicolet Fourier transform IR spectrometer. Quantum efficiency (QE) was measured with a calibrated blackbody source under both spot and flood illumination to extract the effective lateral optical collection length (L_o), which was used to determine the optical collection area A_o. The optical collection area A_o for each junction was used to calculate the R_oA, which shall be reported as R_oA_o.

MATERIAL CHARACTERISTICS

The material characteristics of the epitaxial HgCdTe on silicon layers selected for testing and device fabrication are summarized in Table I. The Cd composition range for the layers selected for device fabrication was $\sim x_{Cd} = 0.225$–0.235, which can be used to estimate the bandgap (Eg) and cutoff of each layer by the Hansen, Schmidt, and Casselman relation.[15] The predicted cutoff (λc) at 78 K for the layers listed in Table I is nominally centered about ~10.0 μm.

Figure 1 is a plot of the measured 78 K carrier concentration and mobility for recent LWIR HgCdTe layers grown on silicon substrates at Rockwell Scientific. The results highlight the reproducibility of the doping control and mobility for LWIR HgCdTe on silicon. The carrier concentration distribution was centered about $\sim 1 \times 10^{15}$ cm^{-3} with an average mobility of approximately 10^5 (cm^2/V·s). The minority carrier lifetime versus temperature for two LWIR HgCdTe on silicon layers is plotted in Fig. 2. The 78 K carrier lifetime for the two LWIR HgCdTe on

Table I. Characteristics of HgCdTe Layers from Two Wafer Lots That Were Processed to Give LWIR Diodes and FPAs

Layer	Structure ID	Buffer	× Active	Thickness (μm)	EPD ×1 × 10^5 cm^{-2}	n ×1 × 10^{15} cm^{-3}	μ × 1000 (cm2/V-s)
3-971	C1079	CdTe	0.233	~10	53	0.8	98.7
3-984	CST069	CdSeTe	0.236	~10	55	0.9	99.6
3-1016	C2108	CdTe	0.239	~10	62	1.1	79.9
3-1029	CT-088	CdTe	0.231	~10	47	0.8	105.0
3-1175	C3085	CdTe	0.232	~10	38	1.0	127.0
3-1083	C3046	CdTe	0.231	~10	46	1.1	109.0
3-1085	C3048	CdTe	0.231	~10	44	1.3	116.5

silicon samples is ~1−2·10^3 ns. Layer 3−1,016 has a CdTe buffer layer, and layer 3-984 has a ternary CdSeTe buffer layer. Both samples show comparable minority carrier lifetime over the temperature range used for the measurements. The solid line plotted in Fig. 2 is the theoretical lifetime curve assuming Auger and radiative recombination mechanisms, with no active SRH recombination and a layer composition and carrier concentration of x = 0.23 and n = 9 ×10^{14} cm^{-3}, respectively. The lifetime for the LWIR HgCdTe on silicon shows near theoretical lifetime values at 77 K and is comparable to the lifetime values reported for similar cutoff LWIR HgCdTe grown on bulk CdZnTe.[16]

DEVICE STRUCTURE AND PERFORMANCE CHARACTERISTICS

Diode I-V and R_oA Performance AT 78 K

A key performance parameter for any HgCdTe PV device is the R_oA product, or the zero bias impedance (R_o) junction area (A) product. The R_oA product versus cutoff wavelength measured at 78 K for multiple LWIR HgCdTe samples is plotted in Fig. 3. The junction area used for the R_oA product that is plotted in Fig. 3 is the optical area of the junction (A_o), which is corrected for carriers that are collected by the junction from a region beyond the junction implant edge and within a diffusion length of the metallurgical junction. The solid square data icons in Fig. 3 represent the R_oA_o product for HgCdTe grown on bulk CdZnTe substrates, and the open circle icons represent layers grown on silicon substrates. For

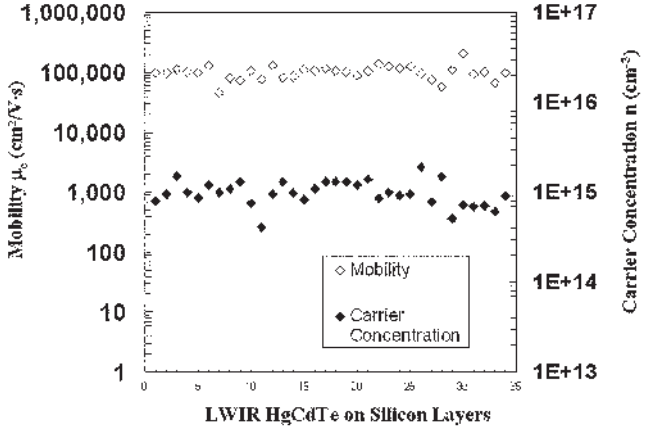

Fig. 1. Carrier concentration and mobility at 78 K for n-type LWIR HgCdTe grown on silicon substrates

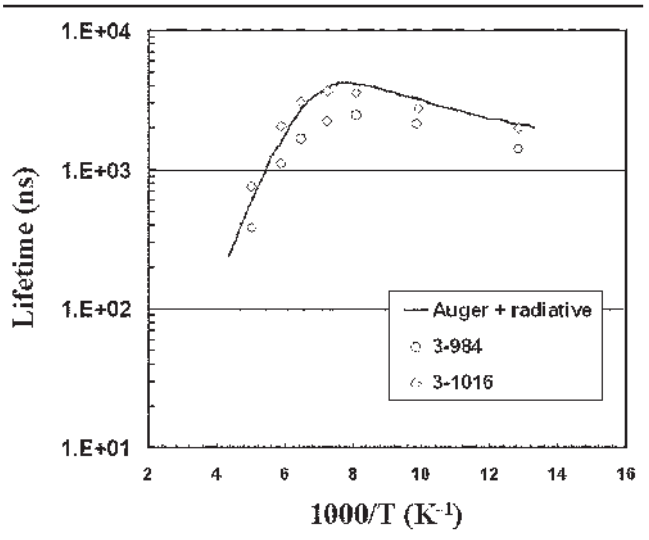

Fig. 2. LWIR HgCdTe on silicon minority carrier lifetime versus temperature. The solid line is a lifetime model that assumes only Auger + radiative recombination mechanisms and x = 0.23 and a carrier concentration (n) of n = 9 × 10^{14} cm^{-3}.

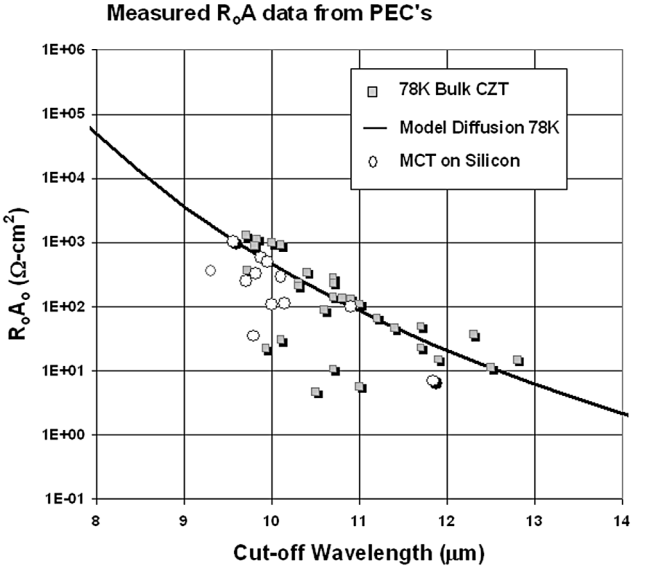

Fig. 3. Historical R_oA_o data at 78 K for LWIR HgCdTe grown on silicon and for LWIR HgCdTe grown on bulk CdZnTe.

layers grown on bulk CdZnTe, the R_oA_o product is equal to the 78 K diffusion line for the majority of devices. For the devices fabricated from HgCdTe on silicon, the R_oA_o product is diffusion limited for the best devices and approaches the HgCdTe/CdZnTe R_oA_o trend line. However, there are limited data with significant scatter for the 78 K LWIR HgCdTe layers grown on silicon.

The 78 K current-voltage response for various size diodes, measured on a single PEC from a representative LWIR HgCdTe on silicon layer, is shown in Fig. 4. The PEC chip contains device sizes (junction areas) of 8- and 16-μm-diameter circular diodes (8C and 16C) and 26-, 46-, 125-, and 250-μm square diodes. The diodes with the smallest junction area (8C and 16C) are diffusion limited beyond 150 mV of reverse bias, showing very little leakage currents or soft breakdown of the diode. As the junction area of the diode is increased, the reverse bias characteristics of the diode becomes increasingly soft, with the largest diodes (125 μm and 250 μm) starting to show significant leakage currents with less than 0.01 mV of reverse bias applied to the diode.

The device characteristics of LWIR HgCdTe on silicon diodes measured at 78 K are typical of diodes fabricated from high dislocation density LWIR HgCdTe. Dislocations threading through the junction region have been shown to reduce the R_0A product and increase the reverse bias leakage currents of LWIR HgCdTe devices. The variation in the reverse bias leakage currents observed for different diode areas is also consistent with high dislocation density LWIR HgCdTe.

Threading dislocations in LWIR HgCdTe have been modeled as a series of variable resistance leakage pathways that intersect the p-n junction.[7] The resistance of each leakage pathway (dislocation) is not believed to be a constant, and can vary between individual dislocations depending on many factors including the dislocation orientation, core structure, and any potential impurity atoms decorating the dislocation core. Consequently, not all dislocations are equal in their ability to act as conductive shorts across the diode junction. Therefore, not all dislocations are "active" in degrading diode performance. Relatively small diodes (8–12-μm junction diameter) that have a small number of dislocations threading through them may actually show performance comparable to HgCdTe layers with mid-10^4 cm^{-2} dislocation densities depending on the number of dislocations intersecting the junction. The idea is that for a given dislocation density, as the junction diameter increases, the junction begins to capture an increasingly greater number of dislocations (Fig. 5). For large junction area diodes, the number and density of dislocations captured by the diode are believed to be large enough to ensure leakage current in reverse bias even if a significant number of dislocations in the layer are essentially "nonactive" dislocations. However, for small area diodes (diode on the left in Fig. 5), the number of dislocations threading through the junction is sufficiently small that the occasional small diode may have zero dislocations or only a small number of relatively "nonactive" dislocations threading across it. The average dislocation density for LWIR HgCdTe on silicon is $\sim 5 \times 10^6$ cm^{-2}. The smallest diodes (8C) may have as few as 1–3 dislocations per diode, which may explain why the 8-μm and most of the 16-μm-diameter diodes in Fig. 4 have significantly better reverse bias characteristics compared with the larger diodes from the same layer with an identical dislocation density.

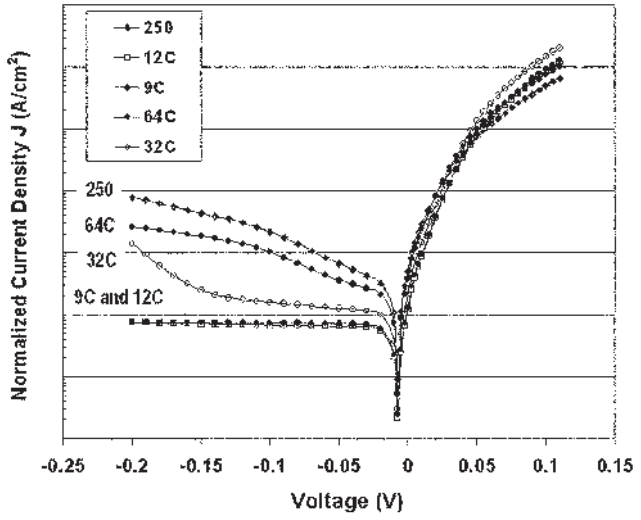

Fig. 4. 78 K current-voltage response for different junction area diodes fabricated from the same layer 3-1175.

FPA PERFORMANCE

Layers selected for FPA hybridization were screened at the PEC level for 78 K electrical and optical performance before proceeding onto FPA fabrication. The FPA format was 256 × 256 pixels, with each pixel consisting of a 28-μm implant on a 40-μm pitch. The FPAs were constructed by hybridizing to a TCM2001 direct injection readout integrated circuit chip using indium bump technology.

Diode Performance of FPA Layer

The PEC characteristics at 78 K for layer 3-1085 are shown in Fig. 6. The spectral response is comparable to that measured for LWIR HgCdTe on a CdZnTe substrate. The cutoff λ_c (defined as the point where the spectral response per watt dropped to 50% of its peak value) measured at 78 K was ~10.0 μm. The QE for these devices without antireflective coating was 54.8%. The I-V characteristics of the best small implant area diodes are diffusion limited near zero bias and show near ideal behavior out to 200 mV reverse bias. The poor performing small diodes and the majority of the larger area diodes show diffusion-limited behavior near zero bias but exhibit a soft reverse bias breakdown typical of LWIR material with a relatively high dislocation density. The R_oA_o values for the best diodes (small diameter 10-μm circular implant) approach 1,000 Ohm-cm^2 and are

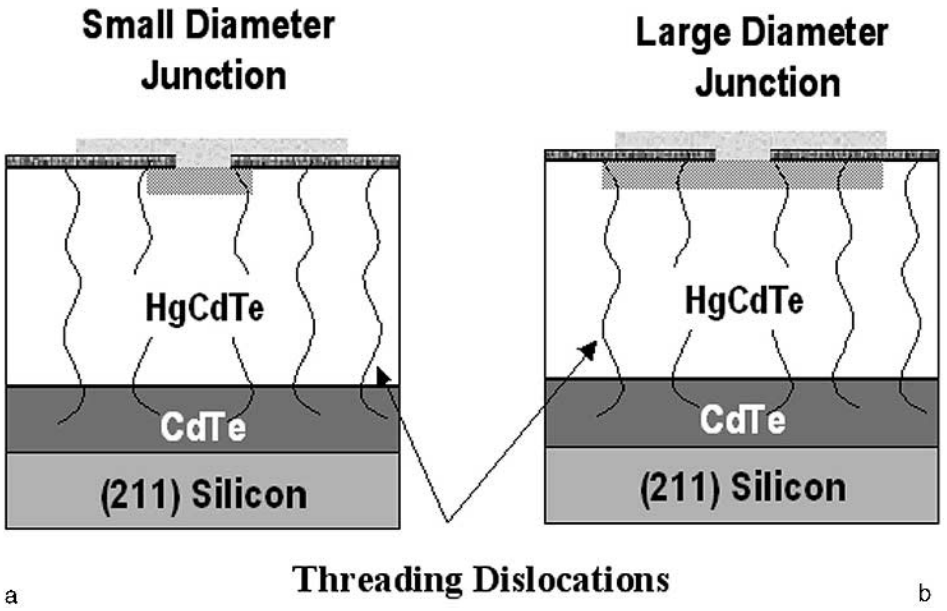

Fig. 5. Cartoon schematic of a high dislocation density HgCdTe sample with both small- and large-diameter p-n junctions. For a constant dislocation density, the small junction captures a very small number of dislocations resulting in diffusion-limited diodes in reverse bias.

comparable to LWIR diodes fabricated on bulk CdZn Te substrates. However, there is appre-ciable spread in the R_oA_o, with most of the larger area diodes centered at an average value of ~100 Ohm-cm^2.

FPA Measurements

Figure 7a shows the noise equivalent temperature difference (NEDT) distribution for an FPA fabricated from layer 3-1085. The FPA was operated at 78 K with a 0.32-ms integration time. A 300 K blackbody source illuminated the FPA through an f/2.8 cold aperture and 7.5–10-μm cold filter. Mean dark current per pixel, measured with the cold shutter closed, was 5.9×10^9 e-/sec, a value approximately 6 times lower than the photocurrent of the NEDT measurement. The magnitude and bias dependence of the dark current are consistent with the R_oA_o values and soft I-V characteristics reported above. The median NEDT of 28 mK exceeds the 16 mK photon noise limit. Possible causes of the excess noise and the high noise tail of the Fig. 7 histogram are 1/f noise associated with the dark current and noise on the ROIC bias lines that determine the detector reverse bias operating point. The percentage of pixels with noise less than twice the median is 92.3%. Dark pixels in the gray-scale map of Fig. 7b show the location of noisy detectors.

The single data frames produced by this FPA operated at 80 K in an IR camera with f/2 optics and a 52 Hz frame rate are shown in Fig. 8. Signals from defective pixels in the image in Fig. 8 are replaced by the average of their neighbors.

The NEDT histogram in Fig. 7 illustrates the technical challenge that remains before silicon can

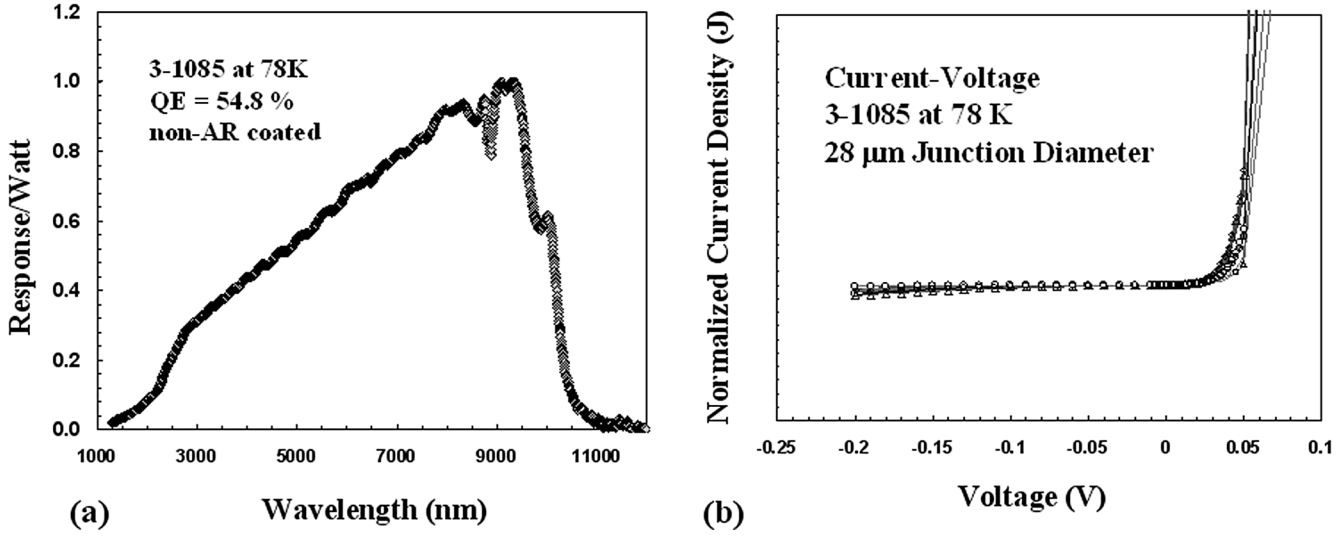

Fig. 6. (a) Spectral response and (b) normalized IV plot at 78 K from layer 3-1085.

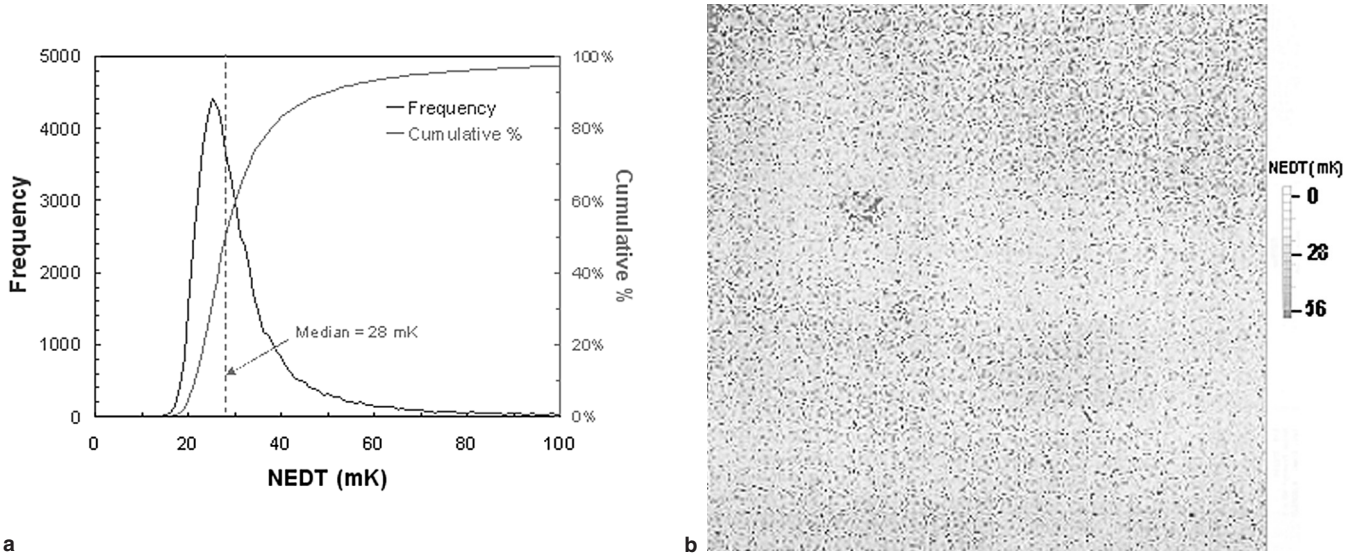

Fig. 7. (a) NEDT frequency distribution and (b) pixel map of a FPA from layer 3-1085.

be used as substrate replacement for CdZnTe. The peak value of the FPA NEDT histogram located near 20 mK represents the group of relatively high performing diodes. The broad tail that extends out to higher values represents the group of poor performing pixels, and the key technical challenge. The NEDT can be written as

$$\mathrm{NEDT} = \frac{i_n \sqrt{\dfrac{1}{2\tau_{int}}}}{A_j \dfrac{\partial J_p}{\partial T_{back}}} \tag{1}$$

where i_n is the detector noise current, τ_{int} is the signal integration time, J_p is the photocurrent density and T_{back} is the temperature of the background. The NEDT is comprised of both a diode dark current term (i_n is calculated from the detector R_0A) and the detector QE term (photocurrent density is proportional to the QE). Thus, both low dark current and high quantum efficiency are required to improve the detector NEDT.

It has been noted that the R_0A versus junction area decreases as the junction area increases. The same trend was noted for reverse bias dark currents in Fig. 4 and was explained in terms of larger diodes capturing a greater number of dislocations. Therefore, for LWIR HgCdTe on silicon, with a relatively high dislocation density, the smallest possible junction diameter should be used to maximize the R_0A. However, as the junction diameter is decreased to improve the detector R_0A, it is possible that the QE will suffer a simultaneous reduction. This decrease in detector QE is illustrated in Fig. 9. For a large junction diameter (the example in Fig. 9a is 25 μm) on a 40-μm pitch, a modest diffusion length of ~10 μm allows for the collection of carriers generated from the entire pixel area. When the junction diameter is decreased to 10 μm (as shown in Fig. 9(b)) to improve the junction R_0A, carriers generated near the pixel edge are now greater than a diffusion length away from the junction and will not be collected by the diode. This results in the reduction of the detector QE. Therefore, the junction diameter cannot be reduced arbitrarily to improve the junction R_0A without considering the junction diffusion length and the possible degradation of the detector QE.

The diffusion length L_D of a diode is proportional to the minority carrier lifetime (τ):

$$L_D \propto \sqrt{D\tau} \tag{2}$$

where D is the minority carrier diffusivity. Dislocations within the HgCdTe can act as carrier recom-

Fig. 8. Image produced by FPA from layer 3-1085 operated in an IR camera with f/2 optics and 52 Hz frame rate.

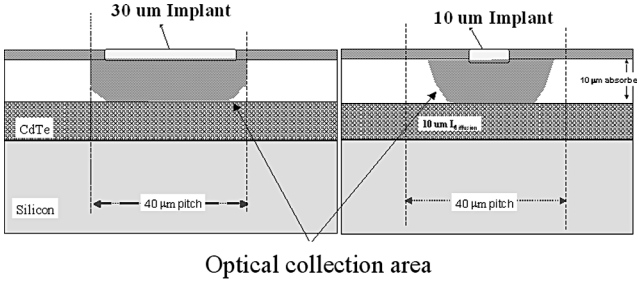

Fig. 9. Schematic of a (a) 25-µm junction and (b) 10-µm junction, both on a 40-µm pixel pitch.

bination centers and reduce the effective carrier lifetime. The dislocation density of HgCdTe grown on silicon substrates is significantly greater ($\sim 5 \times 10^6$ cm^{-2}) than the dislocation density of HgCdTe grown on bulk CdZnTe ($\sim 5 \times 10^4$ cm^{-2}). Therefore, a reasonable assumption is that the diffusion length observed when HgCdTe is grown on silicon should be less than is typically observed for HgCdTe grown on bulk CdZnTe, assuming the same carrier concentration. This trend of lower carrier diffusion lengths for HgCdTe on silicon has been observed experimentally; however, it should be noted that the minority carrier lifetime reported in Fig. 2 is comparable to that measured for HgCdTe on bulk CdZnTe and is not consistent with a suppressed carrier diffusion length. This supports the notion that not all dislocations are active, and that therefore large variations in the reported R_0A, carrier diffusion length, and carrier lifetime data may exist for different samples with comparable dislocation densities.

SUMMARY

Silicon wafers have the potential to be used as an alternative to CdZnTe wafers for large-format, low-cost FPAs. At 77 K, the best R_0A and QE values for diodes fabricated in MBE LWIR HgCdTe on Si and on CdZnTe are found to be comparable. These results are promising for FPAs for high background tactical applications where higher operating temperatures are acceptable. The initial FPA results are promising and indicate that the key to reducing the tail of poor performing pixels in the NEDT distribution is to reduce the density of dislocations that thread through the active junction area to reduce the detector dark current.

REFERENCES

1. N.K. Dhar, P.R. Boyd, P.M. Armirtharaj, J.H. Dinan, and J.D. Benson, *Proc. SPIE* 2228, 44 (1994).
2. P.S. Wijewarnasuriya et al., *J. Electron. Mater.* 27, 546 (1998).
3. N.K. Dhar, M.Zandian, J.G. Pasko, J.M. Arias, and J.H. Dinan, *Appl. Phys Lett.* 70, 1730 (1997).
4. T.J. De Lyon, D. Rajavel, S.M. Johnson, and C.A. Cockrum, *Appl. Phys Lett.* 66, 2119 (1995).
5. K. Jowikowski and A. Rogalski, *J. Electron. Mater.* 29, 736 (2000).
6. R.S. List, *J. Electron. Mater.* 22, 1017 (1993).
7. S.M. Johnson, D.R. Rhiger, J.P. Rosenbeck, J.M. Peterson, S.M. Taylor, and M.E. Boyd, *J. Vac. Sci. Technol. B* 10, 1499 (1992).
8. N.K. Dhar, P.R. Boyd, M. Martinka, J.H. Dinan, L.A. Almeida, and N. Goldsman, *J. Electron. Mater.* 29, 748 (2000).
9. P.J. Taylor, W.A. Jesser, M. Martinka, K.M. Singley, J.H. Dinan, R.T. Lareau, M.C. Wood, and W.W. Clark III, *J. Vac. Sci. Technol. A* 17, 1153 (1999).
10. N.K. Dhar, C.E.C. Wood, A. Gray, H.Y. Wei, L. Salamanca-Riba, and J.H. Dinan, *J. Vac. Sci. Technol. B* 14, 2366 (1996).
11. Y.P. Chen, G. Brill, and N. K. Dhar, *J. Cryst. Growth,* 252, 270 (2003).
12. D. Edwall, J. Phillips, D. Lee, and J. Arias, *J. Electron. Mater.* 30, 643 (2001).
13. R. Zucca, D.D. Edwall, J.S. Chen, and S.L. Johnston, *J. Vac. Sci. Technol. B* 9, 1823 (1991).
14. J. Bajaj, J.M. Arias, M. Zandian, D.D. Edwall, J.G. Pasko, L.O. Bubulac, and L.J. Kozlowski, *J. Electron. Mater.* 25, 1394 (1996).
15. G.L. Hansen, J.L. Schmit, and T.N. Casselman, *J. Appl. Phys.* 53, 7099 (1982).
16. D.D. Edwall, R.E. Dewames, W.V. McLeviage, J.G. Pasko, and J.M. Arias, *J. Electron. Mater.* 27, 698 (1998).