Monolithically Integrated HgCdTe Focal Plane Arrays

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The cost and performance of hybrid HgCdTe infrared (IR) focal plane arrays are constrained by the necessity of fabricating the detector arrays on a CdZnTe substrate. These substrates are expensive, fragile, available only in small rectangular formats, and are not a good thermal expansion match to the silicon readout integrated circuit. We discuss in this paper an IR sensor technology based on monolithically integrated IR focal plane arrays that could replace the conventional hybrid focal plane array technology. We have investigated the critical issues related to the growth of HgCdTe on Si read-out integrated circuits and the fabrication of monolithic focal plane arrays: (1) the design of Si readout integrated circuits and focal plane array layouts; (2) the low-temperature cleaning of Si(001) wafers; (3) the growth of CdTe and HgCdTe layers on readout integrated circuits; (4) diode creation, delineation, electrical, and interconnection; and (4) demonstration of high yield photovoltaic operation without limitation from earlier preprocessing such as substrate cleaning, molecular beam epitaxy (MBE) growth, and device fabrication. Crystallographic, optical, and electrical properties of the grown layers will be presented. Electrical properties for diodes fabricated on misoriented Si and readout integrated circuit (ROIC) substrates will be discussed. The fabrication of arrays with demonstrated I-V properties show that monolithic integration of HgCdTe-based IR focal plane arrays on Si read-out integrated circuits is feasible and could be implemented in the third generation of IR systems.

Key words: HgCdTe, monolithic, molecular beam epitaxy (MBE), CdTe/Si, Fourier transform infrared (FTIR), Hall, lifetime, reflection high-energy electron diffraction (RHEED), R_0A, readout integrated circuit (ROIC)

INTRODUCTION

The current baseline for infrared focal plane arrays (IRFPAs) is a hybrid technology wherein the HgCdTe detector array and the Si readout integrated circuit (ROIC) chips are fabricated separately and connected element by element with indium.[1,2] The size of these hybrid arrays and the number of pixels is limited by the following.

- The size of commercially available $Cd_{1-x}Zn_xTe$ wafers, which are currently the substrates of choice for HgCdTe epitaxial growth.
- The large thermal expansion mismatch between HgCdTe/CdTe and the Si readouts (thermal coefficients: 4.8×10^{-6} K^{-1} and 2.3×10^{-6} K^{-1}, respectively), which misalign the detector and ROIC arrays during heating and cooling cycles.

An alternative to the current technology would be the substitution of CdZnTe/Si composite substrates for the conventional CdZnTe substrates. This alternative is quite attractive for the following reasons.

- The Si substrates are available in very large areas (up to 12 in. in diameter), with high crystalline quality (they are very inexpensive and extremely robust).

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- The Si is transparent in the IR region of the spectrum. Therefore, backside illumination is possible.

CdTe/Si composite substrates are currently a real alternative to bulk substrates because of the impressive progress that has been achieved in the past ten years,[3–6] based on the innovative work pursued initially at the University of Illinois at Chicago.[7] Single-domain and twin-free 3-in.-diameter CdTe (211)B/Si(211) and CdTe(111)B/Si(001) layers, exhibiting double-crystal rocking curve, full-width at half-maximum (FWHM) of less than 100 arcsec, and etch pit densities (EPD) in the mid-10^5 cm^{-2}, are now routinely grown.[3] HgCdTe on CdTe/Si composite substrates have already been investigated and demonstrated.[3–6] Hybrid IRFPAs based on molecular beam epitaxy (MBE) grown HgCdTe/CdTe/Si of 640×480 and 1024×1024 staring format have been fabricated and thermal imaging has been demonstrated.[6] This finding has validated this approach to large format IRFPAs. However, even these Si-based IRFPAs have some of the drawbacks of conventional hybrids, namely, that detector and read out arrays assembled using a bump technology require extensive packaging efforts, are susceptible to vibration failures, and are plagued by parasitic capacitances and inductances that degrade their sensitivity and high frequency bandwidth.

A technology for which HgCdTe detector arrays are monolithically integrated with Si ROICs would obviate these deficiencies and appears to be the most advanced technology for high performance and very large IRFPAs.[8,9] Such a system provides the following advantages:

- elimination of the complex and low yield hybridization process;
- elimination of problems related to thermal mismatchs, which leads to FPAs with longer thermal stability and the possibility of very large formats;
- creation of compact systems with less heat load; and
- reduction of costs by increasing yield.

Although the existence of a mature MBE growth technology for CdTe/Si composite substrate and HgCdTe/CdTe/Si has paved the way for such a monolithic approach, the realization of a full monolithic structure requires a dedicated ROIC substrate for CdTe and HgCdTe growth. Some of the major challenges are listed as follows.

- The design of an ROIC suitable for the fabrication of the IRFPAs.
- The epitaxial growth on Si ROICs requires a low temperature, an appropriate selection of the Si ROIC wafer orientation, the control of the growth of CdTe on Si, the achievement of n-type and p-type doping of HgCdTe, the prevention of deposit formation on the ROIC area using selective epitaxy or the removal of deposits using selective etching or other means, and the establishment of reliable interconnects between the IRFPA and the ROIC.
- Another critical issue concerns the highest temperature acceptable during the entire process, including Si substrate preparation, growth, and device processing and integration. The temperature should never exceed 500°C for a conventional Si ROIC.
- The area of a unit cell in a two-dimensional monolithic array is limited by both the area of the active element and that of the adjacent electronics. This may considerably reduce the fill factor when compared with the hybrid approach. A possible solution to this problem involves the use of the lateral overgrowth approach in which the active elements are grown directly over the ROIC electronic element. Lateral overgrowth was successfully achieved in the past in LPE HgCdTe/CdTe/GaAs[8] and in MBE CdTe/Si[10]

In this paper, we address many of the issues related to the monolithic integration of HgCdTe/Si with Si ROICs. We successfully developed a monolithic array based on a HgCdTe/CdTe/Si ROIC. This paper describes the development of this technology and presents a comparison with the work of other groups.

ROIC AND LAYOUT DESIGN

Commercially available ROICs have no growth area for HgCdTe. We worked with Indigo Systems (Goleta, CA) to modify its standard ISC9802 ROIC[11] in order to meet the requirements for the direct growth of HgCdTe/CdTe on the circuit and for monolithic detector fabrication and interconnects. The new ROIC ISC98022 is electrically equivalent to ISC9802 but has a modified layout for the detector interface. ISC98022 is a 512-channel linear ROIC implemented as pairs of dies with 256 channels each and has on-ROIC signal processing capabilities: auto-zero input circuit and skimming (offset). It also has a wide range of integration capacitance selections (eight octave steps) and has the postoffset gain selectable over four settings. ISC98022 can operate in Integrate While Read and Integrate Then Read modes with selectable bandwidths for optimal noise performance. It has selectable 128/256/512 element multiplexing, high-speed analog output, and extensive built-in-test capabilities.

The device layout of the customized ROIC is shown in Fig. 1. Here, a window of about 14.4 mm $\times$ 0.68 mm is provided, which is covered with SiO_2 at the end of the ROIC fabrication. After selectively removing the SiO_2 layer by wet chemical etching, a buffer CdTe layer followed by the HgCdTe heterostructure is grown by MBE. Planar junctions are fabricated by arsenic ion implantation followed by activation annealing.

The cross section of a single device is shown in Fig. 2. Subsequent to the fabrication of the junctions, monolithic interconnects between the detector

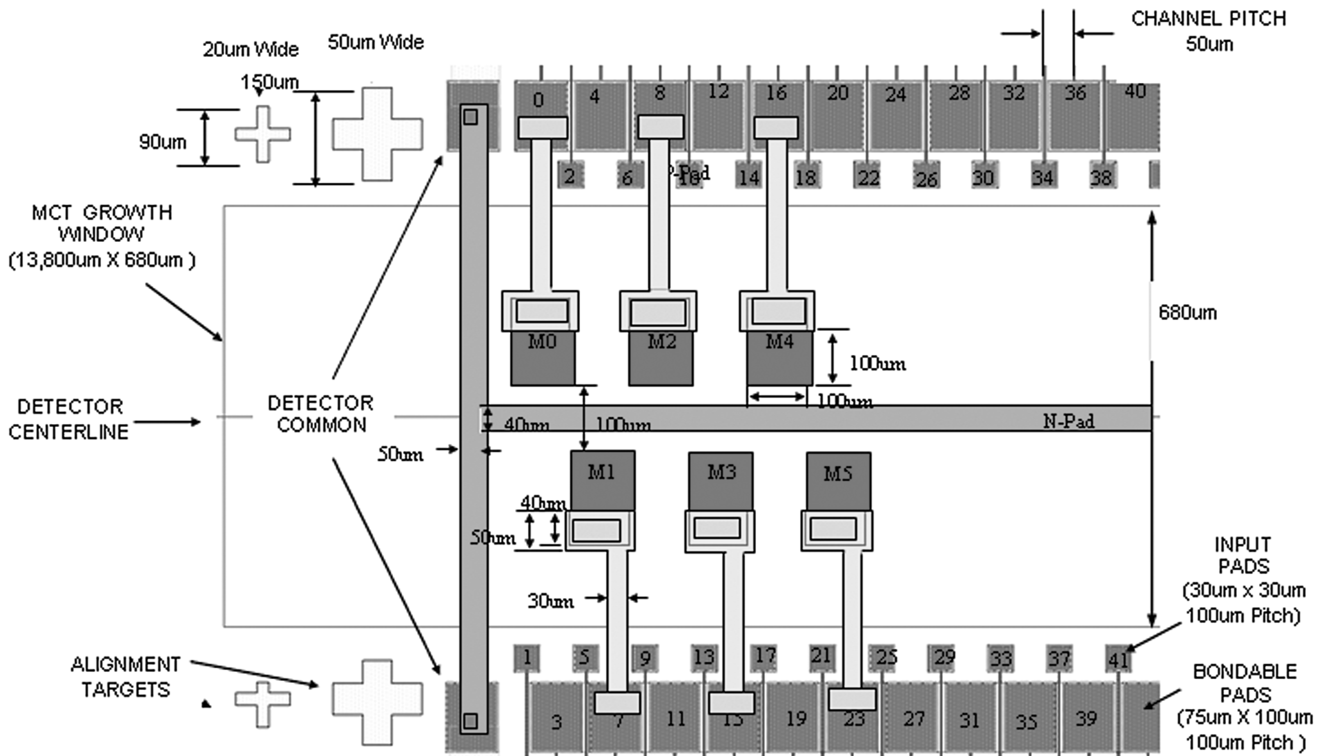


Fig. 1. Monolithic HgCdTe PV device layout (128 array pixels: 64 on odd input pads, and 64 on even input pads).

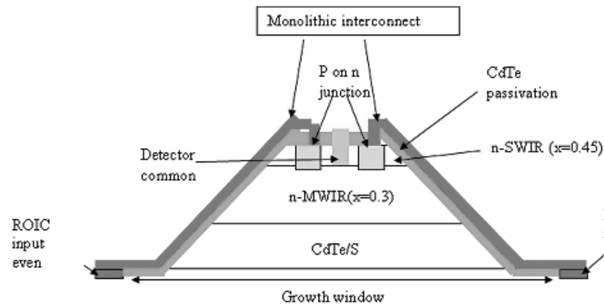


Fig. 2. Cross-sectional view of a single-color monolithic device.

outputs and the multiplexer inputs were established. The alternate mux input pads are designed to accommodate wire bonding for intermediate testing, if necessary. Various test patterns were added on the mask set in order to test and evaluate the material properties of HgCdTe layers and the fabricated devices. Note that standard ROICs are fabricated on (001)-oriented silicon substrates. We have earlier established a key orientation requirement for the successful growth of HgCdTe on silicon by MBE: an approximately 1° tilt from the (001) direction is a critical requirement to achieve twin-free, high-quality HgCdTe growth.[12] Hence, the ROICs were fabricated on such misoriented substrates.

CDTE BUFFER AND HgCdTe GROWTH

The most critical issues for growing CdTe and HgCdTe on ROICs are associated with the highest temperature acceptable during the entire processing sequence. The sequence includes Si substrate preparation, which involves chemical processing. A custom preparation and growth procedure was implemented to accommodate ROIC processing constraints.

ROIC Preparation

The Si ROICs cannot be cleaned with our standard RCA[13] process followed by hydrogen passivation since this would give rise to a chemical reaction between the metal pads of the ROIC and the HCl solution used in the RCA process. Although excellent results for CdTe/Si have been achieved using a combination of the RCA cleaning process and hydrogen passivation, we had to seek an alternate way to clean the Si ROIC.

The Si cleaning using an ozone oven has been successfully applied to Si(211) substrates in the past.[14] In this process, UV/Ozone oven cleaning followed by an HF/ARA etching creates an air-stable hydrogen-passivated Si(211) surface, which can be thermally cleaned at a temperature of about 600°C. We modified our standard cleaning process that includes hydrogen passivation developed for Si(001) wafers by replacing the RCA portion with UV/Ozone oven cleaning. The cleaning steps are as follows.

- Preheat UV/Ozone oven for 10 minutes and gently heat Si(001) wafer on a hot plate.
- Place Si (001) wafer on the wafer holder inside the oven for 10 minutes with rotation.
- Remove the wafer from the oven and etch in 2.5% HF solution for 1 min.
- Etch in 40% NH_4F for 30 sec.
- Rinse in de-ionized water for 2 sec.
- Blow dry with nitrogen or spin dry and load into chamber immediately.

CdTe Deposition on ROIC

CdTe was deposited on a 29.2 × 32.1 mm^2 Si(001) ROIC misoriented wafer in a DCA MBE system. Prior to CdTe deposition, the Si wafer was heated to about 480°C to desorb hydrogen from the Si(001) surface followed by cooling under As and CdTe fluxes to establish a Te or Te/As terminated surface that leads to CdTe(111)B growth. Figure 3 shows sequential reflection high-energy electron diffraction (RHEED) images of a Si(001) substrate and CdTe layer taken during different growth stages. The RHEED patterns show that a clean Si(001) surface can be obtained at temperatures around 480°C. The ROIC specifications indicate that such temperatures can be sustained without deterioration of the circuits. Although the growth temperature could be further optimized, the present growth seems to produce very encouraging results. A clear $(2\sqrt{3} \times 2\sqrt{3})$R30 surface reconstruction pattern and the presence of a second Laue zone at the end of the growth show that the CdTe(111)B layer is single domain and has good quality. The success of the growth of CdTe using this procedure cleared a critical hurdle for the growth of CdTe on Si ROIC, namely, the cleaning of the Si ROIC both chemically and thermally.

HgCdTe Growth on CdTe/ROIC

HgCdTe growth on CdTe/Si ROIC was carried out in a Riber 32P MBE system (Rueil–Malmaison, France). The structure of the HgCdTe grown on CdTe/Si ROIC consisted of an approximately 6-μm-thick midwavelength IR layer followed by an approximately 1-μm short-wavelength IR top layer and a ~1,000 Å CdTe cap layer. Both HgCdTe layers were in situ n-type doped with indium. The as-grown CdTe/ROIC chips were unloaded into a sealed container for rapid transportation into the HgCdTe growth chamber, though there exists some chance for contamination. Before being loaded into the Riber 32P MBE chamber, the CdTe/ROIC chips underwent a brief cleaning procedure. They were rinsed in methanol and etched for 2 sec in 0.1% bromine-methanol solution, which leads to a Te-terminated surface due to different etching rates of Cd and Te, preventing further substrate contamination. Finally, the substrates were dried with nitrogen and then loaded into the Riber 32P MBE machine. The excess Te on the CdTe/Si ROIC was later thermally removed in vacuum.

During the growth of CdTe on Si ROIC, we employ a blanket growth method that leads to the complete coverage of CdTe on the Si ROIC. Since the majority of the ROIC's surface area is covered by oxide and metal, growth of CdTe on these areas resulted in polycrystalline CdTe. Single-crystal CdTe was grown only on the narrow strip that had been opened for CdTe growth. For the same reasons, it is expected that single-crystal HgCdTe can only be grown on top of a single-crystal CdTe strip.

The deposition of HgCdTe results in significant changes in thermal absorption coefficients and surface emissivity when the substrate is mounted on an In-free block. The changes will, in turn, alter the surface temperature of the substrate. In order to compensate for this, we must modify the substrate temperature set point by employing an empirical ramping sequence during the first hour of HgCdTe growth on CdTe/Si. Since the direction and amount of ramping depend on the growth rate and composition of the HgCdTe layer, it is difficult to obtain an optimized growth procedure. Moreover, Si ROICs are 90% covered by oxide and metals, which makes the thermal dynamics of the substrate surface much more complicated after HgCdTe deposition. In order to bypass these difficulties, we used a graphite plate on the back of the Si substrates in the case of HgCdTe growth on ROIC. This almost completely eliminates the transient period after HgCdTe nucleation.

We used RHEED to monitor and establish the proper conditions during the growth and nucleation of HgCdTe material. However, we could only obtain RHEED patterns when the electron beam was focused on the narrow growth strip. For this reason, it was difficult to obtain a symmetric pattern. Growth was initiated at 160°C, which is the optimized growth temperature for HgCdTe on 32.1 × 29.2 mm^2 plain CdTe/Si substrates. However, immediately after HgCdTe nucleation, an additional spot was present along with the RHEED streaks, which indicated that nucleation of HgCdTe on CdTe/Si ROIC was in the low-temperature regime. The growth was

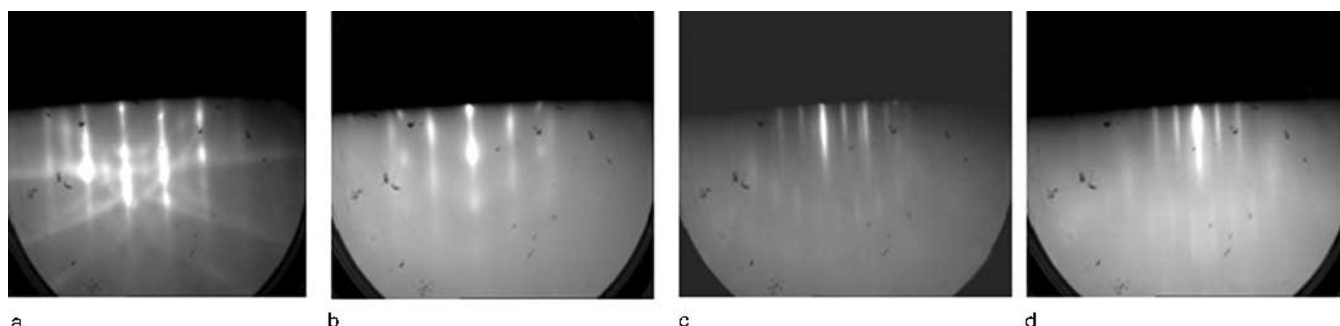


Fig. 3. RHEED images of a Si(001) substrate and CdTe layer taken during different growth stages: (a) clean Si(001) surface after As and CdTe exposure at 210°C; (b) CdTe(111)B deposited at 210°C for 2 min: double domain; (c) CdTe(111)B cooled to 360°C with Te flux showing second Laue zone and $(2\sqrt{3} \times 2\sqrt{3})$R30 pattern; and (d) CdTe(111)B at the end of growth with Te flux.

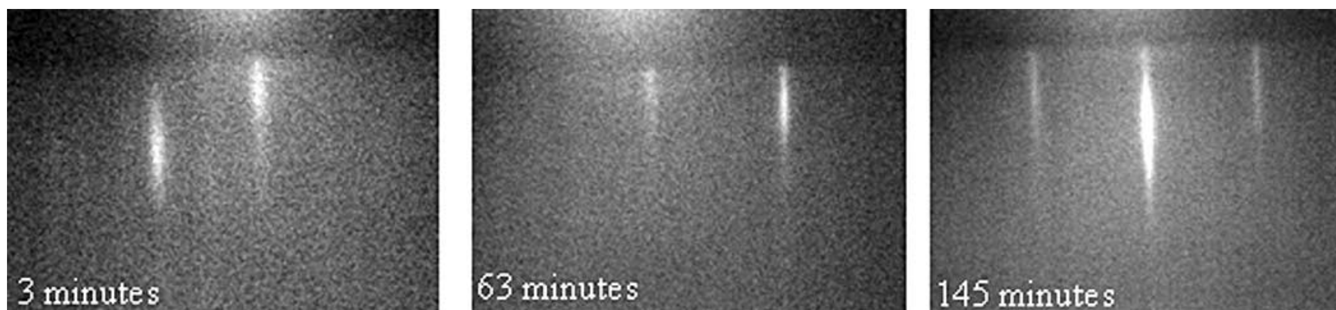


Fig. 4. RHEED patterns of HgCdTe grown on CdTe/Si ROIC taken during different growth stages.

stopped and resumed at a higher temperature of 188°C. Although this temperature is in the proper growth window for single-crystal HgCdTe, it was found to be in the lower end of the window. In the early stages of nucleation, the RHEED patterns show a set of on-streak spots related to the formation of reflection twins, which is a very common problem for the growth of HgCdTe on nominal CdTe (111)B substrates. Although we used misoriented (111)B substrates, the formation of twins will be enhanced when the nucleation temperature is too low. A second sample was nucleated at a higher temperature, followed by a small ramp: we decreased the thermocouple set point from 190°C to 186°C. Figure 4 shows a set of RHEED images taken at different stages for this growth. Streaky patterns with no additional spots are an indication of a two-dimensional growth. The smooth RHEED streaks indicate that good-quality single-crystal HgCdTe has been grown on CdTe/Si ROIC. Using these growth conditions with slight adjustments, more HgCdTe layers were grown on CdTe/Si ROIC.

Single-Chamber CdTe and HgCdTe Growth on Si Substrates

The demonstration that good-quality single-crystal HgCdTe can be grown on Si ROIC is a major requirement for the success of monolithic technology. For further improvements in the material quality, we implemented a second approach. In the first approach, the CdTe buffer and the subsequent HgCdTe layers were grown in two different MBE chambers. During the transfer, the CdTe layer was exposed to the atmosphere and became contaminated, leading to higher defect densities at the CdTe/HgCdTe interface. The best solution to this problem is to grow the CdTe and HgCdTe layers in a single chamber without exposing the CdTe surface to the atmosphere. We have succeeded in establishing single MBE chamber growth of CdTe/HgCdTe on silicon substrates (not yet ROICs) without exposing the surface to the atmosphere at any stage of the growth. The entire structure consisted of about a 7-μm-thick CdTe buffer, followed by our standard double layer planar heterostructure, as previously reported. The streaks in the RHEED patterns indicate single crystalline growth. The surface of the sample is mirror like.

MATERIAL CHARACTERIZATION OF HgCdTe GROWN ON ROIC

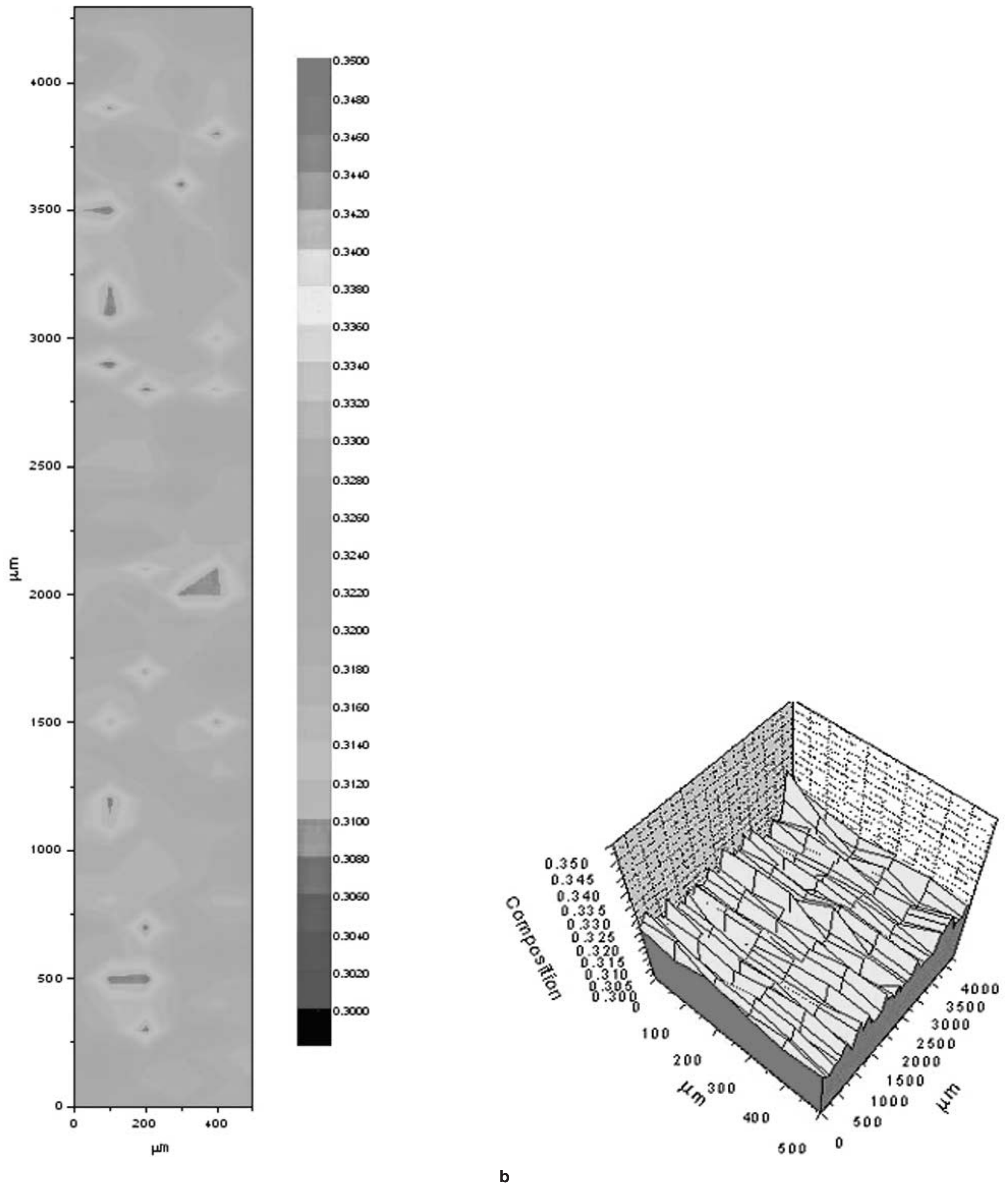
Fourier Transform Infrared Spectrometer Mapping

Although the initial characterization during growth using RHEED indicates good-quality crystalline material on the growth window, we performed additional characterization to evaluate the uniformity of the grown material. The composition uniformity measurements were performed on a Nicolet 870 Fourier transform infrared (FTIR) transmission spectrometer. Shown in Fig. 5a is the composition distribution over the entire $13.8 \times 0.68\ \mathrm{mm}^2$ growth window. Figure 5b gives further details on the distribution of composition over a $500 \times 500\ \mu\mathrm{m}^2$ square area. The average Cd composition x is 0.318 and the standard deviation is 0.003. The standard deviation is slightly larger than that previously reported for HgCdTe grown on conventional substrates,[15] and is probably due to spatial variation of the substrate temperature caused by the influence of the different elements of the ROIC. However, these nonuniformities are not critical because of the absorption band (midwavelength IR) of our devices. Further improvements in uniformity are necessary to implement monolithic technology for long-wavelength IR devices.

Transport Properties

Carrier concentrations, mobilities, and lifetimes are important tools for characterizing the quality of the grown material. They depend on the composition, temperature, doping concentration, degree of compensation, and also on the concentration of inhomogenities, nonuniformities in doping, and defects including grain boundaries and dislocations. As mentioned above, we have incorporated patterns in our mask design that help us electrically characterize the grown wafers.

Hall patterns were fabricated by isolation etching, n-contact In deposition, and Ti/Au pads deposition. The layout and the fabricated pattern are shown in Fig. 6a. The measured results, shown in Fig. 6b, give a carrier concentration in the mid $10^{15}\ \mathrm{cm}^{-3}$ range and a mobility of 10,000 cm^2/Vs at 77 K. Mobilities of the order of mid-$10^4\ \mathrm{cm}^2$/Vs are expected [16] for high-quality $Hg_{1-x}Cd_xTe$ samples with Cd concentrations of $x \sim 0.3$.



a b

Fig. 5. (a) FTIR mapping of the composition over the growth window. (b) Composition distribution across a 500 × 500 μm^2 square area inside the growth windows (right).

Recombination Lifetime Data

Measurements of minority carrier recombination lifetimes are necessary to determine whether the properties of the grown material are limited by fundamental or by defect-induced mechanisms. If defect-induced mechanisms limit the performance, temperature-dependent lifetime data would give insight into the nature of the trap levels. The photoconductive decay method was used for minority carrier lifetime measurements. Temperature-dependent experimental lifetime data are presented in Fig. 7 for material grown on one of the ROICs. The composition x of the material is 0.3 and the doping level is in the low

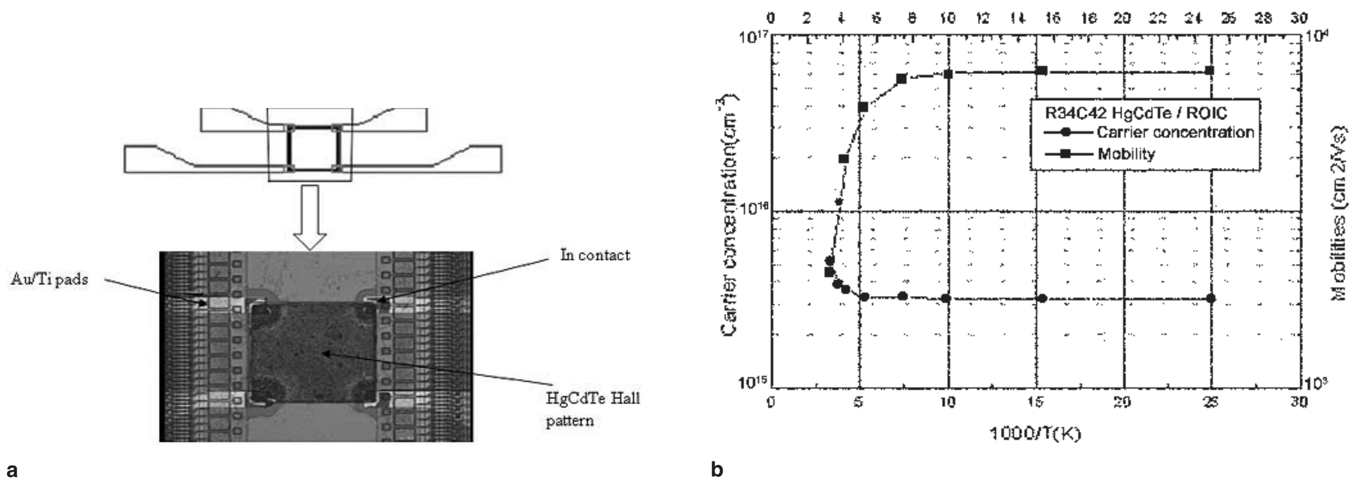


Fig. 6. (a) Lay-out (top) and fabricated (bottom) Hall pattern. (b)Carrier concentration and mobility for HgCdTe grown on ROIC.

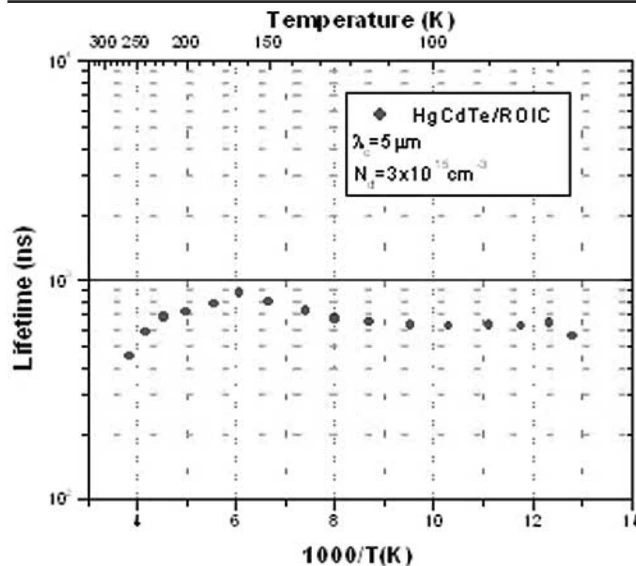


Fig. 7. Temperature-dependent lifetime data.

10^{15} cm^{-3}. A comparison with the theoretical lifetime leads to the conclusion that Shockley–Read–Hall recombination is the dominant recombination pathway in this sample. This is consistent with the observed mobility values presented in the previous section, indicating that the nature of the scattering and recombination centers could be identical.

MONOLITHIC DEVICE FABRICATION

Figure 8 shows a schematic diagram of the monolithic PV fabrication process on the Indigo ROIC wafer. The HgCdTe growth window was opened by chemical etching. Buffered oxide etchant with 10:1 concentration was used. The etching time had first been optimized on Si samples having the same SiO_2 thickness to avoid any overetching on the actual ROIC. CdTe and HgCdTe growth followed, as explained in previous sections. After growth, the entire surface of the ROIC was covered with a HgCdTe/ CdTe layer.

The material grown on Si in the growth window and the material grown on SiO_2 have very different characteristics. The FTIR mapping data shown in the previous section indicate that HgCdTe with uniform composition exists in the 0.68×13.8 mm^2 area designed for array fabrication. However, outside of this area, no FTIR cutoff can be seen. Surface cleaning, preparation, and the complete removal of the oxide appear to be critical factors in growing high-quality HgCdTe on ROICs. An isolation etching was then done to remove the material outside the 0.68×13.8 mm^2 growth window. This etching was carried out using $HBr{:}H_2O_2{:}H_2O$ (10:1:30 in volume) solution. Some deterioration in the metal pads was seen due to the fact that the oxide thickness on the metal pads is less than on the rest of the ROIC, and, as a consequence, it was more easily attacked by the processing chemicals. To solve this problem, we deposited an additional 2000 Å SiO_2 in a plasma enhanced chemical vapor deposition (PECVD) system before the start of processing. Windows for the MBE growth were opened after the deposition. The temperature during the PECVD deposition was lower than 300°C, compatible with the ROIC processing temperatures. Due to lateral etching, slopes were created on the lateral walls assuring that good step coverage was achieved. The step coverage was physically checked with a microscope and step profiler. P-n junction areas were opened through photolithographic processes in the next step. Arsenic ion implantation followed by As activation annealing was performed for p-n junction formation.[17] After annealing, the old CdTe cap layer was etched out due to degradation of its electrical property and a ZnS passivation layer was deposited in thermal deposition chamber. P and n contact areas were opened by wet etching. The n- and p-contact metal deposition was followed by the deposition of interconnection metal between the n- and p- contact metals on the HgCdTe layer and the input metal gates on the Si ROIC, as shown in Fig. 9. The technical difficulty here was to overcome the high step between the HgCdTe layer and Si ROIC surface. For good step coverage, we made a small angle slope on the edge of the HgCdTe/CdTe layer by chemical

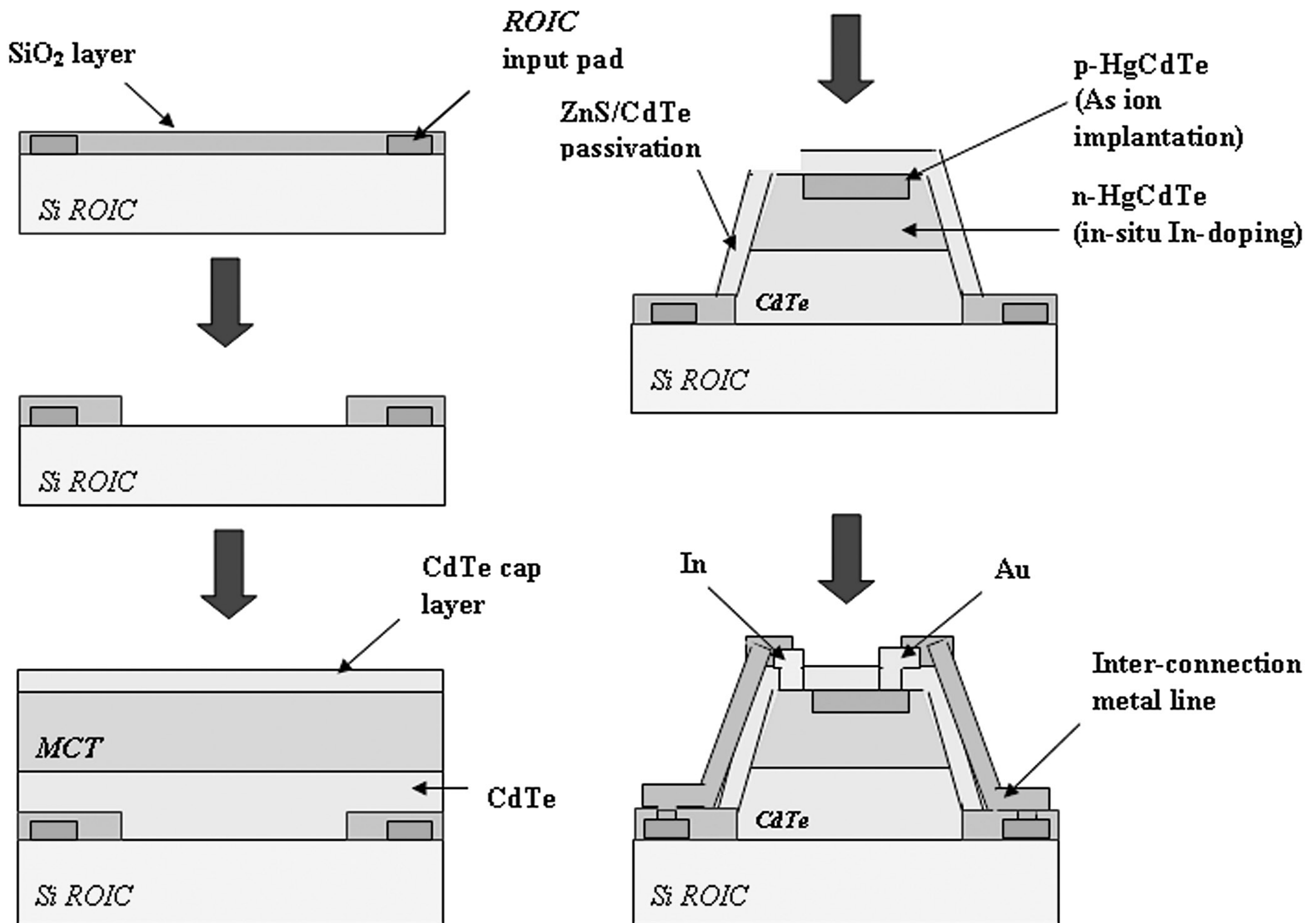


Fig. 8. Schematic diagram of the monolithic HgCdTe PV device fabrication process.

etching and used a planetarium system during interconnection metal deposition. The structure of the interconnection metal was studied by scanning electron microscope. Good step coverage was observed, as seen in Fig. 9.

To implement the monolithic approach in a two-dimensional array format and to preserve the fill factor currently achieved in hybrid arrays, further developments in CdTe and HgCdTe MBE lateral overgrowth are necessary. The processing sequence presented here is compatible with the lateral overgrowth and could be applied for two-dimensional array fabrication if CdTe and HgCdTe lateral overgrowth becomes mature.

DEVICE CHARACTERIZATION

Devices Fabricated from Layers Grown in a Single Run on Si Substrates

A significant achievement is the fabrication and demonstration of devices with 20-μm pixel sizes in a 25-μm pitch linear array format. The I-V characteristics measured at 80 K of the devices fabricated on the single chamber growth sample show excellent properties, with high peak dynamic impedance average on the order of 10^6 Ohm-cm^2 and a breakdown voltage in excess of 600 mV.

Representative I-V characteristics obtained from devices with 20 μm × 20 μm active area fabricated in linear array formats with 25-μm pitch are shown in Fig. 10. The zero bias currents are on the order of picoampere (pA) and the breakdown voltage is greater than 600 mV. The peak R_dA values obtained are in the range of 1×10^5 to mid-10^6 Ohm-cm^2. A peak R_dA value of 1.6×10^7 Ohm-cm^2 was obtained in a 20-μm square pixel. These I-V characteristics were tested in a low-temperature probe station with a 300 K background. We expect the R_dA values to be even higher under true dark conditions with use of good cold shielding.

Devices Fabricated on ROIC

We fabricated a second batch of devices using the growth and device processing technology described in the Monolithic Device Fabrication section. The I-V and R_dA characteristics for one of the pixels of the monolithic array are shown in Fig. 11. Dynamic impedance at zero bias (R_0A) for this device is, to our knowledge, the highest ever reported for an IR device fabricated with monolithic technology. Peak dynamic impedances in the 10^5 Ωcm^2 range were achieved. The dark current at zero bias is 9.2 pA. Some issues related with the uniformity of the electrical

Fig. 9. Metal interconnection between the linear array and the ROIC metal gate.

characteristics are still present, but the demonstration of high impedance devices in a monolithic format is a major step toward monolithic technology.

IRFPA TESTING

After array processing, some dies were tested. Two sets of samples were tested: the first had only HgCdTe/CdTe grown on ROICs (with no subsequent processing) and the second was fully processed. The purpose of the testing was to check the functionality of the ROICs after MBE growth and device processing. Test results for the power dissipation of the ROIC circuitry are listed in Table I.

These test results show higher power dissipation after MBE growth and processing than before. We believe that this deterioration may have been caused by an increase in the resistance of some metal lines that were thinned and narrowed during isolation etching. The strong etchant (HBr + H_20_2) seeps under the photoresist and affects the ROIC metal lines, while the isolation etch (necessary to remove more than 10 µm of HgCdTe/CdTe) is underway. This undercut could be removed or considerably minimized by redesigning the isolation process step. Another cause for deterioration could be the thermal degradation of metal lines during growth. Table I shows the results of power dissipation measurements for four ROIC dies after their fabrications [after the MBE growth (R9C5 and R9C6) and after device processing (R3C5 and R3C6)]. The letters R and C indicate the row and column position of the particular ROIC chip in the 5–in. ROIC wafer. These measurements prove that the operability of the ROIC is retained after the entire MBE growth and monolithic device fabrication

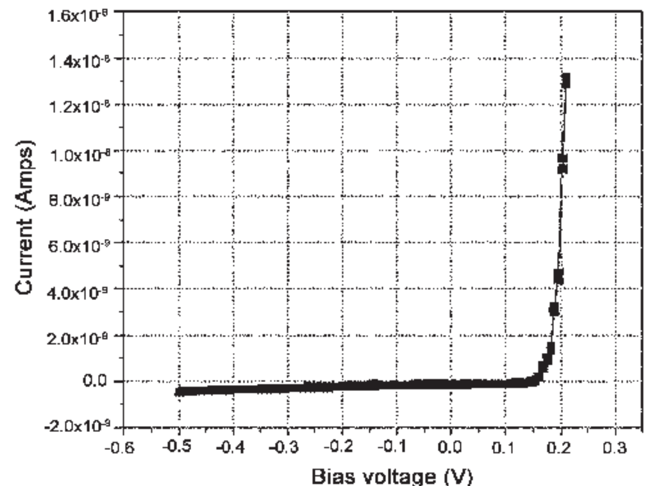


Fig. 10. I-V characteristics of a test diode with 20 µm × 20 µm active area in a linear array of 25-µm pitch, located in the first die of the device layout.

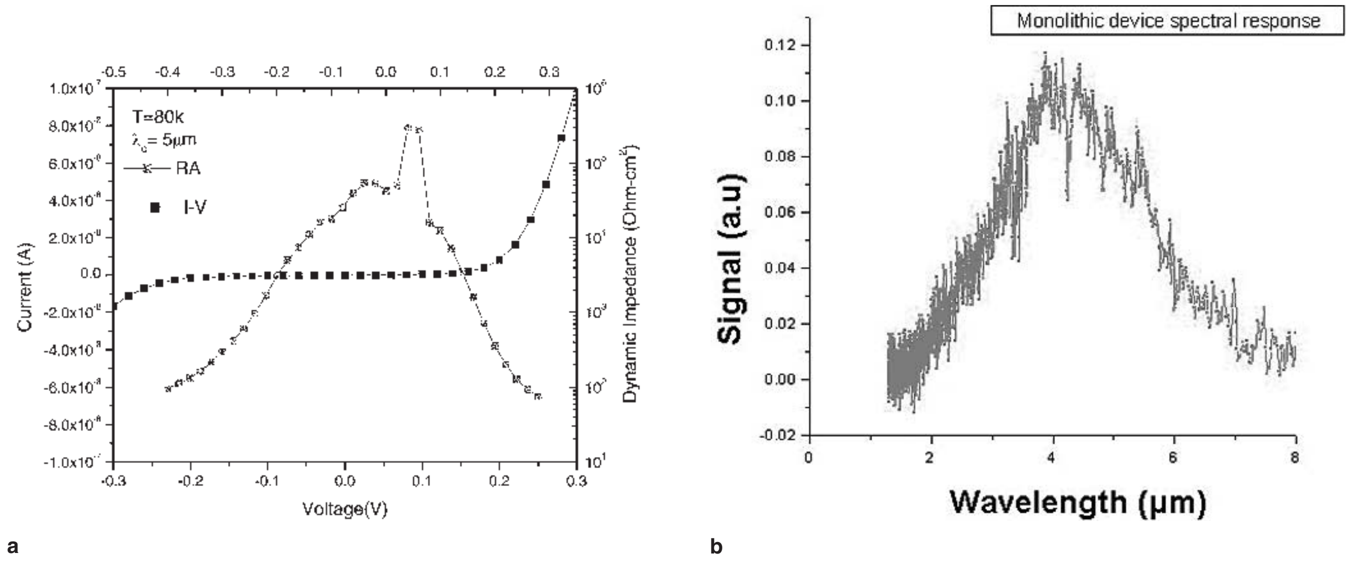


Fig. 11. (a) I-V curve and dynamic resistance for one of the diodes in the monolithic array. (b) Spectral response of the diode.

Table I. Power Dissipation Test Results before and after MBE Growth and Device Fabrication Processing

	Power Dissipation (mW)	
Die	**Preprocessing**	**Postprocessing**
MBE growth		
R9C5 odd channels	44.9	74.9
even channels	44.9	124.7
R9C6 odd channels	44.9	54.9
even channels	44.9	109.7
Fully processed		
R3C5 odd channels	54.9	116.0
even channels	188.5	124.8
R3C6 odd channels	49.9	19.9
even channels	44.9	109.8

process. However, a factor of 2–3 deterioration in the power dissipation indicates that there is room for improvement in the developed technology before arriving at a robust manufacturing method for such devices. The operability of the ROIC is shown in Fig. 12. Implemen-tation of a ROIC protection technique currently underway is expected to further improve the IRFPA operability.

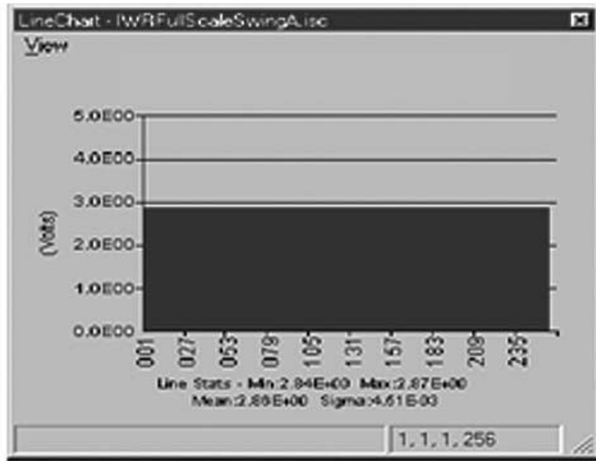
DISCUSSION AND CONCLUSIONS

There are three research groups currently involved in developing monolithic technology for IR applications: the EPIR-Indigo group (Goleta, CA) pursuing a MBE HgCdTe approach, the MOSET-Fermionics group (Simi Valley, CA)[8] pursuing a MOCVD HgCdTe one, and the Swiss Federal Institute of Technology group[9] working on MBE lead chalcogenide (IV-IV) materials. A brief comparison between the best materials grown by these techniques on standard substrates is given in Table II.

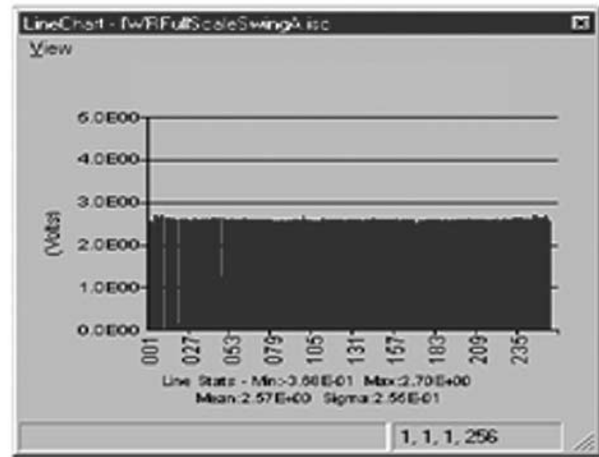
The MBE HgCdTe approach has some advantages over the other techniques. It is interesting to see if these advantages are maintained when monolithic technology is employed. Table III shows in parallel the results obtained by the EPIR, MOSET (Lake Forest, CA), and Swiss Technologies groups. The EPIR results are quite impressive, especially in light of our very recent starting date compared with the other groups. Our low-growth temperature allows for complex structure growth with a minimum of interdiffusion between different layers. The capability to grow in a single chamber considerably reduces the complexity of the growth process and minimizes the defect and dislocation densities. The measured mobilities and lifetimes are compatible with the photovoltaic operation (they lead to diffusion lengths long enough for carrier collection). The obtained R_0A's are compatible with the requirements of the Indigo ROIC that was specially designed to be compatible with the monolithic approach. The demonstration of ROIC operation shows that the fabricated arrays can be practically implemented in an imaging system.

As this program proves, MBE has evolved as an excellent approach for monolithic technology. Great flexibility, precise control over the growth parameters such as layer thickness, composition, doping, and the potential for complex bandgap engineered multilayer detector structures with precisely controlled interface graded layers make MBE a superior technology compared to other methods and materials.

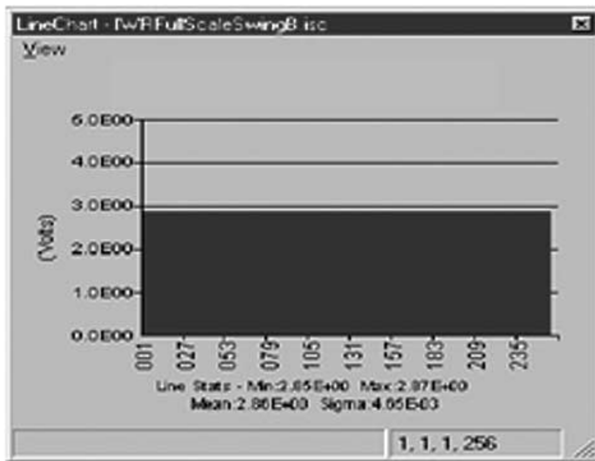
We have addressed and solved several critical issues related to the growth of HgCdTe on Si ROICs and the fabrication of monolithic IRFPAs. The major achievements were (a) the design and the layout of Si ROICs; (b) the low-temperature cleaning of Si(001) wafers; (c) the thermal cleaning of Si ROICs at temperature below 480°C; (d) the design of IRFPA layouts; (e) array fabrication, achieving good interconnections between IRFPA and ROIC input nodes and demonstration of the photovoltaic operation; and (f) maintenance of the ROIC characteristics



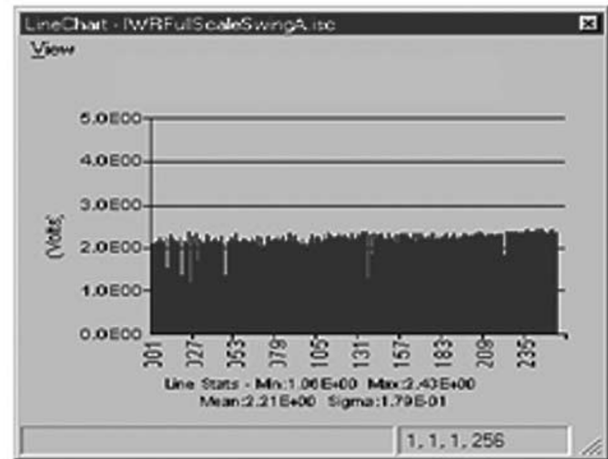
Operability,Odd Channels – pre test



Operability, Odd Channels – post test



Operability, Even Channels – pre test



Operability, Even Channels – post test

Fig. 12. Comparison of the operability before and after fabrication processes.

after substrate cleaning, MBE growth, and device fabrication. The specially designed and custom-fabricated ROICs on misoriented Si(001) wafers to enable subsequent HgCdTe growth by MBE was the first requirement for the technology. The growth of the CdTe buffer layers followed by the multilayer HgCdTe heterostructures was the next significant technological step. Finally, the fabrication of the array along with demonstrated I-V properties takes the proposed monolithic IRFPA technology a leap toward future two-dimensional monolithic IRFPAs. We believe that the current achievements provide a solid foundation for future development of high-performance advanced monolithic HgCdTe IRFPAs.

Table II. State-of-the-Art Material Grown by Different Techniques

Characteristic	MBE HgCdTE	MOCVD HgCdTe	MBE PbTe
Wavelength covered (μm)	3–5, 8–12, 12–18	3–5, 8–12	3–5
Structures grown	p/n, pin, APD, two-color structures	p/n	Metal/semiconductor, p/n
Dislocation density (cm^{-2})	10^5	10^6	10^7
Typical lifetimes (μs) in 3–5-μm range	6	1	No data reported
R_0A ($Ohm\text{-}cm^2$) in 3–5-μm range	10^6–10^7	10^5–10^6	10^2
Status	Advanced development	Development	Research

Table III. Comparison between Monolithic Results of Different Groups

Characteristic	EPIR	MOSET	Swiss Technology
Beginning of the effort	2001	1990	1995
Growth temperature	180°C	360°C	300°C
Dislocations density (cm^{-2})	Mid-10^5	Data not available	2×10^7
Single chamber/single growth achieved	Yes	No	No
Lifetime (ns)	700	Data not available	Data not available
Mobility (cm^2/Vs)	8000	Data not available	Data not available
R_0A (Ohm-cm^2)	10^6	10^5	10^2
ROIC operability demonstrated	yes	no	no

The research results show that monolithic integration of HgCdTe-based IRFPAs on Si ROICs is feasible and can be implemented in the third generation of IR systems.

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