Journal of ELECTRONIC MATERIALS, Vol. 33, No. 5, 2004

Electro-Chemical Mechanical Polishing of Silicon Carbide

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In an effort to improve the silicon carbide (SiC) substrate surface, a new electrochemical mechanical polishing (ECMP) technique was developed. This work focused on the Si-terminated 4H-SiC (0001) substrates cut 8° off-axis toward <1120>. Hydrogen peroxide (H_2O_2) and potassium nitrate (KNO_3) were used as the electrolytes while using colloidal silica slurry as the polishing medium for removal of the oxide. The current density during the polishing was varied from 10 μA/cm^2 to over 20 mA/cm^2. Even though a high polishing rate can be achieved using high current density, the oxidation rate and the oxide removal rate need to be properly balanced to get a smooth surface after polishing. A two-step ECMP process was developed, which allows us to separately control the anodic oxidation and removal of formed oxide. The optimum surface can be achieved by properly controlling the anodic oxidation current as well as the polishing rate. At higher current flow (>20 mA/cm^2), the final surface was rough, whereas a smoother surface was obtained when the current density was in the vicinity of 1 mA/cm^2. The surface morphology of the as-received wafer, fine diamond slurry (0.1 μm) polished wafer, and EMCP polished wafer were studied by high-resolution atomic force microscopy (AFM).

Key words: Electro-chemical mechanical polishing, silicon carbide, atomic force microscopy, hydrogen etching

INTRODUCTION

Silicon carbide (SiC) is a wide band gap semiconductor being developed for high-temperature, high-power, and high-frequency device applications. It is also a promising substrate for the growth of III-V nitrides because of its close lattice match and high thermal conductivity.[1,2] However, SiC presents many challenges for wafer preparation prior to epitaxial growth due to its high hardness and remarkable chemical inertness. A smooth and defect-free substrate surface is important for obtaining good epitaxial layers. Processing-induced defects such as scratches generated by lapping and polishing are the primary contributors to unwanted inclusions in SiC epitaxial films.[3] Standard surface preparation techniques use hard abrasives such as diamond polishing compounds.[4] However, because diamond abrasives achieve material removal through plastic deformation, a damaged subsurface layer containing dislocations is unavoidable.[5,6] In contrast, chemical mechanical polishing (CMP) combines mechanical polishing with a chemical etching action, and can achieve defect-free surfaces. Several CMP techniques have been reported[7,8] and one of them used concentrated colloidal silica slurry with a high alkalinity (PH > 10) at elevated temperature (~55°C). However, normal CMP techniques have low removal rates (0.1–0.2 μm/h at elevated temperature). Chemical mechanical polishing is being used by several wafer vendors, but their processes are proprietary. Hydrogen etching was also reported to obtain a defect-free SiC surface.[9] An obvious disadvantage of a purely hydrogen etching method is that etching removes a uniform layer of material from the surface and therefore cannot efficiently reduce long-range roughness. The purpose of this study is to investigate a new polishing method that can potentially provide a much faster polishing rate with minimal subsurface damage. The idea of this process is to combine anodic oxidation with normal CMP technique, i.e., anodically oxidizing the SiC surface while removing the oxide using oxide CMP.

(Received December 17, 2003; accepted Feb. 23, 2004)

We investigated the use of this new electro-chemical mechanical polishing (ECMP) technique for the removal of subsurface damage on commercially available SiC wafers. Since the colloidal silica slurry is softer than SiC, the polishing process will only remove the oxide formed without introducing any additional subsurface damage. High-resolution AFM study indicates that an optimized ECMP may provide an alternative method of obtaining a smooth SiC surface. The process described here can also be used to polish saw cut wafers at a fast rate. This will be an alternative method of polishing that can result in potentially subsurface damage-free wafers.

EXPERIMENTAL CONDITIONS

The wafers used in this study were standard commercial 2-in.-diameter n-type 8° off-axis 4H-SiC (0001) substrates. The samples were cut to 1 cm × 1 cm size and carefully mounted onto the polishing holder using wax. The edges of the sample were sealed to prevent sharp edges cutting the polishing pad and chipping the samples and to prevent leakage current around the edges. A Minimet polisher (Buehler Ltd., Lake Bluff, IL) was used with a Southbay Technology Chemotex polishing pad (SBI Inc., San Clemente, CA) and Advansil 2000 silica slurry with a pH of about 10. The samples were polished with downward pressure of 1 psi at a speed of 120 rpm. KNO_3 and H_2O_2 were used as the anodizing agents. The schematic of the ECMP setup is shown in Fig. 1. The samples were polished in pure de-ionized water for 5 min after the EMCP process to remove silica particles from the surface.

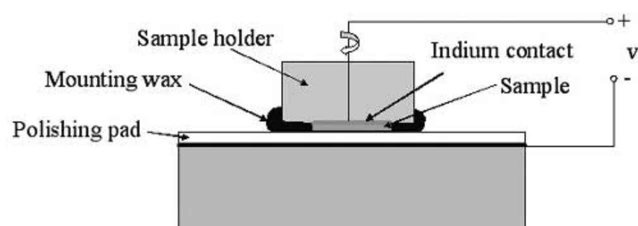

Fig. 1. Schematic of the ECMP setup.

RESULTS AND DISCUSSION

Several preliminary polishing experiments were carried out without passing current. Both silica slurry and a mixture of anodizing agents and silica slurry were used in these trials. No polishing was observed after 6 h of CMP at room temperature, although a very low polishing rate (~150 Å/h) was reported by Saddow et al.[10] A simultaneous oxidation/CMP process was then carried out. A mixture of KNO_3 with silica slurry solution (1:1 = 10% KNO_3: silica slurry) was first used as the medium for this process. Current density was varied from 10 μA/cm^2 to 20 mA/cm^2 under otherwise identical conditions. The removal rate increases with the current level, finally reaching 0.4–0.5 μm/h with a current level of 20 mA/cm^2. However, scratches can still be seen even after 3 h of the simultaneous process. We believe that the faster anodization rate leads to net growth of oxide and also polishing scratches on the oxide by CMP. Further processing would replicate these features into the SiC surface. Similar experiments were carried out by replacing KNO_3 with H_2O_2. However, the same surface features were observed after the process. Scratches can be seen under the optical microscope, as shown in Fig. 2.

It is clear that a simultaneous oxidation/polishing process results in many scratches on the SiC surface. Because silica abrasives are used to remove the oxide, the oxide will have scratches. Because

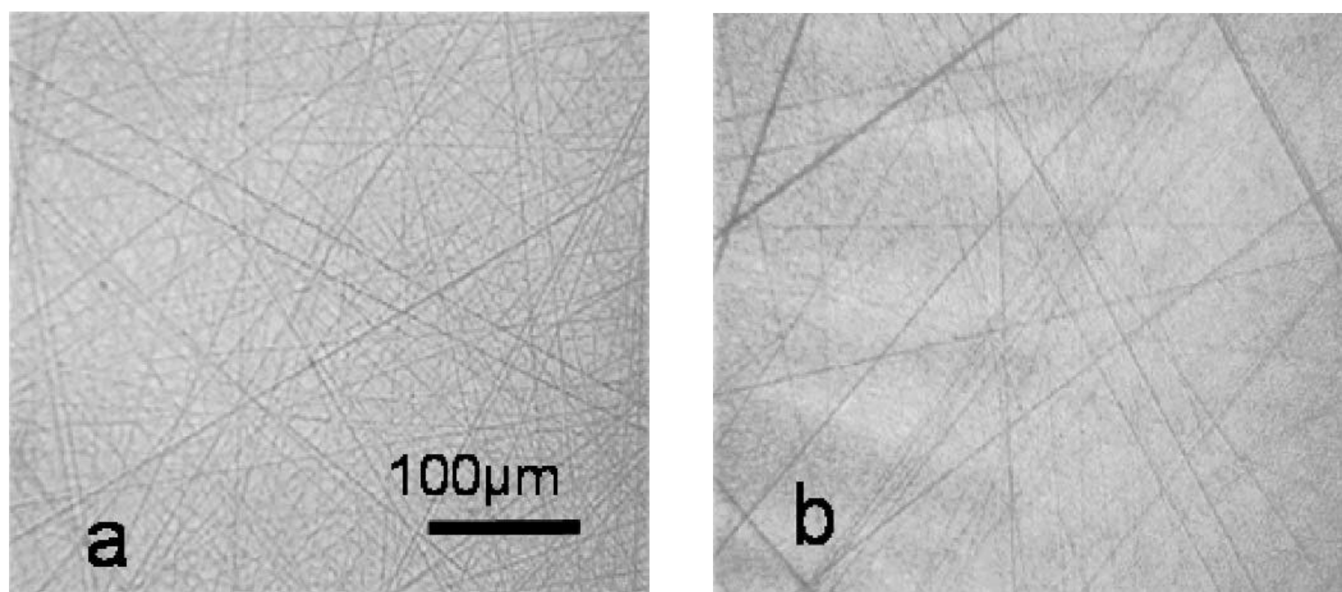

Fig. 2. Optical microscope images of the SiC surface after the simultaneous oxidation/CMP using 1:1 = H_2O_2: Advansil 2000 silica slurry: (a) current density = 16 μA/cm^2; and (b) current density = 1 mA/cm^2. The surface was etched in a dilute HF solution after polishing to remove any residual oxide.

the oxidation takes place during polishing, these scratched regions will preferentially oxidize more than the surrounding region where the oxide thickness is the least. Hence, these scratches will carry over to the substrate during anodic oxidation. To avoid this, a two-step process was developed in which the oxidation and the polishing steps are separated. Anodic oxidation was carried out using pure H_2O_2 for a short time (typically 30 sec), followed by the silica slurry CMP polishing process for 30 min to remove the oxide. Both steps were done with the downward pressure of 1 psi at a speed of 120 rpm. This two-step cycle can be repeated until scratches on the sample surface are no longer visible. We have observed that the as-received substrate after oxidation reveals numerous polishing scratches decorated by the oxide, whereas these scratches are hardly seen on as-received SiC under the optical microscope prior to oxidation. After several cycles of the two-step ECMP process, scratches were hardly seen with the decoration by anodic oxide, as shown in Fig. 3. We believe that the top surface layer with scratches has been removed by our ECMP process. The reason why the two-step process results in scratch-free surface can be explained as follows: During anodization, uniform oxidation may take place on a rough surface. However, during the oxide CMP, only the "surface peaks" get polished. During the succeeding anodization process, these surface peaks may get preferentially oxidized because current density in this oxide-free area is the highest. Hence, the two-step process may be self-planarizing.

The effects of the anodic current density and time on the polishing rate and surface morphology were investigated. Oxide thickness in one anodic cycle was measured by a spectroscopic ellipsometer, and the thickness of SiC removed was measured by weight loss, as summarized in Table I. The surface roughness of the oxide and the small amount of weight change for the 1 cm × 1 cm SiC sample resulted in a significant error for these measurements. Even so, we can see that anodic oxide thickness increases with the anodic current density and time; thus, the amount of SiC removal also increases. Therefore, high anodic current density associated with the high removal rate of oxide could be a potential way to obtain fast removal of SiC.

The surface morphology after the EMCP process was also studied by high-resolution atomic force microscopy (HRAFM), as shown in Fig. 4. The surface morphology significantly changed after the ECMP process. Scratches were not seen on the surface, which confirmed the previous conclusion that the top layer with scratches was removed during the process. The 0.1-μm fine diamond slurry polishing did not improve surface roughness. In contrast, extra scratches were introduced after the diamond polishing, as shown in Fig. 4b. The best surface was obtained when anodic current density was in the vicinity of 1 mA/cm^2. The surface is almost featureless under high- resolution AFM except for some contamination created during the polishing and cleaning of the sample (Fig. 4c). However, with an increase of the current density, wavy pits were present after the ECMP process, and surface roughness of the samples increases, as shown in Fig. 5. The depth of the wavy pits varied from 10 nm to 20 nm, which indicated that they are not related to micropipes. Higher current leads to a rougher surface, and a shorter anodic time for each cycle did not improve surface roughness, as shown in Fig. 4d–f. The reason for the formation of pits is not clear at

Fig. 3. Optical microscope images of an oxidized surface under 5 mA/cm^2 for 30 sec after (a) 1 cycle, (b) 6 cycles, and (c) 12 cycles of polishing using the two-step ECMP process.

Table I. Comparison of the SiC Removal Rate under Different Anodic Current Conditions

Anodic Current (mA/cm^2)	Anodization Time (s)	Oxide Thickness in One Cycle (Å)	Number of Cycles	Thickness Removed (μm) (by Weight Loss)
1	30	~150	12	Not measurable
5	30	~400	12	0.65
>20	30	~1000	12	0.7
5	5	~150	36	1.2

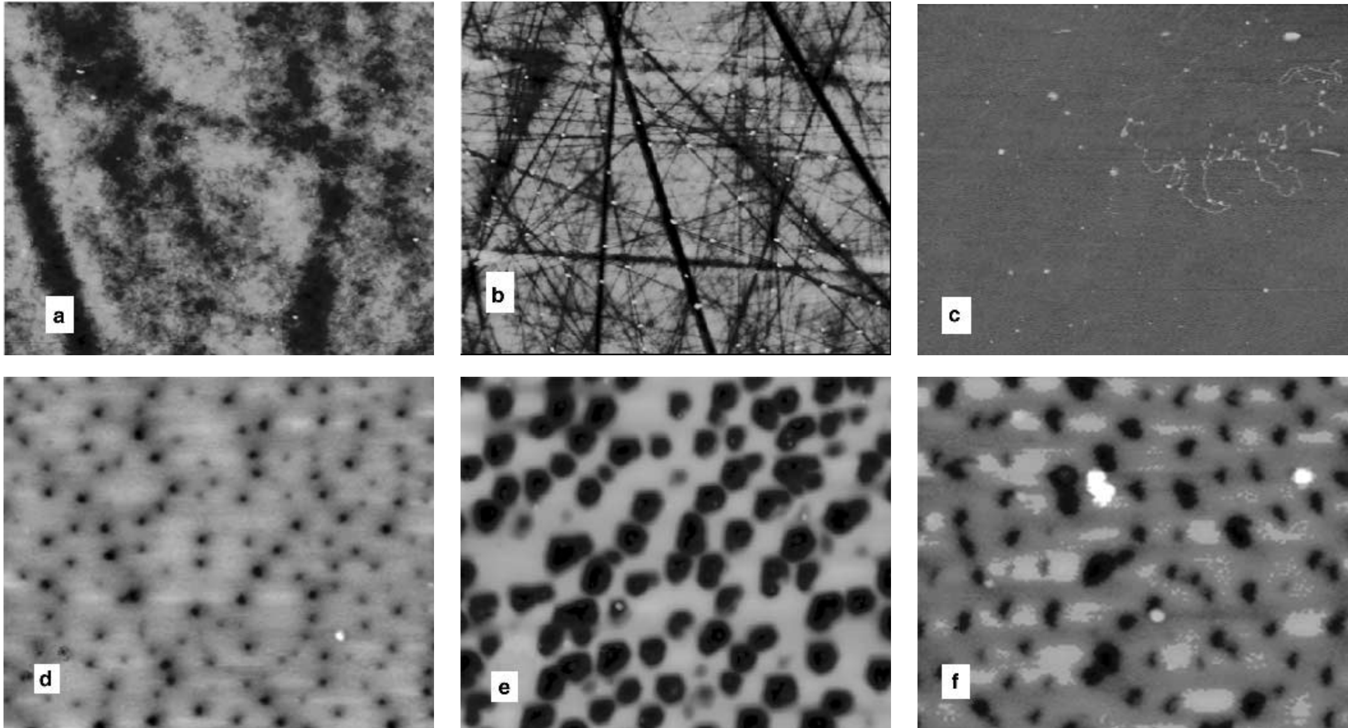

Fig. 4. High-resolution (2 μm × 2 μm) AFM images of 4HN SiC polished under different anodic current conditions: (a) as-received, RMS roughness: 0.77 nm (Z range: 8.0 nm); (b) 0.1-μm diamond polish, RMS roughness: 0.50 nm (Z range: 12.1 nm); (c) 1 mA/cm^2, 30 sec, RMS roughness: 0.20 nm (Z range: 14.5 nm); (d) 5 mA/cm^2, 30 sec RMS roughness: 1.11 nm (Z range: 29.4 nm); (e) >20 mA/cm^2, 30 sec, RMS roughness: 10.52 nm (Z range: 63.3 nm); (f) 5 mA/cm^2, 5 sec, RMS roughness: 2.42 nm (Z range: 28.2 nm).

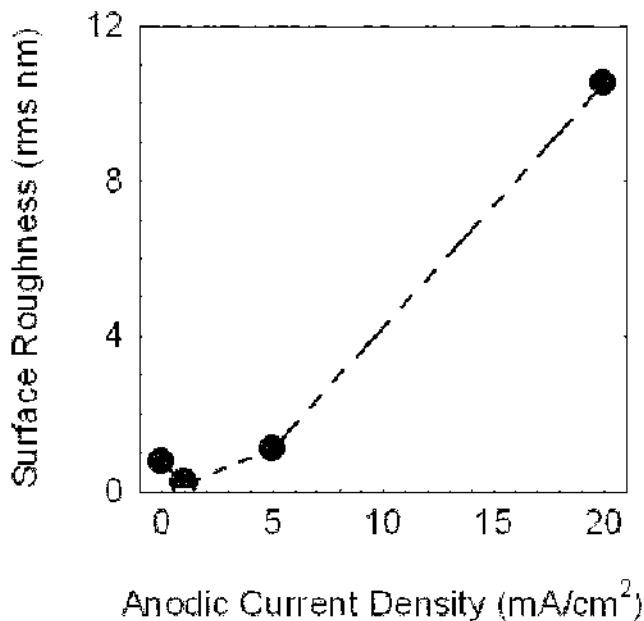

Fig. 5. SiC surface roughness versus anodic current density. Zero current density corresponds to as-received wafer.

present. Pits have been observed by oxidation/etch[10] and molten KOH etch of SiC.[11] They were believed to be related to the preferential oxidation at the dislocations. However, based on the distribution of the pits on the surface of the ECMP wafers, we believe that pit formation involves a distribution of electric field across the surface during the anodic oxidation process. The field lines concentrate at surface "peaks" and selectively enhance anodization and removal of SiC. Under low current density, the selective anodization and removal rate of SiC are not high enough to form pores. The result is a smooth, planarized surface after removal of the oxide by softer slurry CMP. However, a larger current density would enhance the nonuniformity of breakdown across the surface, resulting in the initiation of pores, as happens during Si anodization.[12,13] It is noteworthy that a balance between the formation and the removal of the oxide is also crucial for successful polishing of SiC by this process. Faster anodization will form thick porous oxide on the surface that cannot be easily removed completely during the succeeding oxide polishing step. An intentional long-time anodic process was carried out on SiC. The anodization lasted for 20 min under 20 mA/cm^2. Half of the sample was then dipped into HF to remove the oxide layer. The boundary was clearly seen after HF rinse, and the thickness of the oxide removed was about 0.5 μm. Figure 6 shows the AFM images for both halves of the sample. It can be clearly seen that porous oxide was formed after the long-time anodic process and porosity of anodic oxide was propagated onto the SiC surface.

It has been reported that hydrogen can be a useful pregrowth etchant for SiC epigrowth.[14] To study the effects of hydrogen etching on a pitted ECMP wafer, simultaneous hydrogen etching was

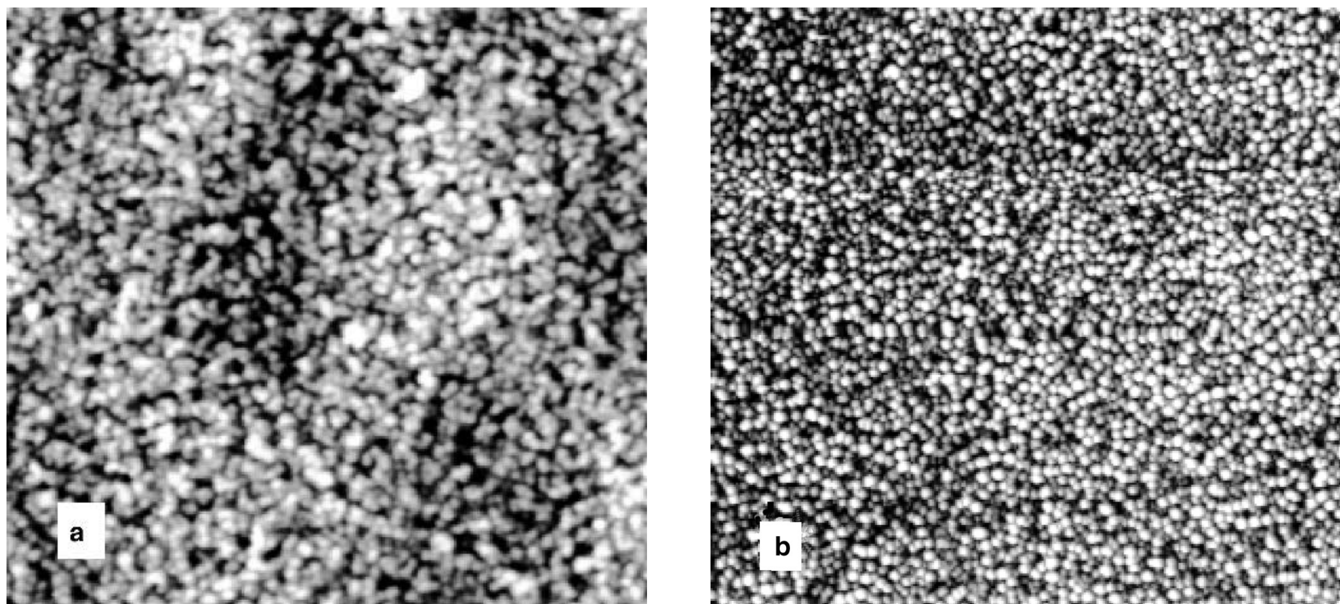

Fig. 6. AFM images (5 μm × 5 μm) of n-type 4H SiC: (a) after 20 min of anodic oxidation under 20 mA/cm^2 current and (b) after removal of oxide by HF. The thickness of the oxide was about 0.5 μm measured by profilometer.

performed on an as-received sample and the pitted ECMP polished sample shown in Fig. 4f. The 60 ppm propane was added to hydrogen during the etching to avoid the formation of Si droplets after hydrogen etching, as described elsewhere.[15] The HRAFM of the hydrogen-etched surface is shown in Fig. 7. Surface roughness (RMS) of the ECMP sample improved significantly (Fig. 7b compared to Fig. 4f). A smoother surface was obtained for the ECMP sample even though the surface was very rough before etching. This suggests that hydrogen etching is a very effective method to further reduce the surface roughness of ECMP polished wafers.

CONCLUSIONS

A new ECMP process was developed to polish SiC at a fast rate. The balance between anodic oxidation and oxide polishing is crucial to achieve a smooth and defect-free surface. The simultaneous oxidation/polishing process with our experimental setup results in a rough surface, whereas the two-step process under appropriate anodic oxidation conditions results in a smooth surface. Higher anodic current density would lead to a pitted surface morphology. However, high-temperature hydrogen etching is effective at reducing the surface roughness further for the ECMP-polished wafer. A smooth

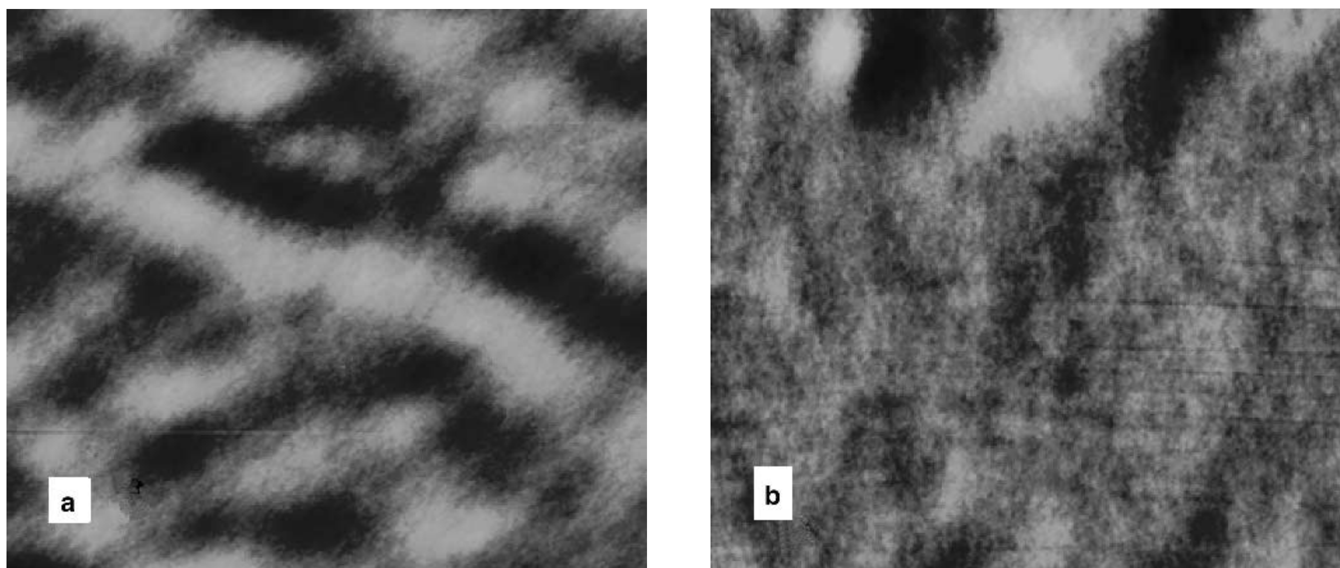

Fig. 7. High-resolution AFM images (10 μm × 10 μm) of 4HN SiC after H_2 etching at 1450°C for 10 min with 60 ppm C_3H_8 added: (a) as-received wafer, RMS roughness 0.46 nm (Z range: 3.1 nm); and (b) ECMP polished with 5 mA/cm^2, 5 sec during anodic oxidation step, RMS roughness 0.27 nm (Z range: 2.9 nm).

surface has been achieved on the pitted ECMP sample after hydrogen etching. The method described provides an alternative way to polish SiC substrates at a fast rate and still achieve an atomically smooth surface.

ACKNOWLEDGEMENT

This work was supported by DARPA Contract No. DAAD19-02-1-0246.

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