Threading and Misfit-Dislocation Motion in Molecular-Beam Epitaxy–Grown HgCdTe Epilayers

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Lattice mismatch between the substrate and the absorber layer in single-color HgCdTe infrared (IR) detectors and between band 1 and band 2 in two-color detectors results in the formation of crosshatch lines on the surface and an array of misfit dislocations at the epi-interfaces. Threading dislocations originating in the substrate can also bend into the interface plane and result in misfit dislocations because of the lattice mismatch. The existence of dislocations threading through the junction region of HgCdTe IR-photovoltaic detectors can greatly affect device performance. High-quality CdZnTe substrates and controlled molecular-beam epitaxy (MBE) growth of HgCdTe can result in very low threading-dislocation densities as measured by the etch-pit density (EPD $\sim 10^4$ cm^{-2}). However, dislocation gettering to regions of high stress (such as etched holes, voids, and implanted-junction regions) at elevated-processing temperatures can result in a high density of dislocations in the junction region that can greatly reduce detector performance. We have performed experiments to determine if the dislocations that getter to these regions of high stress are misfit dislocations at the substrate/absorber interface that have a threading component extending to the upper surface of the epilayer, or if the dislocations originate at the cap/absorber interface as misfit dislocations. The preceding mechanisms for dislocation motion are discussed in detail, and the possible diode-performance consequences are explored.

Key words: HgCdTe, dislocations, molecular-beam epitaxy (MBE)

INTRODUCTION

The performance of long-wave infrared (LWIR) and very long-wave infrared (VLWIR) photovoltaic devices can be degraded by the presence of dislocations in the HgCdTe epitaxial layer.[1–5] Dislocations threading the junction region can theoretically act as tunneling (conductive) pathways, and dislocations in the active layer can also act as trapping and recombination centers that degrade detector performance.[1–5] When dislocations in LWIR and VLWIR HgCdTe focal-plane arrays (FPAs) intersect the diode region, they result in degraded zero-bias impedance (R_oA) and an increased diode dark current. Consequently, understanding and controlling the formation and motion of dislocations in the junction region of the diode are of critical concern when fabricating high-performance LWIR and VLWIR detectors.

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It is well-known that the misfit strain between the substrate and the epitaxial layer in heteroepitaxial systems is accommodated (at least partially) by the formation of misfit dislocations at the substrate/epilayer interface.[6–10] These interfacial misfit dislocations are far from the metallurgical-junction interface and are believed to have minimal impact on diode performance. However, for a typical LWIR heterojunction-device structure, where a cap layer is grown on top of the absorber layer, misfit dislocations can theoretically form near the p-n junction at the cap/absorber interface.

The formation of misfit dislocations at the interface between the substrate and the absorber layer and between the absorber layer and the cap depends on the misfit strain between the adjacent layers and the thickness of each layer. Because the location, density, and mobility of these misfit dislocations can degrade individual diode performance and, thus,

reduce the ultimate performance of the array, understanding the dislocation formation and motion mechanisms involved is crucial when attempting to improve the ultimate performance of LWIR and VLWIR devices.

BACKGROUND

The theory for misfit-dislocation formation and glide has been extensively developed and detailed for many different epitaxial systems. Specifically, when a thin epitaxial film with a lattice constant of a_e is grown epitaxially on a suitable substrate of lattice constant a_s, where $a_e \neq a_s$, the layer is grown in a state of biaxial strain.[11–13] Initially, the strain is accommodated elastically by the epitaxial layer and is stored as elastic-strain energy. As the thickness of the epitaxial layer is increased, the stain energy increases accordingly. Eventually, a critical thickness (h_c) is reached, above which it becomes energetically favorable for the epitaxial layer to accommodate a portion of the misfit strain by introducing a network of misfit dislocations at the epitaxial interface.[6–10] The magnitude of the critical thickness is dependent on the magnitude of the lattice strain between the substrate and the epitaxial layer and the thickness of the epitaxial layer. Berding et al. published the details regarding the calculation of the critical thickness (h_c) for the HgCdTe/CdZnTe system.[14]

The misfit strain (f) in the epitaxial system is typically defined as

$$f_{misfit} = \frac{a_s - a_e}{a_s} \quad (1)$$

For a one-dimensional network, full relaxation would result in a network of misfit dislocations with a spacing of S (or written as a linear misfit density, ρ_{MD}) where

$$S = \frac{1}{\rho_{MD}} = \frac{b}{f_{misfit}} \quad (2)$$

where b is the magnitude of the Burger's vector. This spacing represents the maximum density of dislocations, assuming 100% of the strain energy is released via the formation of misfit dislocations at the epitaxial interface.[6–10] However, in the HgCdTe/CdZnTe epitaxial system (as well as other semiconductor systems), some of the strain energy is known to be released by other mechanisms, such as the formation of surface relief or crosshatch.[15–30] Consequently, the spacing of misfit dislocations at the interface may actually be significantly larger than the equilibrium spacing predicted by Eq. 2, assuming 100% of the elastic strain is released via the formation of misfit dislocations.

For epitaxial layers exceeding the critical thickness (h_c), it becomes energetically more favorable for the misfit strain to be accommodated by the formation of misfit dislocations at the epitaxial interface. However, this condition alone ($h > h_c$) is not sufficient to guarantee the formation of misfit

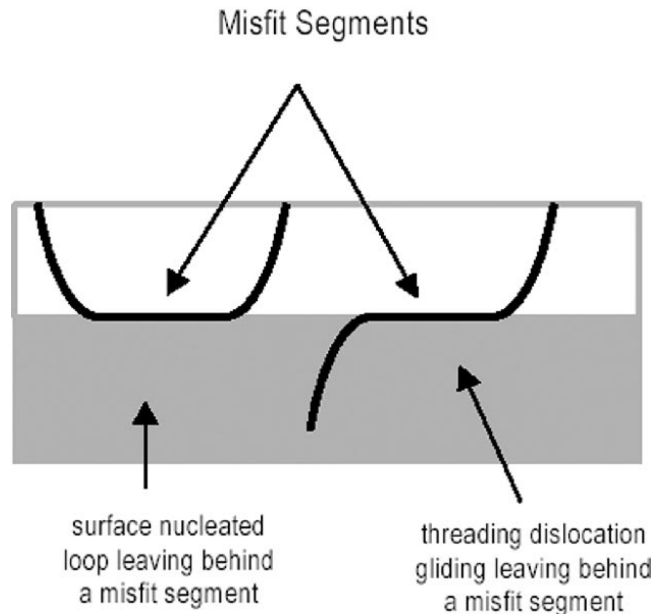

Fig. 1. The schematic of misfit-dislocation formation mechanisms in epitaxial systems.[8]

dislocations. Once the thickness of the epitaxial layer is greater than the critical thickness, there is a driving force for misfit formation (the release of the elastic strain); however, a mechanism for misfit formation is required to form the misfit dislocations at the epitaxial interface. A mechanism for misfit formation was proposed by van der Merwe and expanded on by Matthews and Blakeslee whereby existing threading dislocation can bend over and glide along the epitaxial interface leaving behind a misfit segment.[6–8,10] It was also proposed that dislocation loops could nucleate at the surface of the epitaxial film and grow down and into the film until it intersects the interface forming a misfit-dislocation segment (Fig. 1).[6–10]

The formation of misfit dislocations as proposed by van der Merwe and the subsequent concept of a critical thickness for the epitaxial layer is an equilibrium argument.[6–10] The bending over of existing threading dislocations or the nucleation of new dislocations is a kinetically driven process and requires activation energy. The relatively low temperatures used during the MBE growth of HgCdTe allow for epitaxial layers to grow in a metastable regime exceeding the critical thickness without the formation of misfit dislocations, resulting in a final epitaxial layer that has not fully relaxed the misfit strain by the formation of misfit dislocations or surface relief (crosshatch) and exists in a metastable state of high strain.[15–30]

Both the crosshatch formation and misfit-dislocation formation during growth occur along certain crystallographic directions consistent with operating-slip systems. For (111)B-oriented growth, which is typical for the liquid-phase epitaxy growth of HgCdTe, the crosshatch pattern and the misfit-dislocation network that forms are parallel to the

⟨110⟩ slip directions where the (111) growth plane intersects three other {111} planes.[15–18] For MBE growth of HgCdTe on CdZnTe, where the (211)B growth surface is used, the resulting crosshatch pattern and misfit-dislocation network form parallel to the [−231], [−213], and [01−1] directions.[15–18] Although the crosshatch pattern and the misfit-dislocation network form along the same crystallographic directions, the two strain-relief processes are not directly related, and the spacing of the crosshatch pattern does not directly correlate with the formation and spacing of misfit dislocations. In some epitaxial systems, the stress concentration located in the valley regions of the crosshatch pattern can nucleate dislocation loops that grow to form misfit segments; however, other systems have been shown to form crosshatch patterns at the exclusion of misfit dislocations, while other systems have shown the opposite tendency, where misfit formation seems to be dominant over crosshatch formation.[19–25] In fact, the two strain-relief mechanisms may actually be competing mechanisms; both seeking to relieve the misfit strain in epitaxial growth of HgCdTe. Many excellent papers have been published on the topic of surface relief and crosshatch formation, and the details can be found there.[15–25]

Both mechanisms of strain release (crosshatch-surface relief and misfit-dislocation formation) are typically kinetically driven processes and, thus, depend on the thermal history of the sample and the growth conditions under which the epilayer was grown. Consequently, the extent of the strain energy stored in the as-grown layer can conceivably vary from layer to layer, depending on the growth parameters. Layers that exist in a relatively high state of stress after growth are metastable at room temperature and will seek to relieve this stress by the formation of misfit dislocations, surface relief, or both.[15–30] Although surface relief is known to form in the HgCdTe system, it is not believed to degrade diode performance directly. Therefore, this work will ignore the formation of surface relief (crosshatch) and focus on the formation of misfit dislocations.

Misfit dislocations can form from several different mechanisms. The dominant mechanisms in many semiconductor systems are the bending over of threading dislocations at the interface between the two strained layers and the subsequent glide of the dislocation along the interface, leaving behind a misfit segment (Fig. 1).[31–35] Misfit dislocations can also be formed via the nucleation of dislocation half-loops at steps or impurities at the growth surface. The half-loop grows into the layer until it intersects and glides along the interface, leaving behind a misfit segment connected by two threading-dislocation segments that terminate on the free surface (Fig. 1).

When a threading dislocation bends over and glides along the substrate/epi interface to form an interfacial misfit dislocation, the misfit segment is far from the junction area and should have minimal impact on device performance. However, if the threading dislocation bends over and glides along the cap/absorber interface, the resulting misfit dislocation will lie at the junction interface and can conceivably be highly detrimental to device performance. Figure 2 shows a schematic of a threading dislocation gliding along the substrate/absorber layer interface (left) and a threading dislocation gliding along the absorber/cap interface (right). Theoretically, the cap layer thickness and the lattice mismatch (Δx) between the absorber and cap are designed and fabricated below the critical thickness, and misfit dislocations should not form.[13] However, the nonrelaxed strain accumulated in the growing layer below the absorber/cap interface may result in the lattice mismatch between the absorber and cap to be significantly greater than the theoretical value. This could reduce the critical thickness for the cap and, thus, allow for misfit dislocations to glide along that interface. Because of the proximity of the cap interface to the metallurgical-junction interface, dislocations gliding along this interface may have an impact on detector performance.

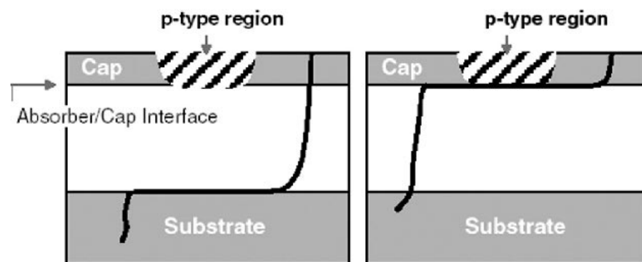

Fig. 2. The schematic on the left is of the threading dislocation gliding along the substrate/absorber interface, leaving behind a misfit dislocation at that interface. The schematic on the right is of the threading dislocation bending over at the absorber/cap interface, leaving behind a misfit-dislocation segment that could intersect the junction region.

The problem of understanding and controlling misfit-dislocation formation at the cap/absorber interface is more complicated than just being able to grow a low dislocation-density HgCdTe layer. The as-grown epitaxial layers exist in a state of strain and are metastable. Consequently, the HgCdTe layer may relax during subsequent processing, and misfit dislocations may form. The epitaxial layers typically undergo a series of process steps to fabricate diodes. These process steps can include local ion implantation via etching, metallization, and high-temperature annealing. The implantation via etching and metallization result in local regions of high stress within the material and potentially act as dislocation-gettering centers or nucleation sites for additional dislocations.[2–4,36] The elevated-process temperature used during device annealing overcomes any kinetic barriers to misfit formation and the layer relaxes, leaving behind a network of misfit dislocations at the epitaxial interfaces. At these elevated temperatures, existing dislocations become mobile and can getter to local regions of high stress, resulting in an increased dislocation density in the diode region. Therefore, understanding whether

dislocations form at the cap/absorber interface and whether they become mobile during device processing and getter to the diode region of the material is vital. For this work, we have developed a series of experiments to determine if misfit dislocations form at the cap interface and if they are mobile under typical processing conditions.

EXPERIMENTAL PROCEDURE

A series of experiments were performed on VLWIR-HgCdTe thin films grown epitaxially on CdZnTe substrates. A series of experimental $Hg_{1-x}Cd_xTe$ epitaxial layers were grown using MBE with various cap Δx to determine if misfit dislocations form at the cap/absorber interface and under what conditions they form. The samples were dislocation etched using a decorative technique to observe misfit dislocations near the surface of the epitaxial layer. The chemical etch used for resolving a misfit dislocation was the same $CrO_3/HCl/H_2O$ dislocation etch used for resolving threading-dislocation etch pits in HgCdTe. The samples were etched for approximately 8 sec. An identical set of samples were annealed at ~430°C for 10 min and then etched using a light, 8-sec decorative etch to observe any dislocations that formed during annealing.

An experimental VLWIR performance-evaluation chip (PEC) was fabricated using the standard planar-device technology used at Rockwell Scientific (Camarillo, CA). After device testing, the PECs were then stripped down to the HgCdTe epilayer using a chemical-etching procedure at room temperature to remove the metal-contact pads and passivation layer. The stripped PECs were then etched using a decorative dislocation etch to observe the presence of misfit and threading dislocations. The stripped and etched PECs were then observed under a Nomarski microscopy to observe the presence of any dislocations and their relative position to the junction area.

RESULTS AND DISCUSSION

Threading dislocations originating deep within the epitaxial layer or the substrate with a Burger's vector perpendicular to the top surface of the epitaxial layer should appear as a single etch pit on the surface of the HgCdTe layer when the layer is etch-pit density (EPD) etched. When a threading dislocation glides, it leaves behind a misfit segment along the epitaxial interface (Figs. 1 and 2). The extra half-plane of atoms and the stress field associated with the edge component of the misfit dislocation are resolved as a thin line connected to a terminating etch pit on the sample surface (Fig. 3) when the sample is EPD etched.[17] This allows for both threading and misfit dislocations to be observed using decorative etching techniques and optical microscopy.[17] The threading component of the dislocation is always observed because it intersects the upper surface of the material. The misfit component is only observed if the strain field associated with the extra half-plane of atoms intersects the upper surface.

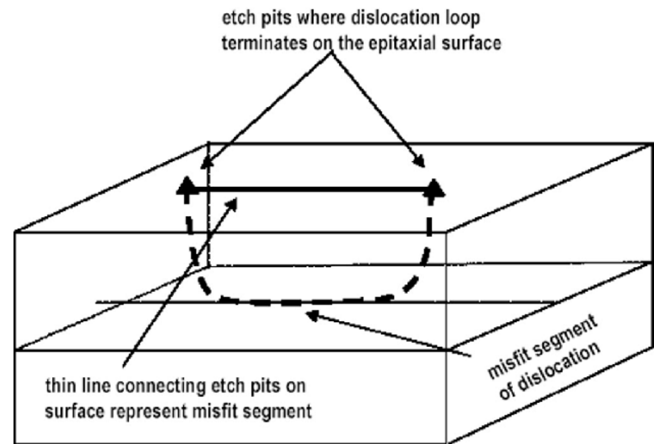

Fig. 3. The schematic of a dislocation loop with a misfit segment that has been EPD etched. The threading section that intersects the epitaxial surface terminates on an etch pit. The misfit segment is resolved as a thin line connecting the etch pits.

The strain field diminishes with distance from the core of the dislocation. Consequently, only misfit dislocations near the surface (the depth is approximately the critical thickness) are resolved by decorative etching. Hence, in a VLWIR or LWIR epitaxial layer with a thickness of 10 μm or more, the strain field of misfit dislocations at the substrate/absorber interface is not observable by dislocation etching because the strain field has diminished to the background level of strain within the material. Therefore, it is reasonable to assume that misfit lines observed by dislocation etching the surface layer are formed at the absorber/cap interface.

Figure 4 shows an experimentally grown, MBE, VLWIR-HgCdTe layer that has been annealed at

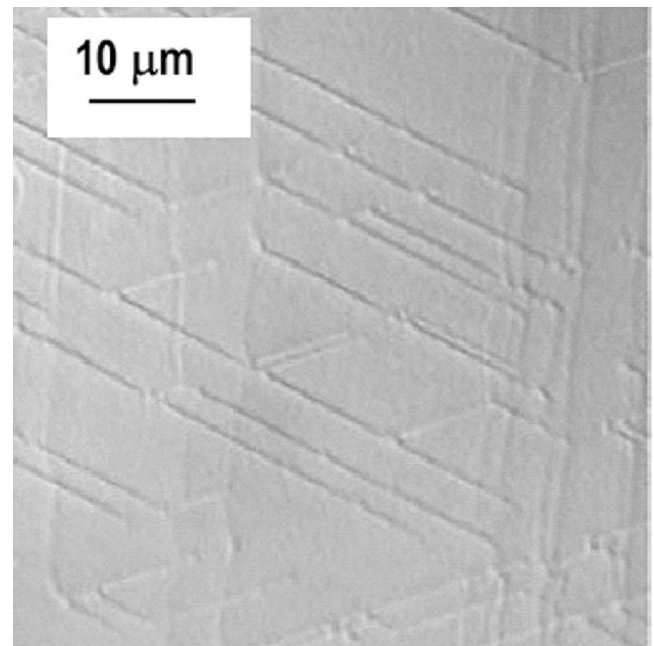

Fig. 4. The Nomarski optical-microscope image of a dislocation-etched HgCdTe epilayer that was etched after annealing.

430°C for 10 min. The layer was grown with a cap thickness below the critical thickness for the Δx between the absorber and the cap layer. Misfit-dislocation lines are evident along the crystallographic-slip planes. Prior to annealing, no misfit lines were observed after decorative dislocation etching. Because of the low temperatures used during MBE growth the "as-grown" layer exists in a state of strain. This state of strain in the as-grown layer has been observed in the past using wafer-level curvature measurements before and after annealing. During high-temperature annealing, the layer relaxes via the formation of misfit dislocations at both the substrate/absorber interface and at the absorber/cap interface. The misfit-dislocation lines are evident in the image along the [−231] and [−213] slip directions, even though the layer thickness was thinner than the theoretical critical thickness. Critical-thickness calculations are based on the lattice mismatch between a relaxed-absorber layer and a thin strained-cap layer.[14] However, the as-grown layer is known to exist in a state of stress, and consequently, the assumption that the absorber layer is relaxed is incorrect. Therefore, the actual critical thickness is significantly less than the theoretical calculations imply.

A second phenomenon was observed in the experimentally grown HgCdTe layers when misfit dislocations were observed at the cap/absorber interface. The misfit dislocations that typically form along one of the three dominant crystallographic directions during annealing can bend out of plane, glide along the absorber/cap interface, and getter to regions of high stress (defects) in the material. Figure 5 shows an experimentally grown HgCdTe layer that has been annealed and etched similar to the sample in Fig. 4. Figure 5 shows a misfit dislocation that has bent out of plane during annealing and gettered to a void defect. This gettering of dislocations to defects increases the effective dislocation density around the defect after annealing and raises a significant point. If the strain field of a defect can exert a force on a dislocation and pull it out of plane, then a process-induced strain field should do the same.

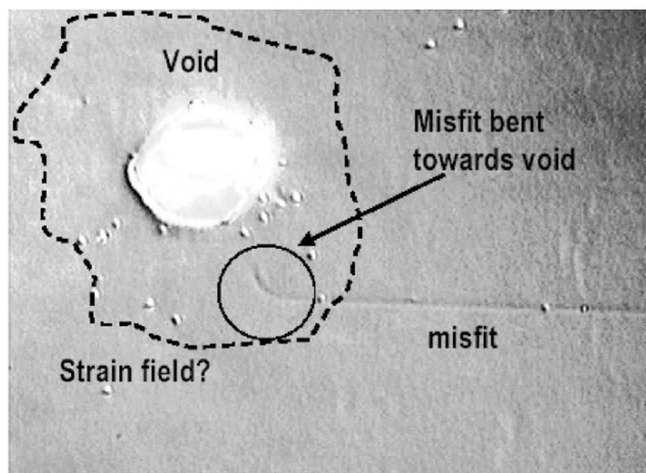

Fig. 5. The Nomarski image of a misfit dislocation that has bent out of the slip plane during a high-temperature anneal and gettered to a void.

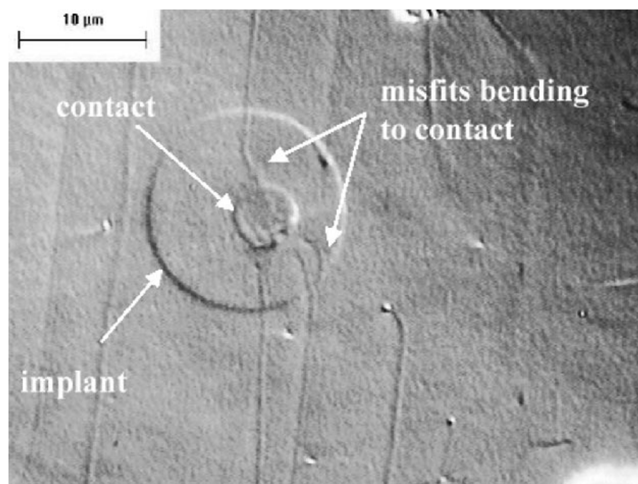

Fig. 6. The Nomarski image of a stripped diode showing the implant and contact region. Note the dislocations have gettered to the region of high stress around the contact.

Figure 6 shows an experimental diode that was fabricated to test whether implantation via etching and annealing can cause misfit dislocations to getter to the diode region. The experimental diode was stripped and dislocation etched to reveal both threading and misfit dislocations. The misfit dislocations near the diode region bend out of plane and getter to the diode region. This gettering of dislocations increases the density of dislocations in the diode region. Because the dislocations that getter to the diode region have a misfit component at the cap/absorber interface, the dislocation intersects a significantly larger area of the diode than if the dislocation was exclusively threading in nature and perpendicular to the epitaxial surface. This is an important point because most decorative dislocation etches are deep etches that remove any evidence of misfit dislocations near the surface of the epitaxial layer and identify only the threading component of the dislocation. Therefore, the total lateral area of the diode consumed by a dislocation can be significantly greater than when only threading dislocations are present.

The annealed, stripped, and etched diode samples show that misfit dislocations crossing the junction do not always terminate within the junction or on the perimeter of the junction. Some of the misfit dislocations cross the junction without terminating (Fig. 7). Consequently, the number of dislocations in the junction region can be significantly higher than the number that would be reported simply by counting the pits formed by etching. Another important point to note is that the misfit segments intersecting the junction cover a larger area of the junction than the threading segments; thus, the misfit segment may have a larger impact on device performance than the threading segments. This is important because most

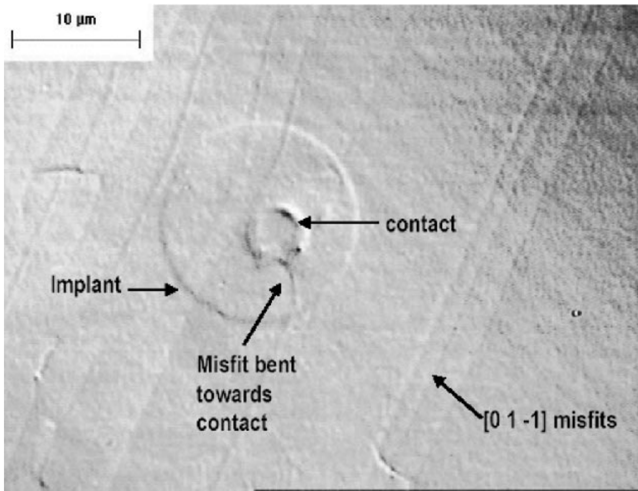

Fig. 7. The stripped and dislocation-etched experimental diode showing several misfit dislocations crossing the diode region without terminating. Consequently, there is no etch pit associated with the dislocation within the diode region, even though the dislocation clearly crosses the diode.

dislocation studies on the degradation of diode performance in HgCdTe devices attempt to correlate diode performance to the density of dislocations threading through or near the junction area perpendicular to the device surface (threading dislocations).[1–5] These studies ignore the possible influence of misfit dislocations that may form along the junction interface at the absorber/cap interface parallel to the surface of the epitaxial layer. Consequently, many diodes may have dislocation densities that are much greater than the density calculated by counting the EPD in the diode area. Therefore, a direct correlation between dislocations in the junction area and the performance of the corresponding diode is not possible by counting etch pits alone. The influence of misfit dislocations within the metallurgical junction must be accounted for when attempting to correlate diode performance directly to the number of dislocations intersecting an individual diode.

The processed-induced strain fields around the contact hole via the implant edge exert a force on the threading dislocations that are oriented perpendicular to the top surface of the material. This force is similar in nature to the image force that a dislocation feels near a free surface sidewall, such as in a mesa structure.[37,38] The image force (F) exerted on a threading dislocation near a free surface can be approximated as

$$F \approx \frac{\mu b^2}{4\pi r} \tag{3}$$

where b is the Burger's vector, μ is the shear modulus, and r is the distance from the sidewall. The validity of the approximations used to obtain Eq. 3 are not crucial, rather it is the 1/r functional dependence that is of interest. Equation 3 shows that the force felt by a dislocation some distance, r, from the sidewall decreases as 1/r. This implies that at some critical distance (r_c) from the sidewall, the force acting on the dislocation will decrease to a level below the frictional forces seeking to keep the dislocation stationary.[39,40] Consequently, for the diodes shown in Figs. 6 and 7, threading dislocations with distances greater than some critical distance r_c cannot bend out of plane and getter to the junction region. The exact nature (geometry, magnitude, sign, and local variations) of the strain field associated with the various process steps in HgCdTe-diode formation is not well understood. Consequently, calculating the critical-gettering radius, r_c, for dislocations near HgCdTe diodes is not trivial. However, from our observations, dislocations within a few microns (2–3) of the diode (on the order of the critical thickness) are capable of gettering to the junction.

The misfit dislocations at the cap/absorber interface shown in Figs. 4–7 form during annealing, even though the thickness of the cap was less than the theoretically calculated critical thickness for the lattice mismatch (Δx) between absorber and the cap layer. This is a result of the absorber layer being strained during growth, causing the equilibrium critical-thickness calculations to be in error. A test structure in which the Δx between the cap and the absorber layer was reduced significantly below the critical thickness accounted for accumulated strain in the absorber layer. Figure 8 shows an annealed and dislocation-etched sample where the Δx of the cap was reduced to eliminate misfit dislocations. The reduced Δx at the cap interface resulted in zero misfit dislocations at the cap/absorber interface. Compare Fig. 8 with Fig. 4. Figure 4 shows an annealed and etched epitaxial layer where a cap Δx was used without consideration of the additional strain in the absorber layer. Figure 8 reveals clearly that the misfits can be eliminated at the cap simply by designing a cap structure that accounts for the accumulated strain in the growing epitaxial layer.

Strain can play a crucial role in performance degradation in thin-film, epitaxial-HgCdTe diodes.[41–43]

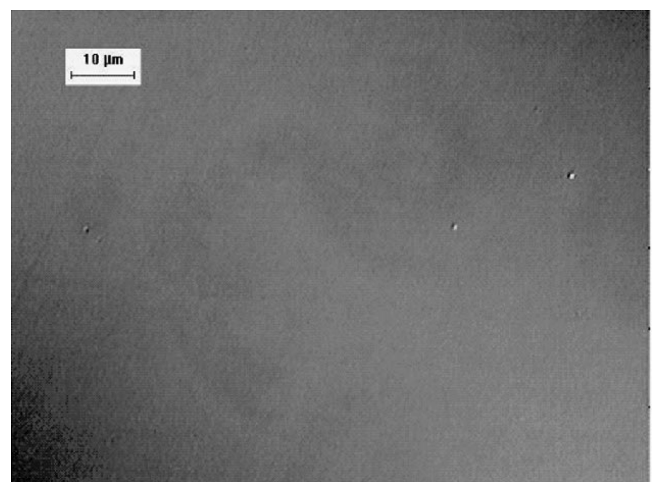

Fig. 8. The Nomarski image of the annealed and dislocation-etched sample with cap modified to eliminate misfits at the cap/absorber interface.

Although this work has focused on misfit dislocations, the same process-induced strain fields around the junction area can result in piezoelectric-effect degradation, strain-induced point-defect tunnel currents, and strain-enhanced impurity gettering to the junction; all of which can significantly degrade the ultimate performance of HgCdTe IR detectors.[41–44] Work continues on the direct correlation between misfit dislocations at the cap interface and the resulting degradation of diode performance. The fundamental question still unresolved is whether misfit dislocations crossing the diode region impact diode performance in an observably different way than threading dislocations oriented perpendicular to the epitaxial-layer surface. Not clear also is how misfit dislocations that terminate within the diode differ from misfits that pass through the diode and terminate outside the diode region. Understanding the stress distribution in an epitaxial layer and managing the stress accumulation and relaxation during layer growth and device processing are crucial to limiting strain-induced degradation of detector performance.

CONCLUSIONS

Misfit dislocations are capable of forming at the cap/absorber interface when the cap thickness is less than the theoretical critical thickness (based on the Δx between the two epitaxial layers). The strain energy stored in the growing absorber layer is believed not to be fully relaxed by crosshatch-pattern formation or the formation of misfit dislocations at the substrate/epilayer interface. Consequently, misfit dislocations can form at the cap interface by the bending over of threading dislocations or the nucleation of surface half-loop dislocations. These dislocations become mobile at elevated-processing temperatures and getter to regions of high stress in the epitaxial layer. These regions of high stress can be natural and can include voids or other defects typically found in the epitaxial layer, or they can be process-induced regions, such as the implant area, the contact metal, or via opening. The net result is that the dislocation density in the detector region can be significantly greater than the density of dislocations reported for the as-grown epitaxial layer. The misfit dislocations located at the cap/absorber interface can be eliminated by reducing the Δx at the cap/absorber interface to account for the strain accumulated during growth in the absorber layer.

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