Comparison of GaAs Grown on Standard Si (511) and Compliant SOI (511)

M.L. SEAFORD,[1] D.H. TOMICH,[1] K.G. EYINK,[1] L. GRAZULIS,[1] K. MAHALINGHAM,[1] Z. YANG,[2,3] and W.I. WANG[2]

1.—Air Force Research Laboratory, Materials and Manufacturing Directorate, WPAFB, OH 45433-7707. 2.—Columbia University, Department of Electrical Engineering, NYC, NY 10027. 3.—Present address: IBM Microelectronics Division, Hopewell Junction, NY 12533

Gallium arsenide (GaAs) films were grown by molecular beam epitaxy (MBE) on a (511) silicon substrate and a compliant (511) silicon-on-insulator (SOI) substrate. The top silicon layer of the compliant (511) SOI was thinned to ~1000 Å. The five inch diameter SOI wafer was created by wafer bonding. The GaAs (004) x-ray diffraction (XRD) reflection showed a 25% reduction in the full width half maximum (FWHM) for GaAs on a compliant (511) SOI as compared to GaAs on a silicon substrate. Cross section transmission electron microscopy (XTEM) clearly indicates a different dislocation structure for the two substrates. The threading dislocation density is reduced by at least an order of magnitude in the compliant (511) SOI as compared to the (511) silicon. XTEM found dislocations and damage was generated in the top silicon layer of the compliant SOI substrate after GaAs growth.

Key words: GaAs, SOI substrate, Si substrate, compliant

INTRODUCTION

From the time molecular beam epitaxy first demonstrated growth of compound semiconductors, the ability to grow these high quality compound semiconductors on silicon substrates has been sought. Unlu et al.[1] provides an overview for the motivation and advantages on the growth of gallium arsenide (GaAs) based devices on silicon substrates. The growth of compound semiconductors on silicon substrates would allow optical emitter and detector technology to be integrated with silicon technology. In addition, the benefits of other device specific components such as HEMTs, HBTs, etc. could be incorporated into silicon circuitry.

There are three main limiting issues that must be addressed for compound semiconductors to be grown on silicon. These issues are lattice mismatch, anti-phase domains, and thermal expansion mismatch. The first issue of lattice mismatch is very well documented. The ~4% lattice mismatch between the GaAs and silicon lattice constants will result in dislocations beyond a critical thickness. Unfortunately, a fraction of these dislocations are threading dislocations that will propagate into the epitaxial layers. This results in a high density of defects in the active region of compound semiconductor devices grown on silicon substrates. These defects limit the optical and electrical quality of these materials. The second issue of concern is the creation of anti-phase domains when the polar GaAs material is grown on the non-polar silicon substrates. When growth of GaAs is initiated on the silicon substrate, there are regions where gallium and other regions where arsenic nucleate first. When the regions coalesce, this difference in nucleation results in Ga to Ga and As to As bonds. The Ga to Ga and As to As provide an excess positive and excess negative charge, respectively. These regions, termed anti-phase domains (APDs), continue from the growth front into the active regions of the device. High quality compound semiconductor layers are prevented by the presence of the interfaces between the APDs. The third issue of concern is the difference in the thermal expansion coefficients of GaAs and silicon. The coefficients of GaAs and silicon at room temperature are 6.8×10^{-6}/K and 2.6×10^{-6}/K, respectively. When the GaAs growth is finished and the substrate temperature is reduced from ~600°C to room temperature, this difference in thermal expansion results in added stress. The compound semiconductor layers are put under tensile stress which can result in warpage, dislocations, or cracking.[2]

Previous research has shown compound semiconductors grown on high index (N11) silicon substrates

(Received September 19, 1999; accepted March 30, 2000)

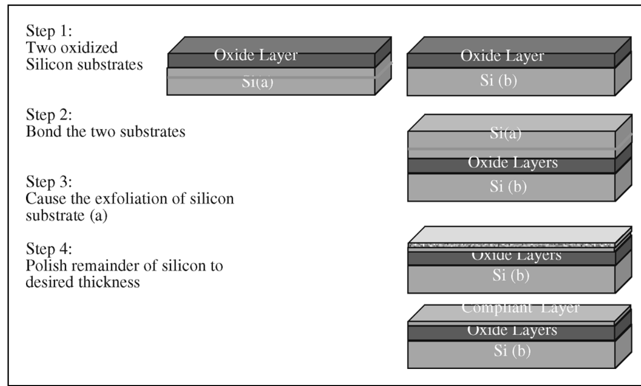


Fig. 1. Process diagram for creating a compliant SOI substrate.

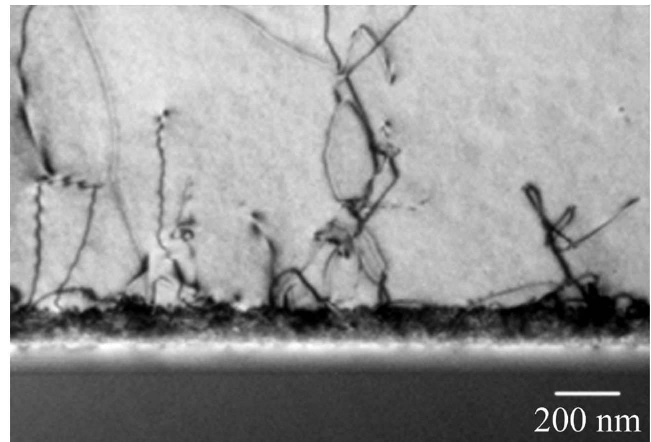
resulted in reduced APD formation.[3,4] This improvement in material has been attributed to the shortened (100) terraces formed by the miscut towards the (011). In addition, the misorientation results in a high density of (100) terraces with double atomic steps. The reduction in the APD density has been attributed to the formation of the double atomic steps in conjunction with an arsenic prelayer prior to GaAs growth.[1]

Compliant substrates have been used to address the issue of lattice mismatch. Gallium antimonide (GaSb) and indium antimonide (InSb) have been shown to have reduced threading dislocation density when grown on a GaAs based compliant substrate.[5] These layers represented a 8% and 15% lattice mismatch, respectively.

A compliant SOI substrate was used to address the issues of lattice mismatch and differing thermal expansion coefficients. Previously, Wang et al.[6] demonstrated that a thick $Si_{0.6}Ge_{0.4}$ layer could be grown on compliant SOI. Transmission electron microscopy of the SiGe layer found a reduced threading dislocation density. This layer would have a lattice constant of 5.517 Å and a thermal expansion coefficient of 3.9×10^{-6}. Since the top silicon layer (compliant layer) is very thin (~200 Å), the usual assumption made for calculating the Matthews-Blakeslee[7] critical layer thickness is no longer valid. Models[8,9] which account for the finite "substrate" layer thickness can be used to determine the amount of stress applied to the compliant layer. The dislocations due to this stress in the compliant layer have been seen previously.[5] Prior work[10,11] on GaAs growth on SOI substrates used very thick (>0.5 μm) top silicon layers.

EXPERIMENT

High index (511) substrates were chosen to reduce APD formation. The (511) direction represents a tilt towards the (011) from the (100) of ~15.8°. The SOI substrate was purchased from SOITEC. The process used to create the SOI substrates is given in Fig. 1. The top silicon layer thickness was 1000 Å and the buried oxide thickness was 4000 Å. A surface roughness of <2 Å for a 2 μm by 2 μm area and a dislocation density in the final silicon layer of <100 cm^{-2} was specified. Identical cleaning and surface preparation was used for both substrates.



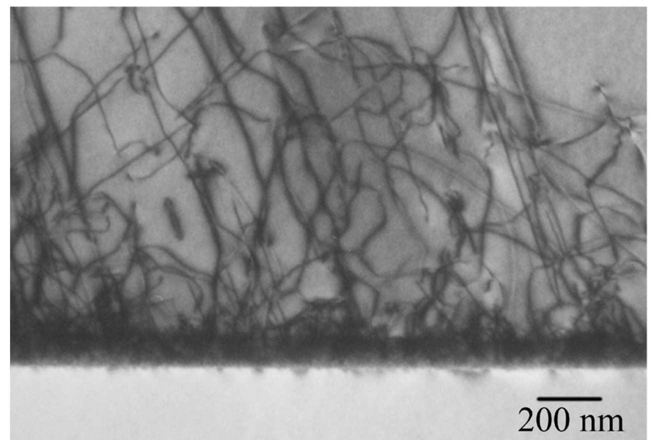


Fig. 2. Cross sectional TEM comparison of GaAs film grown on (upper) compliant (511) SOI and (lower) standard (511) silicon substrate.

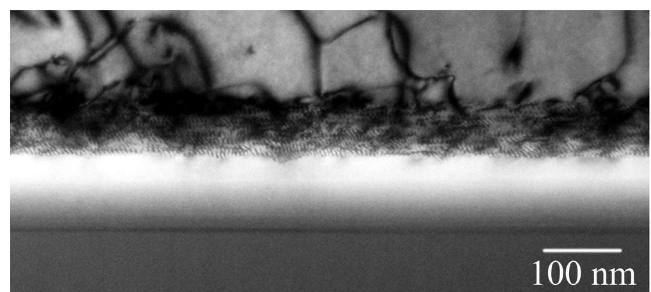


Fig. 3. Cross sectional TEM of compliant 1000 Å silicon layer.

Solid source MBE was used to grow a GaAs film directly on a compliant (511) SOI substrate and a control (511) silicon substrate. The GaAs film was growth at ~580°C at a rate of ~1 μm/h. Selective etching was used to locate APDs. A Philips MRD system was used to perform the x-ray diffraction (XRD) with a 0.45 mm receiving slit. Cross-sectional samples were prepared by ion-milling using a GATAN-precision ion polishing system. TEM observations were performed using a PHILIPS-CM200 TEM operated at 200 kV. Bright-field images were obtained under two-beam conditions with G = 220.

RESULTS AND DISCUSSIONS

The thickness as measured by TEM of the GaAs films was ~4 μm on both types of substrates. Selective

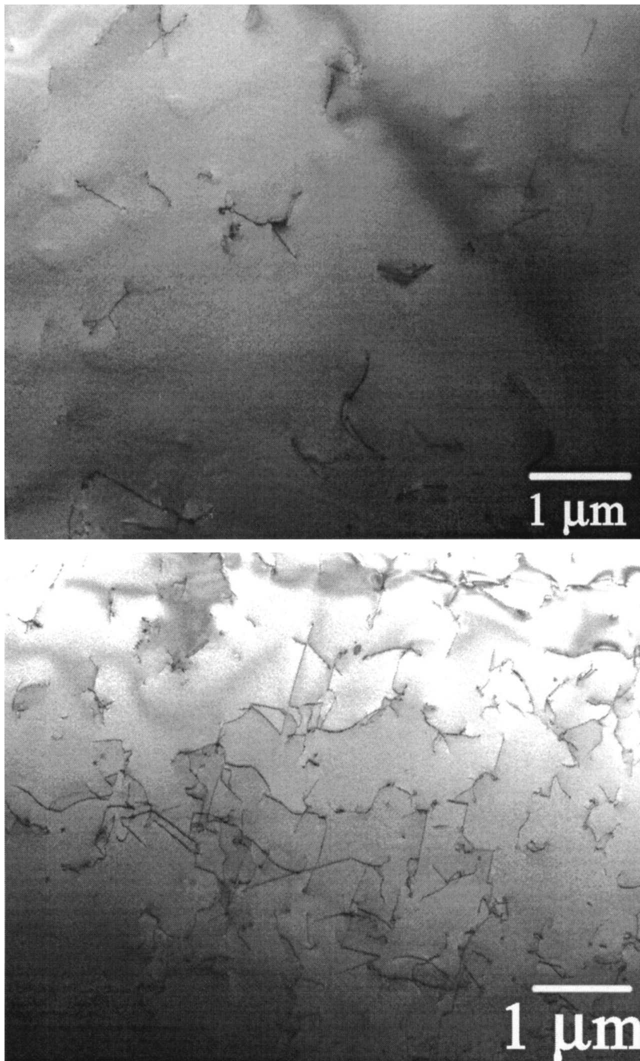


Fig. 4. Plan view TEM comparison of GaAs film grown on (upper) compliant (511) SOI and (lower) standard (511) silicon substrate.

etching of GaAs films grown on either substrate found no evidence of APDs, consistent with other reports[12] of compound semiconductors grown on miscut silicon substrates. The full width at half maximum (FWHM) of the GaAs (004) XRD peak was consistently more narrow for the GaAs grown on the compliant SOI (511) as compared to the standard silicon (511). The FWHM was 150 arcsecs and 200 arcsecs on average for the GaAs on compliant (511) SOI and (511) silicon, respectively. Cross sectional TEM images of the GaAs films are shown in Fig. 2. Figure 2a shows the GaAs film grown on the compliant (511) SOI substrate. While there are dislocations in both samples, the common 60° threading dislocations which are easily seen in Fig. 2b are not present. The dislocations in Fig. 2a also appear to be denser initially and decrease abruptly at about 1000 Å. Above this thickness, the dislocations are numerable and only slowly reduce in density. Figure 3 shows a magnified view of the top 1000 Å silicon layer. The surface of the SOI substrate previously had a surface roughness of less than 2 Å on 2 μm by 2 μm area. The silicon layer thickness in Fig. 3 appears to vary in thickness by about 100 Å. Prior to growth of the GaAs layer, the silicon layer was very uniform with only approximately 2 Å surface roughness. In addition, numerous dislocations are seen in the thin silicon layer. These dislocations were not seen in the top silicon layer prior to growth of the GaAs. The creation of dislocations and increase in surface roughness indicate relaxation occurred within this 1000 Å silicon layer. A comparison of plan view TEM is shown in Fig. 4. There is an approximately three order of magnitude reduction in threading dislocation density. These results suggest that the thickness of compliant (511) SOI layer, which was 0.1 microns in the present case, must be further reduced.

CONCLUSIONS

GaAs films were grown by MBE on (511) silicon and compliant (511) SOI substrates. TEM characterization showed a reduced threading dislocation density for the GaAs grown on the compliant (511) SOI. After the growth of the GaAs layer, the compliant layer of the SOI substrate had threading dislocations and very large surface roughness (~100 Å). Before growth, no threading dislocations were expected or observed in the bonded SOI wafer. In addition, before growth the surface roughness was ~2 Å for a 2 μm by 2 μm area. X ray diffraction measurements consistently found an approximately 25% reduction in the (004) FWHM for the GaAs layer grown on the compliant (511) SOI and compared to the (511) silicon substrate. The thickness of the compliant layer will be reduced to further decrease the threading dislocation density.

REFERENCES

1. H. Unlu, H. Morkoc, and S. Iyer, *Gallium Arsenide Technology,* Vol. II, (Indianapolis, IN: Howard W. Sams & Company, 1990).
2. R. Fischer, H. Morkoc. D. Neumann, H. Zabel, C. Choi, N. Otsuka, M. Longerbone, and L.P. Erickson, *J. Appl. Phys.* 60, 1640 (1986).
3. K. Longgenbach and W. Wang, *Appl. Phys. Lett.* 59, 2427 (1991).
4. I.W. Tao and W. Wang, *J. Vac. Sci. Tech.* B13, 731 (1995).
5. M.L. Seaford, P.J. Hesse, D.H. Tomich, and K.G. Eyink, *J. Electron. Mater.* 28, 878 (1999).
6. Z. Yang, J. Alperin, W.I. Wang, S.S. Iyer, T. S. Kuan, and F. Semendy, *J. Vac. Sci. Tech.* B16, 1489 (1998).
7. J.W. Matthews and A.E. Blakeslee, *J. Cryst. Growth* 27, 188 (1974).
8. L.B Freund and W.D. Nix, *Appl. Phys. Lett.* 69, 173 (1996).
9. T.-Y. Zhang and T.-J. Su, *Appl. Phys. Lett.* 74, 1689 (1999).
10. S.J. Pearton, S.M. Vernon, K.T. Short, J.M. Brown, C.R. Abernathy, R. Caruso, S.N.G. Chu, V.E. Haven, and S.N. Bunker, *Appl. Phys. Lett.* V51, 1188 (1987).
11. S.J. Pearton, C.R. Abernathy, R. Caruso, S.M. Vernon, K.T. Short, J.M. Brown, S.N.G. Chu, M. Stavola, and V.E. Haven, *J. Appl. Phys.* 63, 775 (1988).
12. H.B. Kroemer, *Proc. Mater. Res. Soc.* 67, 3 (1986).