Die Bonding with Au/In Isothermal Solidification Technique

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A gold-indium isothermal solidification technique has been developed for die bonding. Both silicon on silicon and silicon on alloy 42 (chip size 2×2 mm^2) are investigated. For silicon on silicon, the bonding is performed at 200°C within 30 sec. The bonds can withstand 1,500 cycles of temperature cycle between –65°C and 150°C without any degradation. For silicon on alloy 42, the bonding is done at 250°C within 5 sec. The bonds can pass the shear strength test specified by MIL STD 883D, Method 2019.5. The reliability of the bonds is evaluated by thermal cycle testing. After 500 cycles between –65°C and 150°C, only slight degradation was observed.

Key words: Au/In, die bonding, shear strength

INTRODUCTION

Die bonding is an important step for electronic packaging. The bonding layer provides mechanical support, heat dissipation and current conduction (ground) in some cases. Thus it has an important role in device performance and reliability. Metal filled epoxy (for example silver paste), soft solder (Pb/Sn for example) and hard solder (Au/Si for example) are commonly used for die bonding processes. Each process has its own advantages and disadvantages. Isothermal solidification (sometimes called SLID—solid liquid interdiffusion, referred to as IS hereafter) has been considered as a promising alternative for die bonding. The principle is elucidated by Leonard Bernstein.[1] Two metallic layers with respectively high and low melting points are brought together into intimate contact (the high melting point element will be referred to as HI representing its high melting temperature and the low melting point element will be referred to as HO hereafter). By raising the temperature above the melting point of element LO, inter-diffusion takes place between the two elements, forming an intermetallic phase whose re-melting temperature may be much higher than the melting point of the element LO. Besides offering some benefits as other hard solders, the bonds made by isothermal solidification (referred to as IS bonds hereafter) possesses another two advantages: (1) they are fluxless and (2) they have the capability of low temperature bonding and high temperature utilization. The first advantage is attractive for die bonding of photo-electronic devices where flux is undesirable. The second advantage is also important for conventional packaging techniques where the highest temperature of each assembly step is limited by previous steps to prevent bond re-melting (hierarchical soldering). The IS technique eliminates this concern. Furthermore with the rapid development of high temperature devices like SiC, the IS process may play an important role for die attachment as most of the existing die attach media can no longer withstand the high operating temperature of these devices. There are a number of possible candidates[1–3] for IS application, including Au/In and Ag/In. Both systems are well known for their rapid diffusivities.[4] There are a number of papers[5–10] that focus on fundamental or application issues of these metal systems.

Chin et al.[5] has reported results on the Au/In bonding with evaporated multilayer structures. A thin gold layer of 0.3 μm was deposited on the 6.5 μm indium layer to prevent it from being oxidized. The bonding process was done in flowing hydrogen at 200°C for 10 min with static pressure of 10.4 MPa applied to the die. High quality bonding was achieved with bond re-melting temperature greater than 545°C. Mori et al.[6] reported Au/In application for flip-chip attachment of LCD (liquid crystal display). Limita-

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tions of the liquid crystal necessitated the bonding to be performed a temperature lower than 150°C, resulting a process governed by solid state diffusion. Pressure was applied to assist the bonding. Chen et al.[11] reported a silver-indium bonding process. Deposition was performed in a vacuum to form the multi-layers. The bonding was performed in an inert environment to inhibit oxidation. High quality bonds were obtained with excessive indium in the bonding layer, so that they are not suitable for high temperature application.

It is clear that the main obstacle to overcome is the oxidation of indium. In most cases, multilayers are manufactured by deposition in vacuum. Also, a thin layer of gold or silver is normally deposited on top of the indium layer to protect the indium from being oxidized by the formation of an $AuIn_2$ or $AgIn_2$ phases. Bonding is done in inert or even reducing atmosphere. Although high quality bonds can be made, drawbacks include that the technique for multilayer deposition is costly compared to galvanic deposition or chemical plating, and the complex configuration of multilayer structures has to be used and strict bonding environment is necessary, it is difficult for any realistic application for mass production.

In this paper, a Au/In IS process is investigated. The research includes practical issues in production such as process costs, assembly time, compatibility with current die bonding techniques. Some of the results are presented in the flowing sections.

EXPERIMENTAL PROCEDURES

Four-inch silicon wafers were used for the chip material. A 1000 Å gold layer was deposited by electron beam evaporation, with 1000 Å titanium used as the adhesion and barrier layer. The indium layer of 3–5 μm was galvanically deposited on the gold layer. The wafer was diced into individual chips with a dimension of 2×2 mm^2. After wafer sawing, the individual dice were thoroughly cleaned.

Silicon and alloy 42 were used as substrates. For the silicon substrate, after the deposition of Au1000 A/Ti1000 Å, the gold layer was thickened to ~2 μm by chemical plating. The purpose of this silicon on silicon process is to examine the feasibility of the Au/In IS bonding (compared to alloy 42, the silicon substrate has a smoother surface and no CTE mismatch with the chip. Thus it provides an ideal case which should be easier to implement). This process may also be applicable for MCM-D (multi-chip module–deposit) if silicon is used as the substrate material. For alloy 42, 2 μm gold layer was made by galvanic deposition with nickel as adhesion layer.

For the bonding process, the substrates were heated to a temperature between 200°C (silicon on silicon) and 250°C (silicon on alloy 42). The indium coated chip was picked and placed on the substrate with a load of 1.25 N/mm^2 (the fact that indium was coated on the chip side but not on the substrate side minimizes the indium oxidation during assembly as the chip was picked up cold). A mechanical movement of the bond

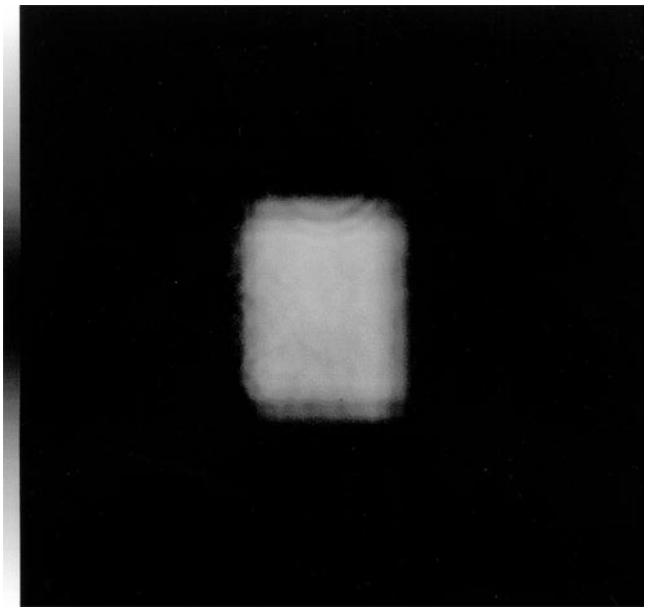


Fig. 1. C-SAM image of an Au/In IS bond (silicon on silicon, bonding temperature 200°C, reaction time ~30 s).

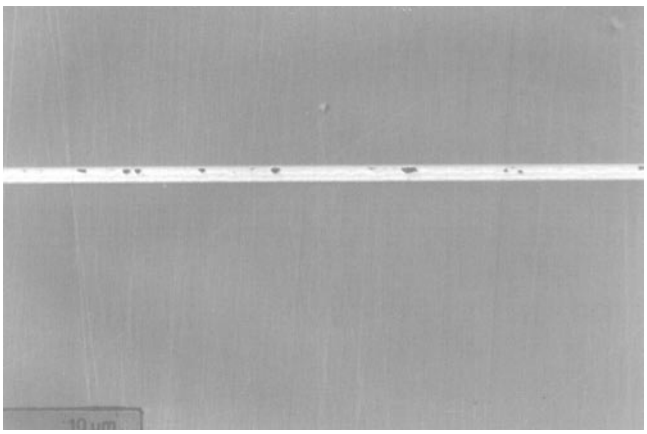


Fig. 2. Cross section of an Au/In IS bond (silicon on silicon, bonding temperature 200°C, reaction time ~30 s.)

tool (about several hundreds of a miniseconds) was immediately activated to initiate the wetting between gold and indium. The load was relieved and the chip remained on the hot stage for some time before cooling down for the gold and indium to react (the time for pick, and place and mechanical agitation is referred to as assembly time, the annealing time after relieving the load is referred to as reaction time hereafter). The minimum reaction time was defined by the duration at the bonding temperature after which the chip can not be easily removed from the substrate with a pincette. This was determined experimentally. Nitrogen flow (~0.5 l/min) was provided (using a bracket to blow nitrogen) during all the bonding process to reduce the oxidation.

Scanning acoustic microscope was used to check the bonding quality. The 100 Mhz transducer provides a lateral resolution of ~38 μm and a depth resolution of ~25 μm. The detailed microstructure was investigated metallographically. Die shear test

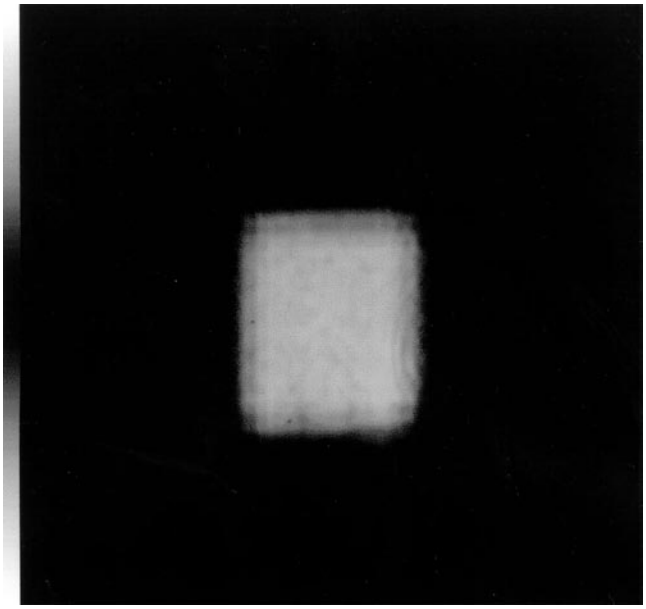


Fig. 3. C-SAM image of an Au/In bond after 1,503 cycles test between –65°C to 150°C (silicon on silicon, bonding temperature 200°C, reaction time ~30 s.).

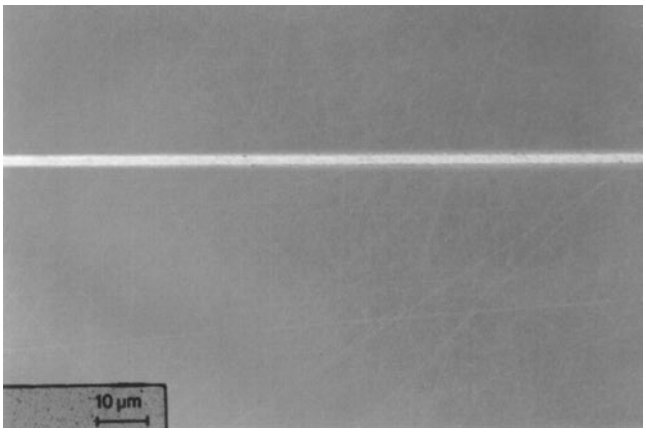


Fig. 4. Cross section of an Au/In IS bond after 1,503 cycles test between –65°C to 150°C (silicon on silicon, bonding temperature 200°C, reaction time ~30 s.).

was performed in accordance to MIL STD 883D, Method 2019.5. The reliability of the bonds was evaluated by thermal cycling between –65°C and 150°C.

RESULTS

Silicon Chip Bonding on Silicon Substrate

For silicon chip bonding on silicon substrate, the thickness of indium layer is ~4.7 µm. The bonding process was done at 200°C. The minimum reaction time was estimated experimentally to be ~30 sec. Figure 1 shows the acoustic image after bonding. A very homogeneous bond is produced. Figure 2 shows the cross section of the die bond. The thickness of the bond region is ~5 µm. Several sub-layers are discernible. During Au/In reaction, $AuIn_2$ is always the first phase to form at the interface. As reaction proceeds, the thickness of the $AuIn_2$ phase increases, and other gold rich phases such as AuIn, Au_9In_4 may appear,

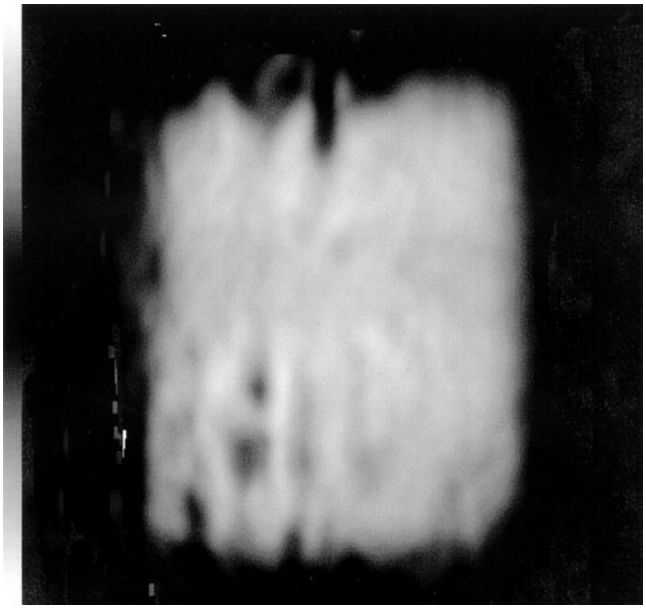


Fig. 5. C-SAM image of a typical Au/In IS bond (silicon on alloy 42, bonding temperature 250°C, reaction time ~5 s).

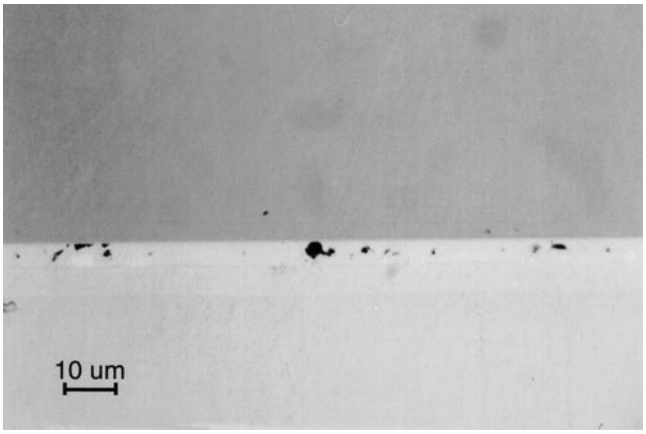


Fig. 6. Cross section of a typical Au/In IS bond (silicon on alloy 42, bonding temperature 250°C, reaction time ~5 s.)

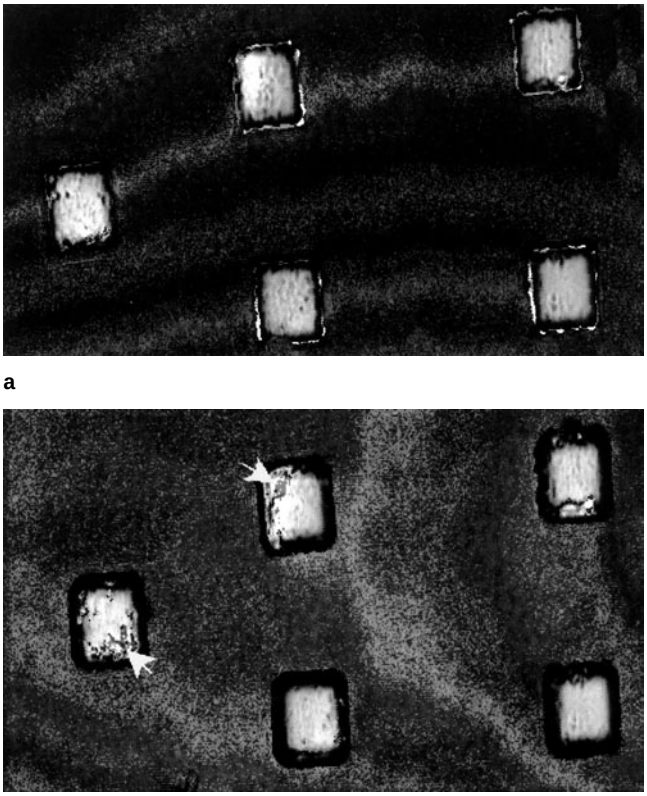
depending on the thickness of the multi-layers. The reaction process often results in the formation of sub-layer structures. With sufficient annealing time, solid state diffusion and phase transformation will happen until the equilibrium in the phase diagram is achieved The existence of the multi-layers indicates that even though the liquid indium phase was consumed, the reaction has not reached the equilibrium. Small voids are detected in the bond layer, which seems to be caused by air entrapment in the bonding layer due to surface irregularities (due to galvanic plating) and the imperfect parallelism between the chip and the substrate.

The samples were subjected to thermal cycling to evaluate the reliability of the IS bonds. A two-chamber (a hot chamber and a cold chamber) test equipment was used. The test condition was –65°C to 150°C with 15 min dwell time at each chamber and the change over time between the chambers was ~10 sec. Figures 3 and 4 show the C-SAM image and cross

Table I. Summary of Shear Test Results

Shear Force f (N)	25≤ f < 35	35 ≤ f < 45	45 ≤ f < 55	55 ≤ f < 65	65 ≤ f < 75	75 ≤ f < 85	f > 85
Percentage (%)	22	27	30	5	8	5	3
(N1/N2)*	8/37	10/37	11/37	2/37	3/37	2/37	1/37

* N1 refers to the number of samples with shear strength in the specified range, N2 refers to the total amount of samples tested.



a

b

Fig. 7. C-SAM images of Au/In IS bonds before and after the thermal cycling tests (–65°C to 150°C for 500 cycles, silicon on alloy 42, bonding temperature 250°C, reaction time ~5 s, arrows show areas with slight degradation) (a) before the test, (b) after 500 cycles between –65°C and 150°C.

section picture of the bond, respectively after 1,503 cycles. No degradation was observed from acoustic investigation. Moreover, the sub-layer structures diminished and the interconnection was homogenized into a very uniform layer as a result of continued reaction during thermal cycle tests.

The results are excellent for silicon on silicon, but the application space for this system is limited. Thus a more practical system of silicon on alloy 42 was investigated.

Silicon Chip Bonding on Alloy 42 Substrate

In order to decrease the reaction time for silicon on alloy 42, the thickness of indium layer was reduced to ~3.5 μm, and the bonding temperature raised to 250°C. The minimum reaction time was estimated to be ~5 sec. Figure 5 displays the acoustic image for a typical sample. Again, homogeneous bonds can be obtained. Contrast variations in the image correspond to different phases (phase with higher gold content appears darker in the acoustic image). The detailed microstructure investigations are still going on. The results will be presented in a later paper.

Table II. CTEs of Some Important Materials Relevant to This Project

Material	Si	GaAs	6H-SiC	Alloy 42
CTE (RT, 10^{-6}/K)	2.8	5.7	4.8	5.9

Figure 6 shows the cross section picture. Unlike the IS bonds for silicon on silicon with clear sub-layer structures, the IS bond for silicon on alloy 42 is vertically homogeneous indicating that the reaction was completed during the bonding process due to the higher processing temperature and small thickness of indium film. Small voids were again observed in the bonding layer.

The results of die shear tests are summarized in Table I. All the samples pass the 25 N criteria required by MIL STD 883D, Method 2019.5.

The samples were subjected to thermal cycling between –65°C to 150°C. Ten samples were tested and all the samples have passed the 500 cycles. Figure 7 gives the C-SAM images of a typical example before and after thermal cycling. In Fig. 7a, some chips (the two chips to the upper left side of the image) showed bright acoustic contrast before the thermal cycling test, which were verified to be due to weak bonding. However, even these two poorly bonded chips survived the thermal cycling test, although the weakly bonded areas showed further degradation after the test (the bright regions looked brighter and the area expanded slightly, as indicated by arrows in Fig. 7b).

DISCUSSION

The multi-layer structure presented here is rather simple compared to other work. The gold layer on the substrate was produced by galvanic plating. On the chip side, before the indium plating, electron beam evaporation was used to deposit the barrier and adhesion layer of Ti/Au, but it should be possible to replace this step by chemical deposition of a nickel layer and a flash gold layer. As the equipment involved is inexpensive and the processes are simpler, thus the technique for fabricating the multi-layers should be inexpensive compared to previously reported work. The bonding process can be carried out on a commercial Au/Si eutectic bonder with small

modifications. The requirement on the bonding atmosphere is not excessively stringent. A bracket for blowing nitrogen is sufficient for the application. As described above, the assembly time required is less than one sec and the reaction time is approximately 5 sec for silicon on an alloy 42 substrate. By designing a temperature zone in the bonder, a very quick bonding process can be achieved (the reaction is guaranteed by allowing the sample to go through the temperature zone, so that the bonding can be performed one after another with full speed). Therefore the IS process developed here is very promising for mass production.

For industrial die bonding processes, the wafer is attached to an adhesive foil and then subjected to wafer sawing followed by die pick and place. It is undesirable to add an additional cleaning step after the die cutting process. In order to verify the effect of the adhesive, the same IS bonding process was tried without cleaning after dicing. No obvious detrimental effect was observed by scanning acoustic investigation.

Voids several microns in size were observed in the bonding layers for both silicon on silicon and silicon on alloy 42. The voids seem to be caused by air entrapment in the bonding layer due to surface irregularities. The assumption was supported by the experimental observation that the amount of voids decrease when smoother substrates were used (to be presented in a later paper).

Voiding is the most critical reliability concern for hard solder. In addition to many other detrimental effects, voids tend to produce stress on the backside of the die making it prone to cracking.[12,13] More investigation is needed to evaluate the effect of voids on the reliability of this Au/In IS process.

The CTEs of some important substrate materials are listed in Table II. From the table, it is clear that compared to GaAs and SiC, the CTE mismatch between silicon and alloy 42 is the highest. Thus bonds made by Au/In IS technique are expected to be even better for GaAs or SiC devices.

SUMMARY

Isothermal solidification is a promising technique for die attachment especially for high temperature devices. This paper discusses the results of Au/In IS bonding. The investigation takes into account some important issues for mass production. Silicon on silicon and silicon on alloy 42 were studied. The quality and reliability of the bonds are adequate for both systems. Although the investigation is done with silicon chip, the process should be also applicable for GaAs or SiC devices with even better reliability.

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