

High-Temperature Mechanical Integrity of Cu-Sn SLID Wafer-Level Bonds



THI-THUY LUU, NILS HOIVIK, KAIYING WANG, KNUT E. AASMUNDTVEIT,
and ASTRID-SOFIE B. VARDØY

Wafer-level Cu-Sn SLID (Solid-Liquid Interdiffusion)-bonded devices have been evaluated at high temperature. The bonding process was performed at 553 K (280 °C) and the mechanical integrity of the bonded samples was investigated at elevated temperatures. The die shear strength of Cu-Sn systems shows a constant behavior (42 MPa) for shear tests performed from room temperature [RT—298 K (25 °C)] to 573 K (300 °C). This confirms experimentally the high-temperature stability of Cu-Sn SLID bonding predicted from phase diagrams. The fractography of sheared samples indicates brittle-fracture mode for all samples shear tested from RT to 573 K (300 °C). The two dominating failure modes are Adhesive fracture between the Ti-W adhesion layer and the Si, and interface fracture at the original bond interface. This indicates that the bonding material itself is stronger than the observed shear strength values, and since these interfaces can be improved with process optimization even stronger bonds can be achieved. The presented work offers fundamental evidence of the Cu-Sn SLID bonding process for operating microelectronics and MEMS at high temperature.

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I. INTRODUCTION

SOLID-LIQUID interdiffusion (SLID) wafer-level bonding is an attractive processing technique for MEMS packaging and encapsulation, especially for devices which may operate at high temperatures. The bonding principle is based on rapid intermetallic compound (IMC) formation between two metal components; a low-melting component (In, Sn) and a high-melting component (Cu, Ag, Au).^[1–5] The bonding is performed at a temperature above the melting point of the low-melting component. During the bonding process, the high-melting component diffuses into the low-melting component and reacts to form solid IMCs with higher melting point. The final bond will thereafter consist of IMCs and any excess high-melting component metal. This enables the final bond to tolerate various applications that require operation at, or exposure to, high temperatures (HT).

For applications that require operating at high temperatures such as in automotive, aerospace, and petroleum industry, long-term reliability is critical due to the decline of material properties at high temperatures.^[6–9] It is important that the materials used in a bond-line have high-melting point and a high mechanical integrity at high temperatures without rapid diffusion of materials. To avoid the unwanted diffusion, it is strongly beneficial to

ensure thermodynamically stable bond-lines. Cu-Sn SLID wafer-level bonding is a promising technology for these applications, as it enables low-cost metallization, high mechanical strength^[2,10–12], and high-temperature stability. According to the Cu-Sn phase diagram, the final Cu/Cu₃Sn/Cu bond-line is thermodynamically stable, and the Cu₃Sn phase is solid up to 949 K (676 °C).

Reliability testing of Cu-Sn SLID wafer-level bonding in previous works has shown stable mechanical strength and reliable electrical properties during thermal cycling, high-temperature storage, and vibration at high-temperature tests.^[11,13–18] Although these tests were performed to prove the technology for high-temperature applications, the shear strength of the tested samples was all carried out at room temperature. Mechanical integrity at temperature surpassing the melting temperature of Sn has long been predicted, but experimental verification is scarce. In this study, the mechanical integrity of Cu-Sn SLID bonding was investigated at high temperature. The initial Cu-Sn thicknesses and the bonding process were designed to ensure a thermodynamically stable Cu/Cu₃Sn/Cu bond-line. The mechanical integrity of Cu-Sn bonded samples (shear strength and fractography) was investigated at shear test temperatures up to 573 K (300 °C).

II. EXPERIMENTAL SETUP AND DESIGN OF TEST VEHICLES

A. Fabrication

The design of the test vehicle is shown in Figure 1. We used 100-mm double side polished Si wafer with a 100-nm thick thermally grown SiO₂ layer. A 60-nm Ti-W

THI-THUY LUU, Researcher, NILS HOIVIK, KNUT E. AASMUNDTVEIT, and KAIYING WANG, Professors, are with the Department of Micro and Nanosystems Technology (IMST), Buskerud and Vestfold University College, Raveien 215, 3184 Borre, Norway. Contact e-mail: Thi.Luu@hbv.no ASTRID-SOFIE B. VARDØY, Research Scientist, is with the SINTEF ICT Instrumentation Department, Forskningsveien 1, 0373 Oslo, Norway.

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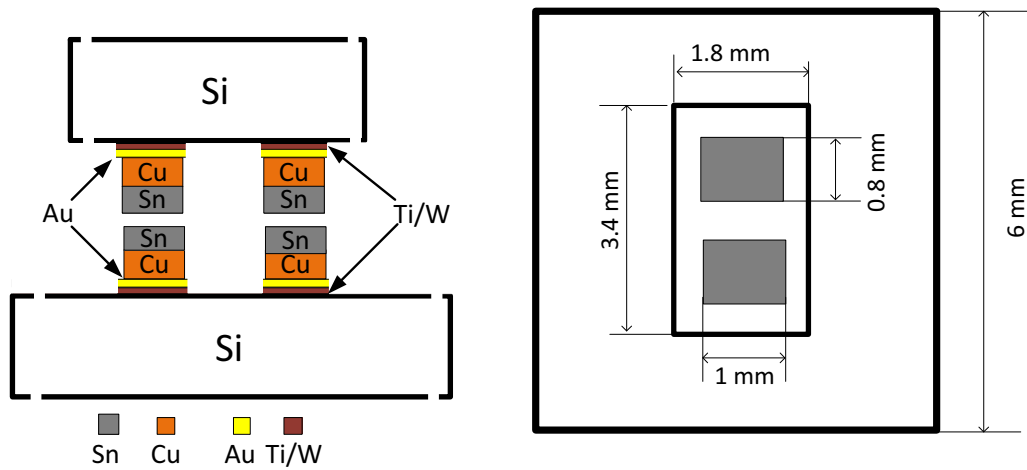


Fig. 1—Cross section and top view of test vehicle design of bond structure for high-temperature shear test. On each die, there are two bond pads with Au seed layer dimension of $0.8 \times 1 \text{ mm}^2$. The Cu and Sn are electroplated on the Au seed layer, using slightly smaller openings in the resist of $0.79 \times 0.99 \text{ mm}^2$. The overall substrate dimension is $6 \times 6 \text{ mm}^2$. The chip dimension is $1.8 \times 3.4 \text{ mm}^2$. Cu/Sn layer thicknesses are $4.5/1.0 \text{ }\mu\text{m}$.

adhesion layer is sputter deposited on one side of the wafer as the adhesion and barrier layer for Au. Lastly, an Au seed layer of $0.8 \text{ }\mu\text{m}$ was then sputter coated onto the Ti-W. The oxidized and sputter coated wafers were prepared and delivered by ACREO Swedish ICT. Both Cu and Sn are electroplated on the Au seed layer, where the photoresist mask opening for each pad measures $0.79 \times 0.99 \text{ mm}^2$. The Sn was electroplated immediately after Cu electroplating, in order to reduce oxidation of the Cu surface which might otherwise deteriorate the bond performance. For both Cu and Sn, a current density of 10 mA/cm^2 was used during electroplating process.

For Cu-Sn SLID wafer-level bonding, one of the concerns is the non-uniformity of the electroplated layer thicknesses which may cause un-bonded areas and result in lower yield or scattering of bond performance.^[19,20] In this study, the wafers were rotated during the electroplating process to improve the uniformity of Cu and Sn thicknesses.

In order to obtain a final Cu/Cu₃Sn/Cu bond-line, the thicknesses of Cu and Sn of 4.5 and $1.0 \text{ }\mu\text{m}$ were selected. After Cu and Sn electroplating, the Au seed layer was etched away using a KI + I₂ solution and the Ti-W adhesion layer was etched using H₂O₂ solution at 323 K ($50 \text{ }^\circ\text{C}$). Photoresist was used as the mask for Au and Ti-W etching, measuring slightly larger than Cu-Sn bond pads ($0.8 \times 1.0 \text{ mm}^2$) in order to compensate any misalignment.

The wafers were bonded at 553 K ($280 \text{ }^\circ\text{C}$) for 30 minutes to ensure that the reaction between Sn and Cu had come to completion.^[21] The bonding pressure used was 1.5 MPa . The bonded wafers were further diced into 124 separated test-dies, as shown in Figure 1, with top-die dimension of $1.8 \times 3.4 \text{ mm}^2$ and substrate dimension of $6 \times 6 \text{ mm}^2$ to fit the specialized die holder on the shear tester used in the experiments. A representative selection of bonded samples was later cross-sectioned and further polished using Ar ion milling before optical microscopy investigation.

B. Die Shear Testing

The samples were shear tested using a NordsonDage 4000Plus shear tester with 200 kg fload cartridge. The test height was $75 \text{ }\mu\text{m}$ above the substrate, and a test speed of $10 \text{ }\mu\text{m/s}$ was used. At each shear test temperature (room temperature [RT— 298 K ($25 \text{ }^\circ\text{C}$)], 273 K ($100 \text{ }^\circ\text{C}$), 473 K ($200 \text{ }^\circ\text{C}$), and 573 K ($300 \text{ }^\circ\text{C}$), nine samples were tested. For an indication of the variation in shear strength over the bonded wafer pair, samples from different regions of the wafer pair (center and edges) were selected for the shear test. The custom-made substrate holder is designed to efficiently transfer heat from the hot plate to the test sample.^[22] An illustration of the set up for shear testing configuration is shown in Figure 2.

Note how the device under test is fixed to the hot plate by the die holder, which was designed for a specific sample size to improve the uniformity of temperature during the test. The temperature of the hot plate is controlled by a proportional integral derivative (PID) controller. Further fractography of sheared samples was obtained using optical microscopy, scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDS), profilometry, and interferometry.

III. RESULTS

A. Microstructure of Bond Interface

After bonding, the dicing yield (the percentage of dies that survives the dicing process) is a good indication of the bond strength; a 100 pct dicing yield was obtained for the bonded wafer. Further cross-section analysis of the bond-line using optical microscope with 1000 times magnification is shown in Figure 3.

It can be seen clearly from the images that a single phase Cu₃Sn bond-line is sandwiched between two copper layers.^[21] The thicknesses of the Cu₃Sn IMC layer and total bond-line thickness vary with position on the bonded wafer pair, implying that the initial Cu and

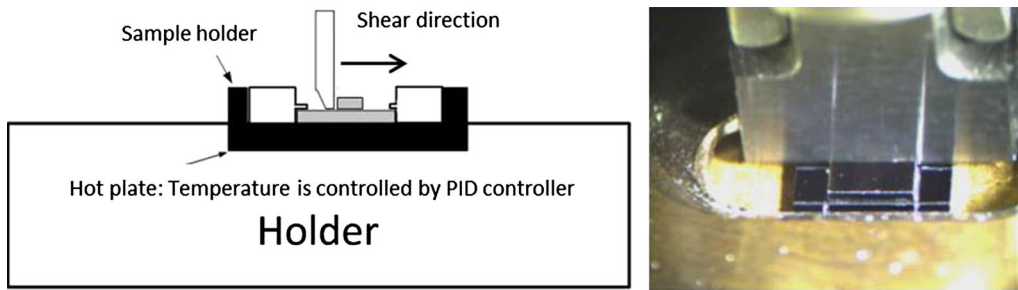


Fig. 2—Illustration of shear test configuration. The bonded sample is attached and clamped to the hot plate, using a custom sample holder. The holder is designed to efficiently transfer heat from the hot plate to the test sample. A PID controller controls the temperature of the hot plate. The entire temperature range was calibrated to ensure that the actual measured temperature on the hot plate matches the indicated temperature on the PID controller.

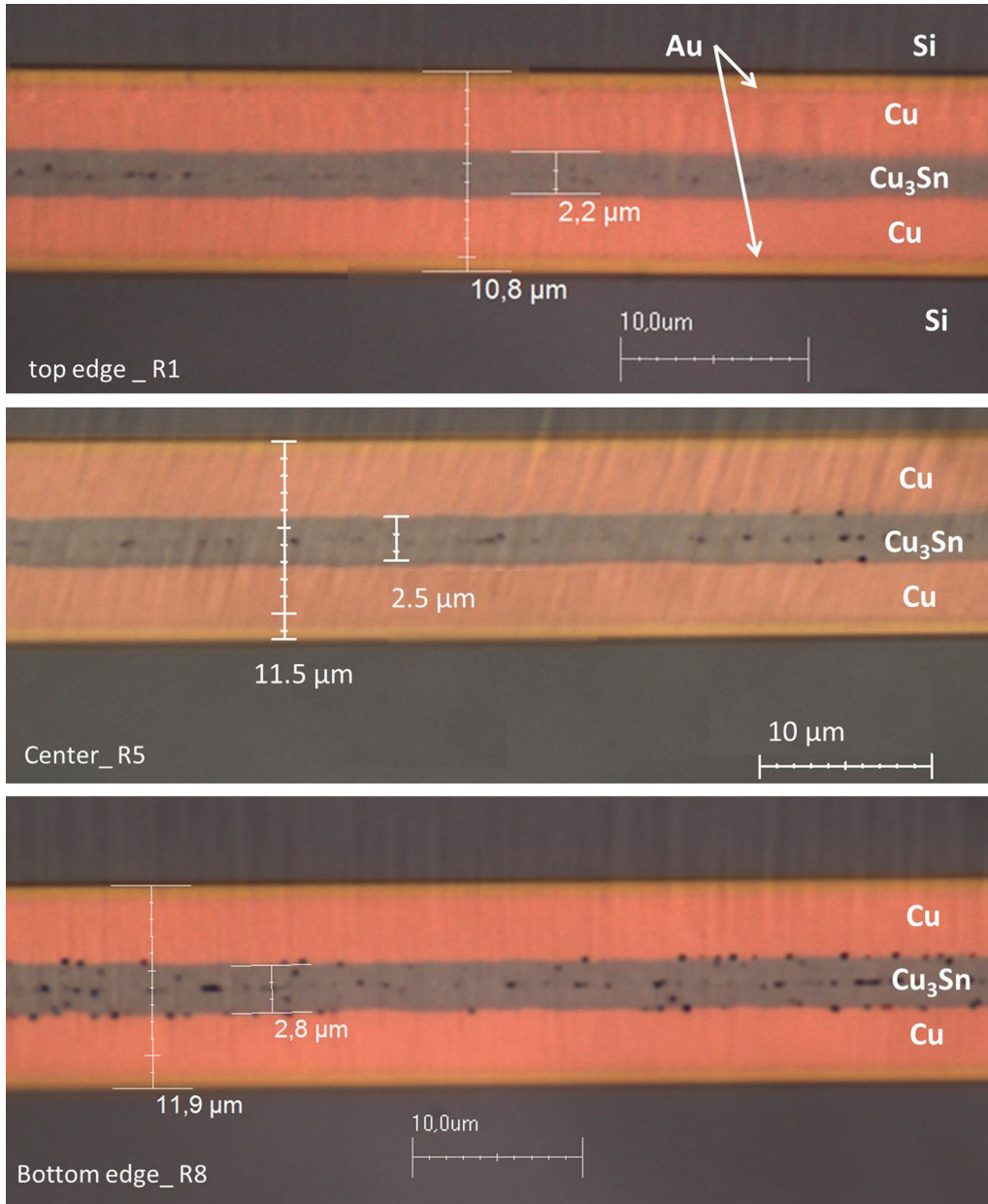
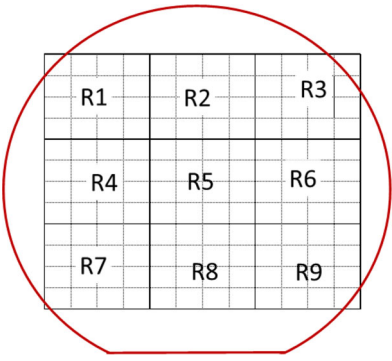


Fig. 3—Cross section of three bonded samples at different regions of the wafer: top edge—R1, bottom edge—R8, and center—R5. A final Cu/Cu₃Sn/Cu bond-line was achieved. The thickness of Cu₃Sn layer at the top edge of the wafer is thinner than at the center and bottom edge of the wafer. The thickness of the total bond-line at the top of wafer is thinner than at the center and bottom of the wafer.

Table I. Measured Initial Cu-Sn Thickness and Final Bond-Line Thickness Across the Bonded Wafer

Wafer Map	Measured Initial Electroplated Cu + Sn Thickness (μm)			Final Bond-Line Thickness (μm)	
	Wafer 1	Wafer 2	Total		
	R1			10.7	
	R2	6.1	6.8	12.9	
	R3				10.3
	R4	7.0	7.4	14.4	11.7
	R5	6.9	7.6	14.5	11.6
	R6	6.2	6.0	12.2	11
	R7				
	R8	6.1	6.9	13	11.9
	R9				
	average			13.4	
	standard deviation			1.0	

Sn layer thicknesses are not uniform. Table I shows details of measured initial Cu and Sn electroplated thicknesses and the final bond-line thickness across the wafer pair. The variations of initial electroplated thickness and final bond-line thickness are ~ 8 and ~ 4 pct. According to our experience, the Cu electroplating process introduces 2 to 7 pct non-uniformity of the thickness. For this actual bonding, the total bond-line thickness has lower variation compared with initial thickness, implying that the non-uniformity is caused by both Cu and Sn layers. The thickness is thicker at the center of the wafer pair. After bonding, the bond-line thickness is thinner than initial total thickness due to Sn squeeze out and volume change of material. The volume change (induced by the higher mass density of Cu_3Sn) causes $\sim 0.3 \mu\text{m}$ reduction of the thickness. Furthermore, voids inside Cu_3Sn layer are observed. Apparently, a thinner IMCs thickness reduces voiding. The typical voids form along the original bond interface.

B. Shear Strength and Scattering

The shear strength of the bonded samples as function of shear test temperature is shown in Figure 4. The bonds show high strength, also above the melting point of Sn. It is worth to point out that the values obtained are well above the requirement of MIL-STD-883. The average measured shear strength at RT is 43 MPa. With increasing temperature, a variation of the measured average shear strength can be observed. It is interesting to observe that at 573 K (300 °C), the shear strength is actually higher than at RT. However, the variation with shear test temperature is smaller than the actual scatter in measured data for each shear test temperature. The scatter in the measured data at room temperature is smaller than at high test temperatures.

For further investigation of the variation of shear strength across the entire wafer pair, the bonded wafer

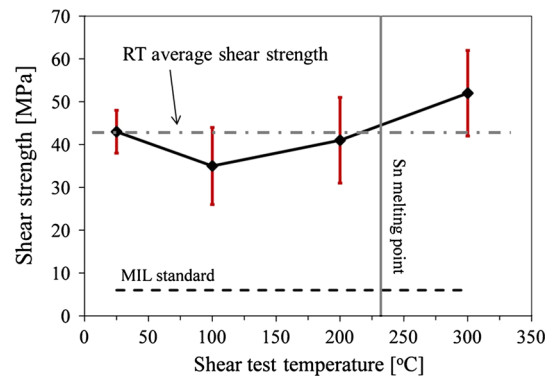


Fig. 4—Measured shear strength as function of temperature. The dot-line shows the MIL-standard shear strength 6 MPa.

pair is categorized into nine regions as shown in Figure 5(a). The scattering of the shear strength over these nine regions of the bonded wafer pair is shown in Figure 5(b). Each data point represents a measured value of the die shear strength. It is worth pointing out that for the bonds where the Cu_3Sn IMC layer is thin (R1), a larger scatter in the shear strength was observed. Less scattering of the measured shear strength was observed at the regions of the wafer where the IMC layer is thicker (R5 and R8). The measured shear strength seems to depend on the region of the tested sample on the wafer. Fractography of all sheared samples was therefore performed; however we did not observe any significant difference in fracture of the low and high shear strength samples. For shear test at room temperature, the samples were not selected in R2 and R3 (large scattered regions). The room temperature shear test was the one where we observe lower scattering of shear strength (cf. Figure 4).

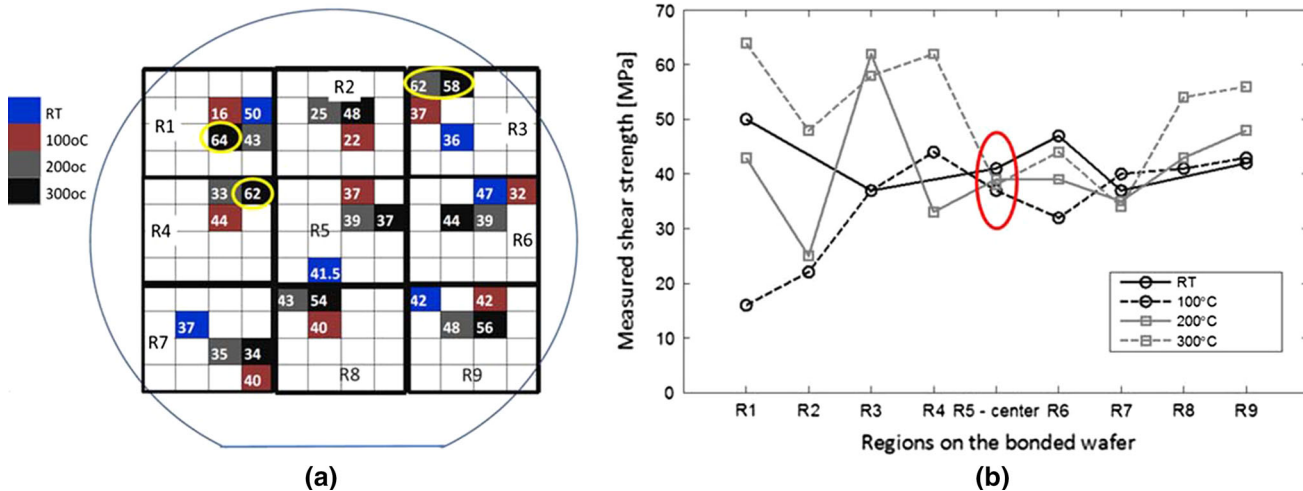


Fig. 5—Wafer map and shear strength distribution over the wafer pair. (a) Wafer map and shear strength distribution over the wafer pair. The bonded wafer pair is divided into nine different regions: R1, R2, R3, R4, R5, R6, R7, R8, and R9. Lowest scattering is observed at R5 and R7. (b) Measured shear strength and corresponding variation over the wafer pair. Each data point presents a measured value of shear strength. Large scattering of the measured shear strength was observed at R1, R2, R3, and R4. Less scattering was observed at R5, R6, R7, R8, and R9.

C. Fracture Analysis

In the bond-line, the fractures may occur at several locations: cohesive fracture in Si, Cu_3Sn , or Cu; adhesive/interface fracture between Cu to Cu_3Sn and the original bonding interface as well as between Cu and Au seed- or Ti-W adhesion layer. Four different fracture modes are observed in our fracture surfaces: (a) interface fracture in the Cu_3Sn layer at the original bond interface, (b) Cu/ Cu_3Sn fracture between Cu and Cu_3Sn IMC, (c) adhesive fracture at Ti-W to Si interface, and (d) cohesive fracture in Si. An illustration of these fracture sites and modes is shown in Figure 6.

For all tested samples, the fracture originates in one of the corners of the Si die and subsequently propagates to the rest of the bond structure. Figure 7 shows a typical fracture surface of the sheared sample; this particular sample is shear tested at 373 K (100 °C). At the origin of the fracture, the Si die is broken. This phenomenon is due to a small misalignment between the shear-tool and the sample during shear testing.

Figure 8 shows the fracture surface of a sample sheared at 473 K (200 °C), as measured by SEM/EDS and interferometry. Three well-defined fracture surfaces can be observed: interface fracture in the Cu_3Sn layer at the original bond interface (a) and Cu/ Cu_3Sn fracture between Cu to Cu_3Sn (b). In addition, squeezed-out Sn around the periphery of the bond pad can be observed. However, any residual Sn will have negligible effect on the shear strength as the Sn is not bonded to any metal. The obtained height profiles show that the fracture surfaces are planar. Using interferometry data, we can obtain the height fraction (percentage of total area) and from this extract the relative fraction of each fracture surface. For this particular sample, 80 pct of the fracture occurred at the original bond interface and 17 pct at the Cu/ Cu_3Sn interface.

The average area of fracture surfaces at different temperatures is shown in Table II. Occurrence of interface fracture between Cu and Cu_3Sn is relatively

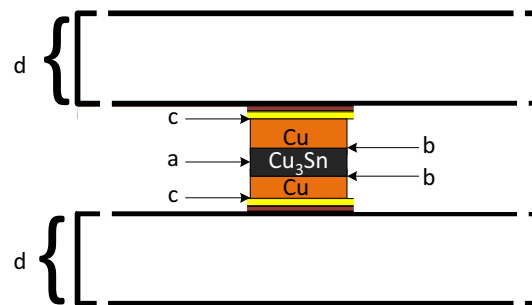


Fig. 6—Different fracture modes of Cu-Sn bonded samples from our investigation. Four different fracture modes were observed: interface fracture in the middle of Cu_3Sn intermetallic layer (a), Cu/ Cu_3Sn fracture at Cu/ Cu_3Sn interface (b), adhesive fracture at adhesion layer Ti-W to Si interface, (c) and cohesive fracture in Si (d).

small (<8 pct) compared with other fracture sites. Between 373 K and 573 K (100 °C and 300 °C), the two dominating fracture modes are interface fracture in Cu_3Sn at the original bond interface (a) and adhesive fracture at the Ti-W to SiO_2 interface. A high percentage of adhesive fracture at the Ti-W to SiO_2 interface (from 37 to 53 pct) and at the original bond interface (from 23 to 51 pct) was observed from RT to 573 K (300 °C), showing that the adhesion between Ti-W to SiO_2 and the original bond interface are the weakest interfaces of the bonded samples. For samples tested at room temperature, cohesive fracture in the Si dies also frequently occurred. A typical fracture surface of the substrate side of sheared samples at RT is shown in Figure 9, where the three different fracture surfaces are well-defined. With respect to the variation in fracture modes at RT and higher temperatures, it is worth to point out that the shear tester tool head was aligned (parallel to the die edge) at high temperature. When cooled to room temperature, a misalignment between

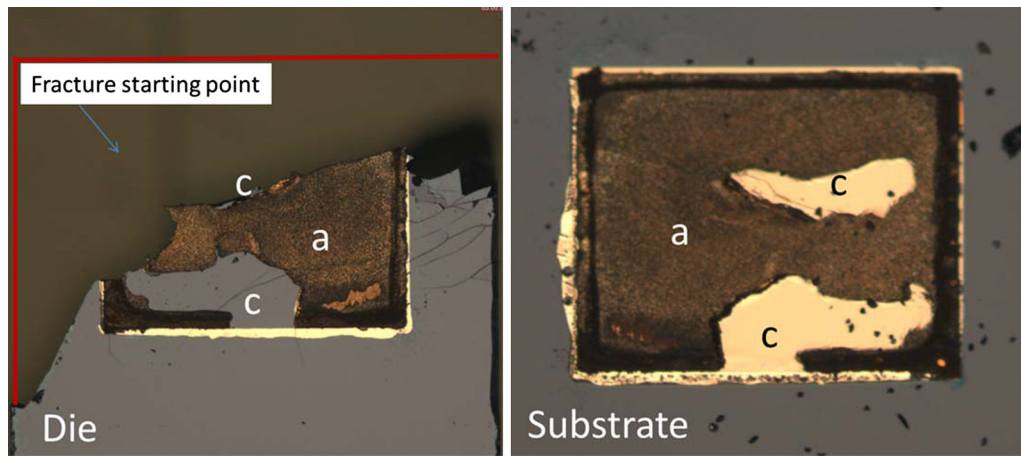


Fig. 7—Typical fracture of the die during shear test. The fracture originates from one of the corners of the die where Si is broken. For this particular sample, two different fracture modes are observed at the substrate side: interface fracture (*a*) and adhesive fracture at the Ti-W to Si interface (*c*).

the tool head and dies may cause the fracture to originate from the die edge and then propagate to other positions of the sample.

IV. DISCUSSION

In this study, we investigated the mechanical strength of the Cu-Sn SLID bonded samples, shear tested at different temperatures, from room temperature to 573 K (300 °C). There is variation of shear strength at different shear test temperatures. The variation of shear strength is dominated by the large scattering in regions R1, R2, R3, and R4 of the wafer pairs. When narrowing in on data obtained from regions with less scatter in measured data (R5-R9) (see Figure 5), the variation of shear strength with shear test temperature is not significant. Based on this, we conclude that there is no mechanical degradation of the Cu-Sn bonded samples from RT to 573 K (300 °C). The measured shear strength is significantly larger than the requirement of MIL-STD-883 (6 MPa). Currently, commercial products use a high-lead content Pb-Sn solders for high-temperature applications.^[23] Alternative solders based on Ag-Sn, Au-Sn, Zn-Sn, Sn-Sb, Au-Ge, and Zn-Al have been investigated to replace Pb-Sn.^[24–26] However, these solders show significant degradation of the mechanical properties at elevated temperatures 373 K to 523 K (100 °C to 250 °C).^[23–27] Therefore, Cu-Sn bonding is an attractive technique suitable for high-temperature applications. Previous studies on Cu-Sn SLID bonding also proved that the bonding has stable mechanical strength after thermal cycling and thermal aging.^[14,28,29] However, in those studies, the mechanical properties of bonded samples were investigated at room temperature. In this study, the mechanical strength was measured at high temperatures, and thus gives experimental evidence for

the high-temperature stability of Cu-Sn SLID that has long been predicted on a theoretical basis.

Significant scattering of measured shear strength is caused by misalignment during shear testing and non-uniformity of the electroplating process. Non-uniformity introduces non-homogenous bond pressure and bond performance over the wafers. Theoretically, when the temperature is above the melting point of Sn, Sn melts and compensates this non-uniformity. In the regions with limited Sn available (thin Sn layer), the Sn is directly solidified into IMCs resulting in limited compensation. This leads to a large scattering of the measured shear strength.

In addition to the non-uniformity of initial Cu and Sn thickness over the wafer, we have non-uniformity at the same bonding pad. An example of non-uniformity of initial Sn thickness at the same pad is shown in Figure 10. At the edge of the bond pad, the bond-line thickness is thicker than at the center of the bond pad. This causes poor wetting at the original bond interface at the center of the pad and results in interface voids and un-bonded areas. During shear testing, this interface is the weakest interface. This is the reason why we obtained a high area fraction of fracture at the original bond interface.

A new method for fracture characterization presented in this work was used to determine that the two most dominating fracture modes (Table II) are brittle in nature: interface fracture at the original bond interface in the Cu₃Sn layer, and adhesive fracture between Ti-W adhesion layer and SiO₂. Fractures at these interfaces imply that the mechanical strength of the Cu-Sn SLID bonded layer is stronger than the adhesion layer and the interface layer. This allows for improving the bond strength by manufacturing process optimization, as improved adhesion layers and improved wetting of the bond interface can further increase the bond strength.

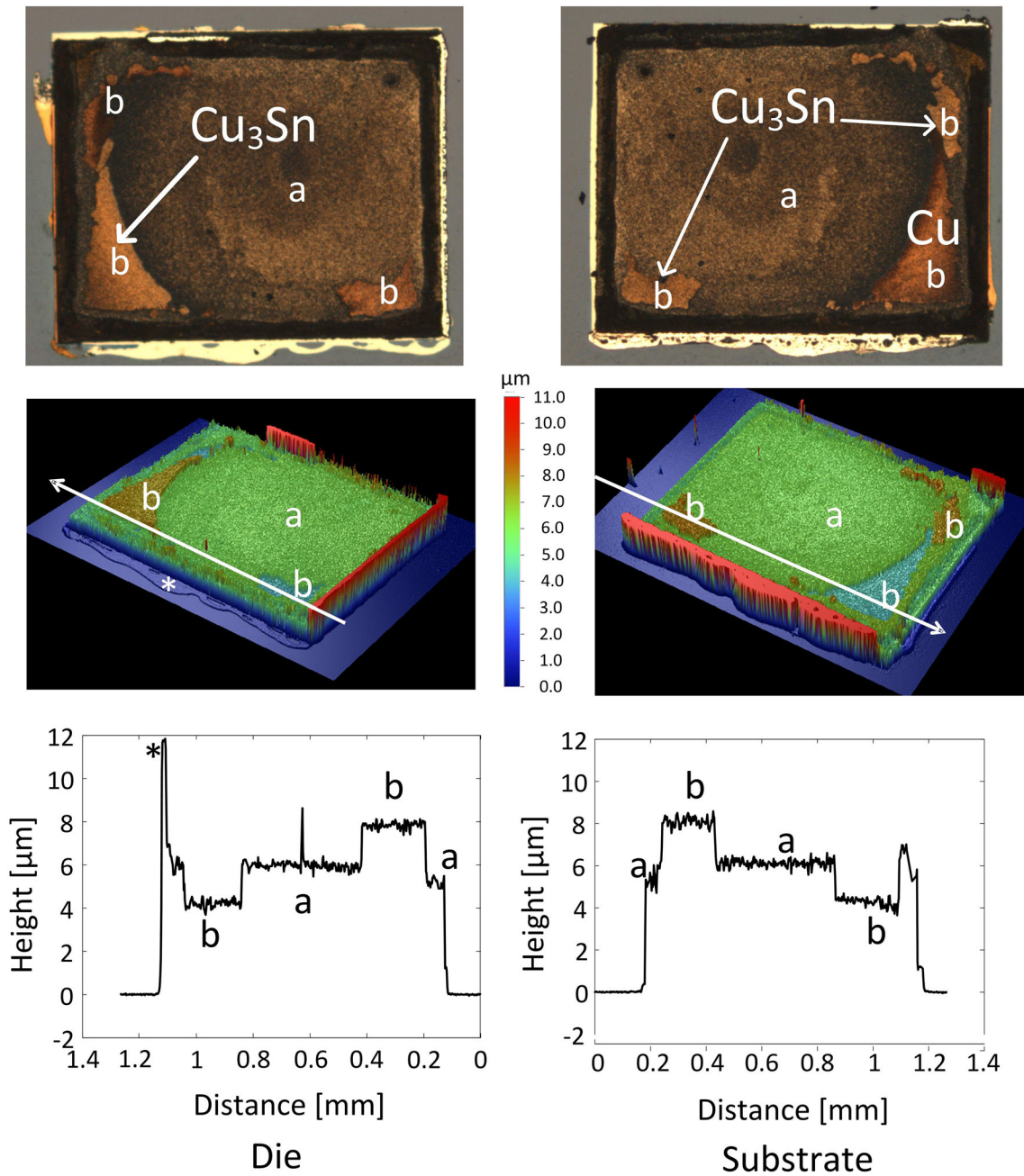


Fig. 8—Microscopy of the fracture surface of a sample sheared at 473 K (200 °C). Three well-defined fracture modes were observed: Interface fracture in Cu_3Sn layer (*a*), $\text{Cu}/\text{Cu}_3\text{Sn}$ fracture at $\text{Cu}/\text{Cu}_3\text{Sn}$ interface (*b*) and fracture at squeezed-out Sn (*). The height profile shows that the fracture surfaces are planar. The pct area surface of each fracture mode can be extracted from percentage height profile.

Table II. Average Area Fraction of Different Fracture Surfaces of Samples Sheared at RT—573 K (300 °C)

Shear Test Temperature	Interface Fracture (a)	Adhesive, $\text{Cu}/\text{Cu}_3\text{Sn}$ (b)	Adhesive, Si, Ti-W,Au (c)	Cohesive Fracture in Si (d)
RT 298 K (25 °C)	0.23	0.01	0.53	0.23
373 K (100 °C)	0.52	0.02	0.41	0.05
473 K (200 °C)	0.50	0.04	0.42	0.04
573 K (300 °C)	0.51	0.08	0.37	0.04

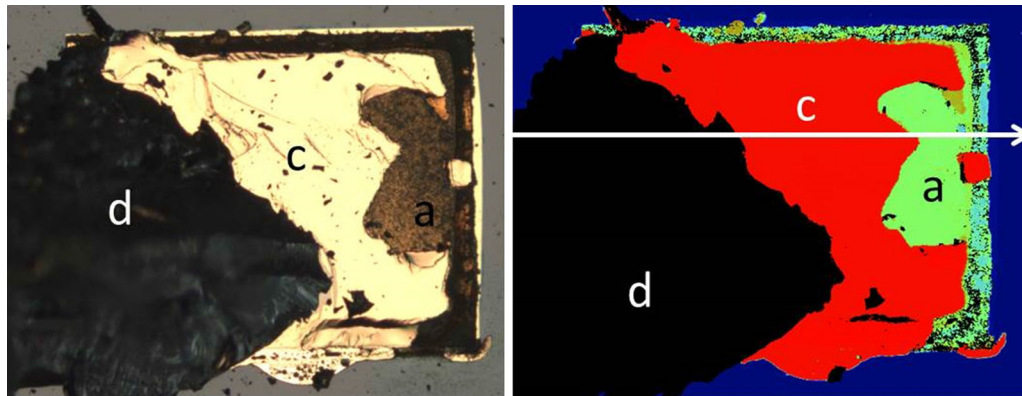


Fig. 9—Fracture surfaces on a sample sheared at room temperature. Three fracture modes are visible: interface fracture in Cu_3Sn layer (a), adhesive fracture at Ti-W layer, (c) and cohesive fracture in the Si die (d).

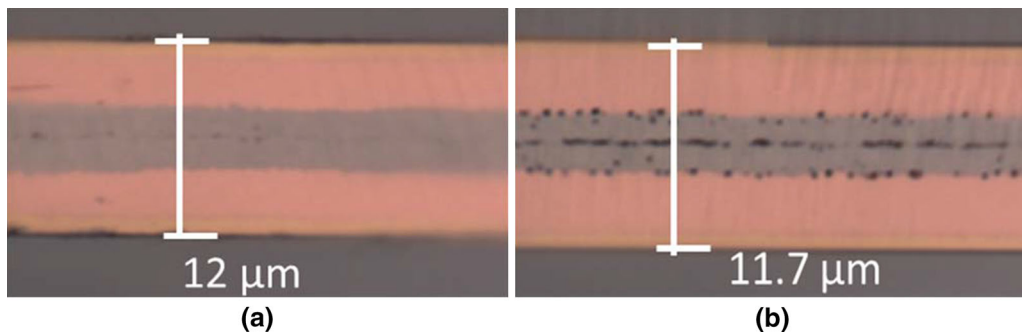


Fig. 10—Cross section of a bonded sample from R4. The bond-line thickness is not uniform across the same die. At the position that the bond-line thickness is thinner, un-bonded areas appear.

V. CONCLUSION

Cu-Sn SLID wafer-level bonding results in a high bonding yield and a high mechanical integrity, also well above the melting point of Sn. The average measured shear strength is 42 MPa, exceeding the MIL-STD by far. For shear tests performed at temperatures from room temperature up to 573 K (300 °C), no significant change in shear test is observed, thus verifying the high-temperature stability predicted for Cu-Sn SLID bonding. The small change observed in average shear strength with shear test temperature is caused by large scatter in data for certain wafer pair areas.

These high shear strengths are obtained although there was non-uniformity in the electroplating process that resulted in larger scattering of the shear strength at several regions of the bonded wafer pair. The non-uniformity also caused voids and un-bonded areas at the original bond interfaces, and led to this being one of two dominating fracture surfaces. The other dominating fracture surface was adhesive fracture at Ti-W adhesion layer to SiO_2 . The fracture at these interfaces provides evidence that the mechanical integrity of Cu-Sn SLID bonded samples is stable up to 573 K (300 °C) and stronger than the adhesion layer. Further improvement of the bond strength may be obtained by improving the adhesion layers and the uniformity of the electroplated layer thicknesses.

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REFERENCES

1. S. Giudice and C. Bosshard: *Microelectronics Packaging Conference (EMPC), 2013 European*, 2013, pp. 1–5.
2. N. Hoivik and K. Aasmundtveit: *Handbook of Wafer Bonding*, 1st ed., Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, 2012, pp. 181–214.
3. J.F. Li, P.A. Agyakwa, and C.M. Johnson: *Acta Materialia*, 2010, vol. 58, pp. 3429–43.
4. T. Tollefsen, A. Larsson, O. Løvrik, and K. Aasmundtveit: *Metall. Mater. Trans. B*, 2012, vol. 43B, pp. 397–405.
5. C. Yu-San, H. Yan-Pin, T. Ruoh-Ning, S. Ming-Shaw, L. Teu-Hua, C. Kou-Hua, C. Chi-Tsung, C. Ching-Te, H. Wei, C. Jin-Chern, T. Ho-Ming, and C. Kuan-Neng: *IEEE Trans. Electron. Devices*, 2014, vol. 61, pp. 1131–36.
6. P.L. Dreike, D.M. Fleetwood, D.B. King, D.C. Sprauer, and T.E. Zipperian: *IEEE Trans. Compon. Packag. Manuf. Technol. Part A*, 1994, vol. 17, pp. 594–609.
7. C. Gallagher, B. Shearer, and G. Matijasevic: *High-Temperature Electronic Materials, Devices and Sensors Conference*, 1998, pp. 180–89.

8. R.W. Johnson, J.L. Evans, P. Jacobsen, J.R. Thompson, and M. Christopher: *IEEE Trans. Electron. Packag. Manuf.*, 2004, vol. 27, pp. 164–76.
9. G. Zonfrillo, I. Giovannetti, and M. Manetti: *Meccanica*, 2008, vol. 43, pp. 125–31.
10. A. Lapadatu, T.I. Simonsen, G. Kittilsland, B. Stark, N. Hoivik, V. Dalsrud, and G. Salomonsen: *ECS Trans.*, 2014, vol. 33, pp. 73–82.
11. H. Xu, M. Broas, H. Dong, V. Vuorinen, T. Suni, S. Vahanen, P. Monnoyer, and M. Paulasto-Krockel: *Microelectronics Packaging Conference (EMPC), 2013 European*, 2013, pp. 1–6.
12. N.P. Pham, P. Limaye, P. Czarnecki, V.P. Olalla, V. Cherman, D.S. Tezcan, and H.A.C. Tilmans: *Proceedings of the Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 1–6.
13. Y. Lv, M. Chen, M. Cai, and S. Liu: *Semicond. Sci. Technol.*, 2014, vol. 29, p. 025003.
14. F. Lang, H. Yamaguchi, H. Nakagawa, and H. Sato: *J. Electrochem. Soc.*, 2013, vol. 160, pp. D315–19.
15. A. Campos-Zatarain, D. Flynn, K. Aasmundtveit, N. Hoivik, K. Wang, H. Liu, T.-T. Luu, M. Mirgizoudi, and R. W. Kay: *Symposium on Design, Test, Integration & Packaging of MEMS/MOEMS*, 2014, pp. 175–79.
16. J.D. Reed, M. Lueck, C. Gregory, A. Huffman, J.M. Lannon, and D. Temple: *Proceedings 60th Electronic Components and Technology Conference (ECTC)*, 2010, pp. 846–52.
17. R. Labie, P. Limaye, K.W. Lee, C.J. Berry, E. Beyne, and I. De Wolf: *Proceedings of the Electronic System-Integration Technology Conference (ESTC), 2010 3rd*, 2010, pp. 1–5.
18. C. Yao-Jen, K. Cheng-Ta, and C. Kuan-Neng: *Electron Device Lett. IEEE*, 2013, vol. 34, pp. 102–04.
19. A. Duan, K. Wang, K.E. Aasmundtveit, and N. Hoivik: *Electronic System-Integration Technology Conference (ESTC), 2012 4th*, 2012, pp. 1–5.
20. H. Xu, T. Suni, V. Vuorinen, J. Li, H. Heikkinen, P. Monnoyer, and M. Paulasto-Kröckel: *Adv. Manuf.*, 2013, vol. 1, pp. 226–35.
21. T.T. Luu, A. Duan, K.E. Aasmundtveit, and N. Hoivik: *J. Electron. Mater.*, 2013, vol. 42, pp. 3582–92.
22. T.A. Tollefsen, A. Larsson, O.M. Lovvik, and K.E. Aasmundtveit: *IEEE Trans. Compon., Packag. Manuf. Technol.*, 2013, vol. 3, pp. 904–14.
23. F. McCluskey, M. Dash, Z. Wang, and D. Huff: *Microelectron. Reliab.*, 2006, vol. 46, pp. 1910–1914.
24. G. Zeng, S. McDonald, and K. Nogita: *Microelectron. Reliab.*, 2012, vol. 52, pp. 1306–1322.
25. A. Geranmayeh, R. Mahmudi, and M. Kangooie: *Mater. Sci. Eng. A*, 2011, vol. 528, pp. 3967–72.
26. R. Mahmudi and S. Alibabaie: *Mater. Sci. Eng. A*, 2013, vol. 559, pp. 421–26.
27. K.E. Aasmundtveit, L. Thi-Thuy, A.S.B. Vardoy, T.A. Tollefsen, W. Kaiying, and N. Hoivik: *Electron. Sys. Integr. Technol. Conf. (ESTC)*, 2014, vol. 2014, pp. 1–6.
28. L. Xu and J.H. Pang: *Thin Solid Films*, 2006, vol. 504, pp. 362–66.
29. H. Xu, M. Broas, H. Dong, V. Vuorinen, T. Suni, S. Vahanen, P. Monnoyer, and M. Paulasto-Krockel: *Microelectronics Packaging Conference (EMPC), 2013 European*, 2013, pp. 1–6.