DOI 10.1007/s11595-016-1335-6

Carrier Transport Across Grain Boundaries in Polycrystalline Silicon Thin Film Transistors

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Abstract: We established a model for investigating polycrystalline silicon (poly-Si) thin film transistors (TFTs). The effect of grain boundaries (GBs) on the transfer characteristics of TFT was analyzed by considering the number and the width of grain boundaries in the channel region, and the dominant transport mechanism of carrier across grain boundaries was subsequently determined. It is shown that the thermionic emission (TE) is dominant in the subthreshold operating region of TFT regardless of the number and the width of grain boundary. To a poly-Si TFT model with a 1 nm-width grain boundary, in the linear region, thermionic emission is similar to that of tunneling (TU), however, with increasing grain boundary width and number, tunneling becomes dominant.

Key words: carrier transport; grain boundaries; thin film transistors; polycrystalline silicon

1 Introduction

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) are commonly used in active-matrix LCDs (AMLCDs) as pixel switches, drivers, and peripheral analogue circuits[1,2]. Compared to the conduction mechanism of a conventional single-crystal metal-oxide-semiconductor field effect transistor (MOSFET), that of a poly-Si TFT is complicated by the inclusion of discrete grain boundaries (GBs) in the channel region. A number of empirical and physical models have been proposed to investigate the conduction mechanism of a poly-Si TFT. In some models, the transport processes are considered separately: drift-diffusion (DD) transport through the grain and thermionic emission (TE) across the grain boundary[3-8]. Other models consider the effect of temperature and assume that tunneling through the grain boundary dominates thermionic emission over the barrier at low temperatures[9-12]. There is a model which assumes that thermionic emission is the major mechanism of carrier over the potential barriers created within the grains and then tunneling (TU) through the grain boundaries is proposed as the carrier transport mechanism[13]. In addition, the conduction process in the poly-Si TFT is found to be affected by the parameters such as grain size, defect density, density of states, and the gate voltage[14].

In this article, a poly-Si TFT model is set up by means of a semiconductor device simulator. Basing on the analysis of the transfer characteristics considering the width and the number of grain boundary in the poly-Si channel region, the transport mechanism of carrier across grain boundary is determined.

2 Model of poly-Si TFT

A conventional poly-Si TFT is often fabricated with a top gate or bottom gate structure. Compared to the former, the latter has the advantage of larger on-state current, low cost[15], and is fully compatible with current a-Si:H production equipment[16]. Fig.1 shows

(Received: Oct. 20, 2014; Accepted: Nov. 4, 2015)

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Funded by the National Natural Science Foundation of China (Nos. 51202063 and 51177003), Hubei Provincial Department of Education (No.Q20111009)

the structure of poly-Si TFT for two dimensional (2D) device simulation. The device is *n*-channel with a doping concentration of 1×10^{15} cm^{-3}, channel length 6 μm, thickness 100 nm, and the source and drain is n^+ doped.

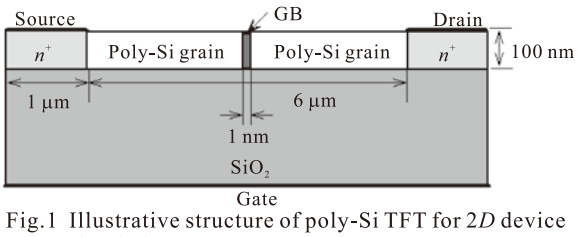

Fig.1 Illustrative structure of poly-Si TFT for 2*D* device simulation

A commercial device simulator of ISE-TCAD package was utilized to investigate the carrier transport of poly-Si TFT at room temperatures. In the simulator, the basic model of carrier transport in semiconductor was the drift-diffusion. By coupling the drift-diffusion model with the thermionic emission model or tunneling model at the interface between the grain and the grain boundary, the action of carrier across the grain boundary by thermionic emission or tunneling was simulated. By comparing the transfer characteristics of the coupled models with that of the drift-diffusion model, the dominant transport of carrier across the grain boundary can be determined.

3 Results and discussion

It is known that the thermionic emission current density J_e and tunneling current density J_t in the semiconductor have the similar expression as:

$$J_e(J_t) = J_{0e}(J_{0t})(-\frac{E_1}{kT}) \tag{1}$$

The prefactors J_{0e} and J_{0t} are given by:

$$J_{0e} = A^*T^2 f_{se} \exp(\frac{-\Delta E_c}{kT}) \tag{2}$$

$$J_{0t} = A^*T^2 t[\exp(\frac{V}{2kT}) - \exp(-\frac{V}{2kT})] \tag{3}$$

where k is the Boltzmann constant, A^* is the Richardson-Fermi constant which is 260 (A cm^{-2} K^{-2}) for electrons in silicon. f_{se} is a factor related to the reduction in current density due to electron-phonon scattering and quantum reflection at the interface. E_1 is the conduction activation energy in the flatband region. ΔE_c is the GB energy barrier and is equal to qV_b, V_b is the potential barrier height of grain boundary. V is the bias voltage, and t represents the transmission coefficient for electron tunneling through the barrier. As $\Delta E_c >> kT$, it can be expressed as[17]:

$$t = \frac{16kT}{\Delta E_c}\exp[-\frac{2s}{\hbar}(2m^*\Delta E_c)^{1/2}] \tag{4}$$

where s is the width of potential barrier. From the above formulas, the thermionic emission current and the tunneling current are related to the potential barrier height V_b, with increasing potential barrier height, both currents decrease. In addition, the tunneling current is related to the width of potential barrier, with increasing width, the tunneling current decreases.

3.1 Poly-Si TFT model with multi-GBs

A poly-Si TFT model with different number of grain boundaries uniformly distributed in the channel is set up to explore the effect of grain size on the carrier transport. The number of grain boundaries is chosen to be 1, 4, 9, 17 and 35, respectively, and the width of grain boundaries is 1 nm. Now that the potential barrier formed by the trap states in grain boundary has a strong effect on the electric property of poly-Si TFT, the energy band diagrams at the surface of poly-Si thin film with different number grain boundaries are plotted for the pure drift-diffusion model, the thermionic emission model and the tunneling model. Here, the potential barriers under two bias conditions are shown, the first condition is that there is no bias applied on the electrodes, and the second is that the drain-source voltage V_{ds} is 1 V and the gate voltage V_{gs} is 45 V. The results are shown in Fig.2, at the same time, the corresponding transfer characteristics of TFT are shown in Fig.3. From the energy band diagrams of TFT with different number of grain boundary, we can see that the potential barrier height V_b of the tunneling model is nearly the same as that of the pure drift-diffusion model and much higher than that of the thermionic emission model in the case of no bias applied on the electrodes, so the thermionic emission current is higher than the tunneling current in the initial stage of TFT operation, in other word, thermionic emission is the dominant transport mechanism across grain boundary in the subthreshold region of TFT. However, to a TFT with one grain boundary, the difference between the thermionic emission current and the tunneling current is less throughout the operating of TFT, in this case, thermionic emission and tunneling compete. With increasing grain boundary number, in

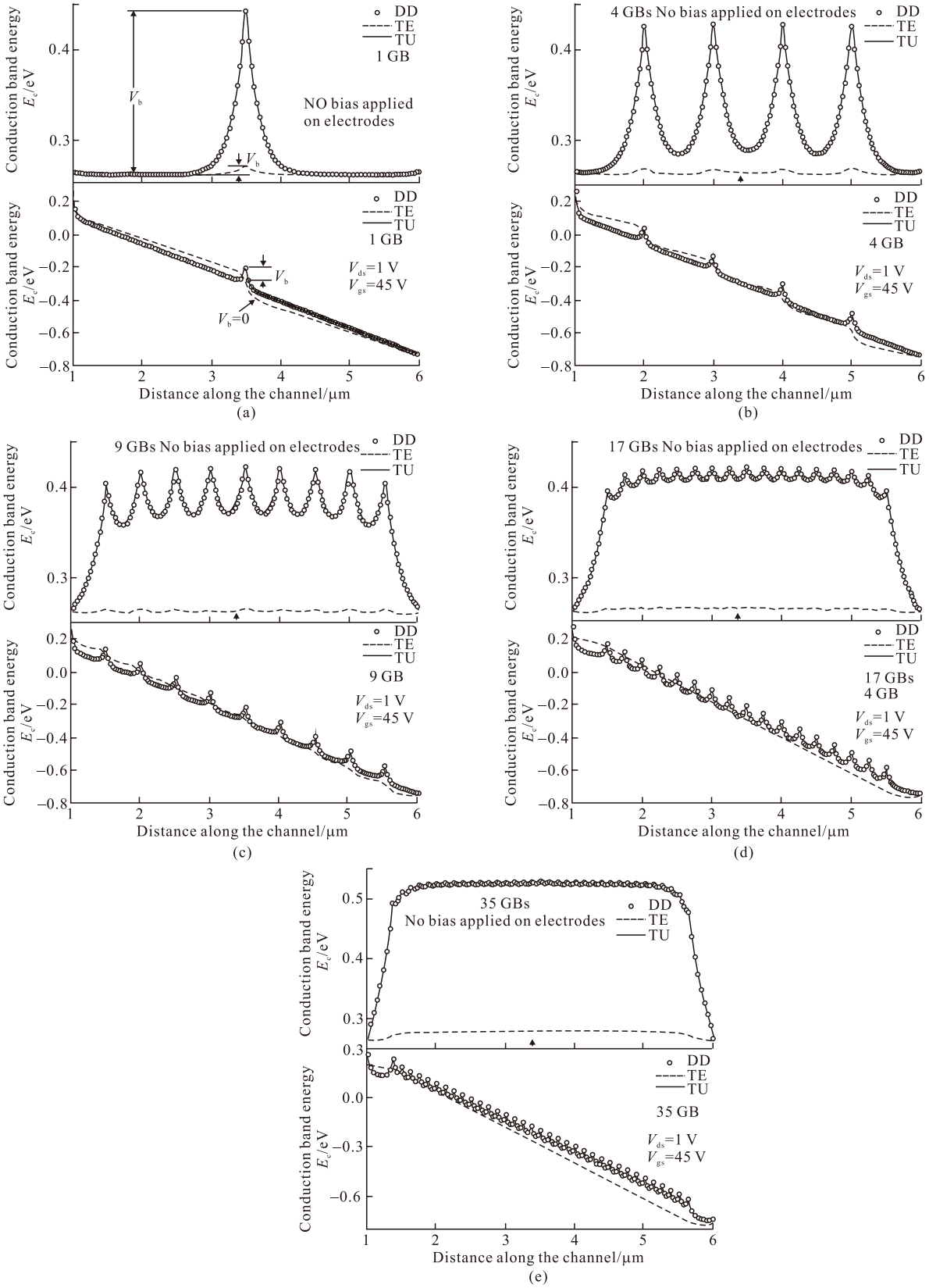

Fig.2 Comparison of energy band diagrams at the surface of ploy-Si thin film for the DD model, TE model and TU model, which are under two bias conditions, the first is no applied bias on electrodes, and the second is that V_{ds} is 1 V and V_{gs} is 45 V: (a)1 GB; (b)4 GBs; (c)9 GBs; (d)17 GBs; and (e) 35 GBs

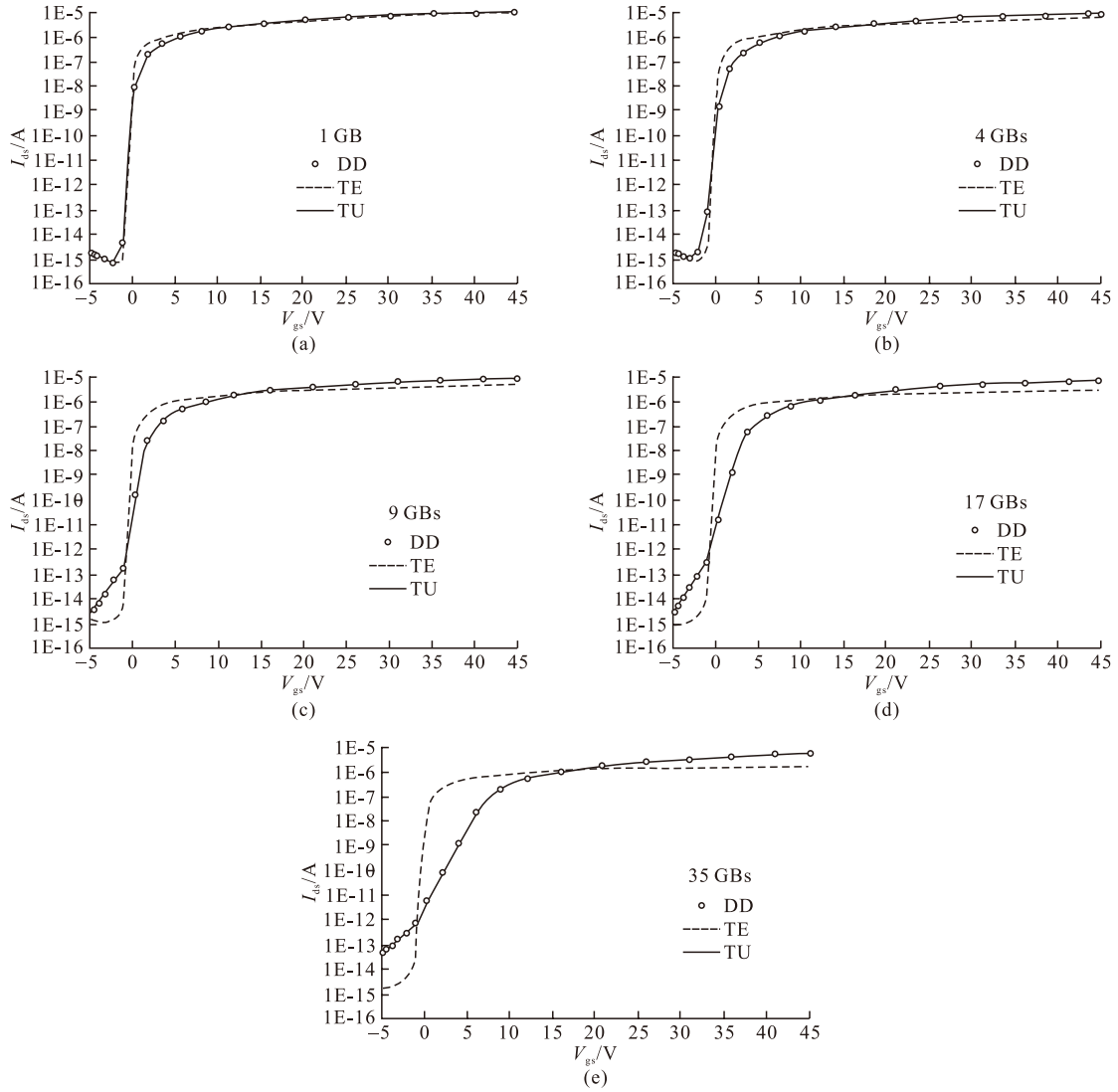

Fig.3 Comparison of transfer characteristics of poly-Si TFT for the DD model, TE model and TU model, the drain-source bias voltage V_{ds} is 1 V: (a)1 GB; (b)4 GBs; (c)9 GBs; (d)17 GBs; and (e) 35 GBs

the linear region, tunneling becomes dominant. This is because the potential barrier of the thermionic emission model is suppressed by the high gate bias V_{gs}, as a result, the thermionic emission current is lower than that of the tunneling current and the pure drift-diffusion current. On the other hand, the tunneling current is less affected by the potential barrier compared to the thermionic emission current, though the number of grain boundary increases, the width of grain boundary keeps unchanged, as a result, tunneling dominates over thermionic emission.

3.2 Poly-Si TFT model with grain boundary with different width

Another poly-Si TFT model with different grain boundary width is set up to investigate the effect of grain boundary width on the carrier transport. The grain boundary width is chosen to be 1, 10, 30 and 50 nm respectively. The energy band diagrams at the surface of poly-Si thin film are plotted in the case of no applied bias on electrodes and the case that V_{ds} is 1 V and V_{gs} is 45 V, and the results are shown in Fig.4. The transfer characteristics are shown in Fig.5. Here, the energy band diagrams and current curves of 1 nm-width grain boundary are the same as the diagrams and curves shown in Fig.2(a) and Fig.3(a). From the curves, a result is obtained that thermionic emission is dominant in the initial stage of TFT operation regardless of the grain boundary width, in the linear region, the potential barrier is suppressed, and the dominant transport is tunneling, which is similar to that of the previous TFT model with different number of grain boundary. With increasing grain boundary width, the number of trap states increases, so the potential barrier height V_b of the thermionic emission model and the tunneling model increases, as a result, the thermionic emission current and the tunneling current both decrease, and

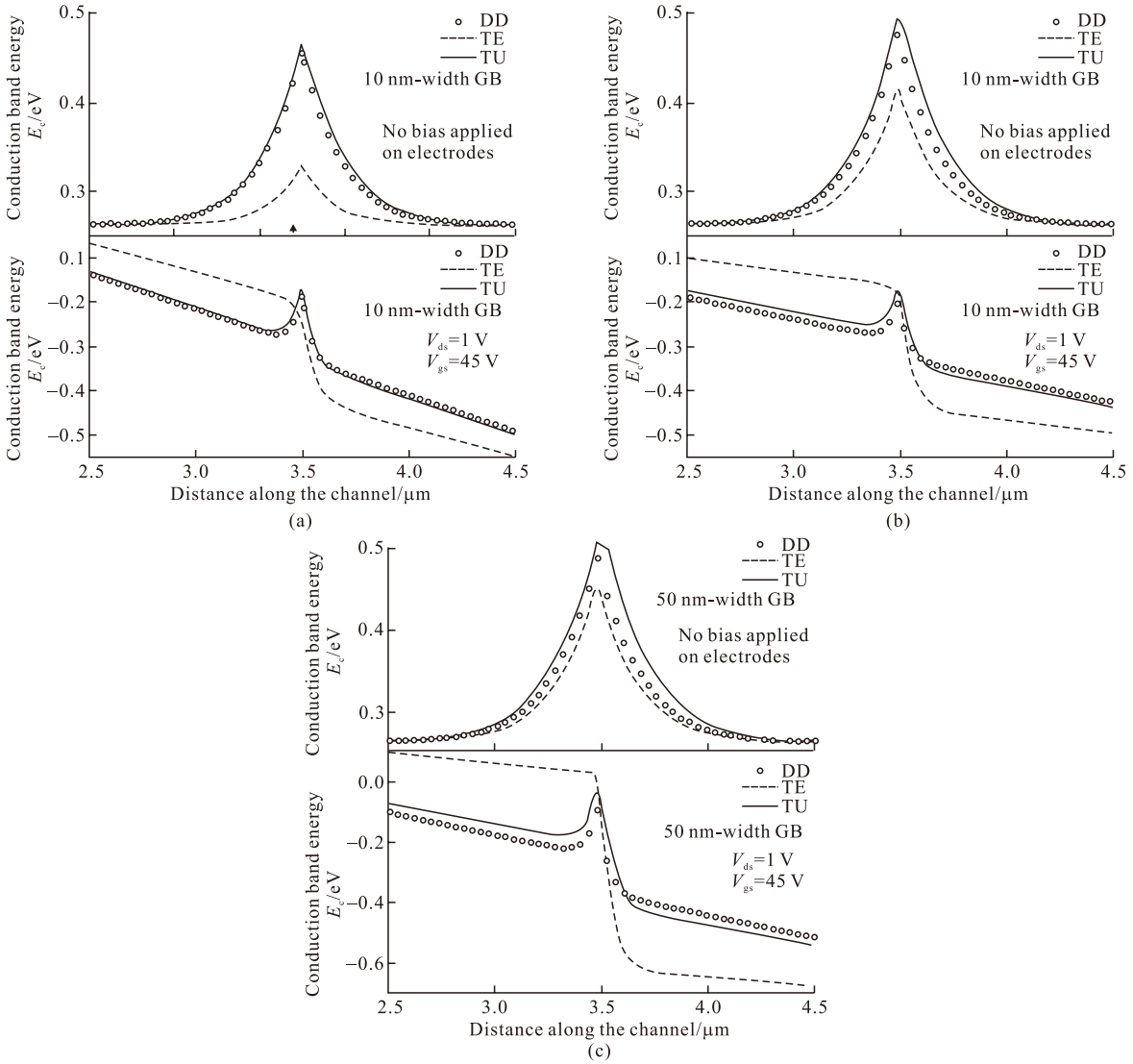

Fig.4 Comparison of energy band diagrams at the surface of ploy-Si thin film for the DD model, TE model and TU model, which are under two bias conditions, the first is no applied bias on electrodes, and the second is that V_{ds} is 1 V and V_{gs} is 45 V: (a) 10 nm-width GB; (b) 30 nm-width GB; (c) 50 nm-width GB. The diagrams of TFT with 1 nm-width GB are shown in Fig.2 (a)

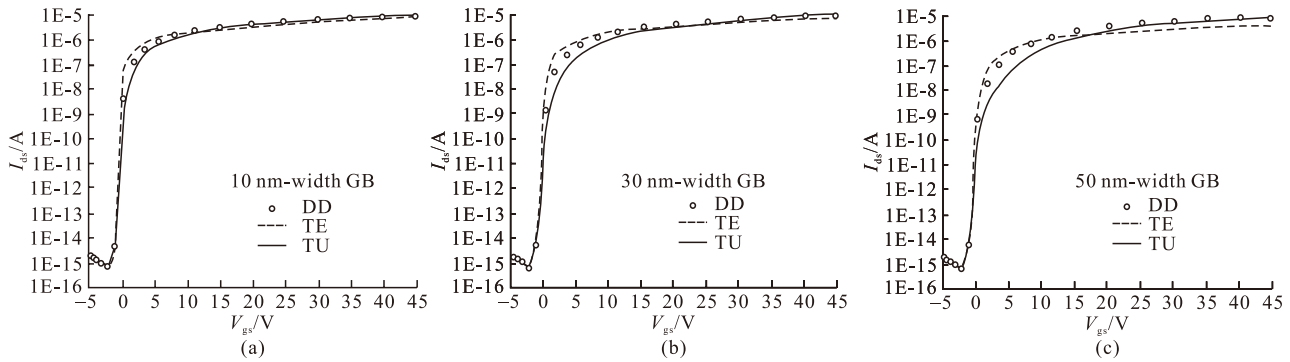

Fig.5 Comparison of transfer characteristics of poly-Si TFT for the DD model, TE model and TU model, the drainsource bias voltage V_{ds} is 1 V: (a) 10 nm-width GB; (b) 30 nm-width GB; (c) 50 nm-width GB. The curves of TFT with 1 nm-width GB are shown in Fig.3 (a)

the tunneling current is less than that of the pure drift-diffusion current.

4 Conclusions

A polycrystalline silicon thin film transistors model is set up, and the effect of grain boundary number and grain boundary width on carrier transport across grain boundary is investigated. In the subthreshold operating region of TFT, thermionic emission dominates over tunneling regardless of the grain boundary number and grain boundary width. In the linear region, tunneling becomes dominant.

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