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Recent research development of FinFETs

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The rapid development of CMOS technology is driven by the device scaling down. Classical MOS devices have encountered difficulties and challenges as scaling down to nanoscale [1], which seriously affects the device performance and limits the further development of CMOS technology. Because of the excellent control over short-channel effects and high current drive capability, novel multi-gate MOS devices have been regarded for years as the most attractive devices to continue the CMOS technology development following "Moore's law" [2]. Among which FinFET, mainly proposed by Hisamoto et al. [3], has attracted considerable scholarly attention [4-7] and has been adopted as the basic device of VLSI by industry. Figure 1 shows the schematic view comparison between classical planar bulk *n*-channel MOSFET and that of FinFET. Intel is the first company who released the production of 22 nm FinFET technology in 2011. To the authors' knowledge, there are mainly three companies in industry having stepped into FinFET Techonlogy. Samsung plans to ship 10 nm FinFET technology by the end of 2016. Intel will move into 10 nm production by mid-2017, with 7 nm slated for 2018 or 2019. TSMC will move into 10 nm production in early 2017, with 7 nm slated to ship in 2018. Meanwhile, in addition to the three companies, GlobalFoundries will be in the mix at 7 nm. This paper will briefly introduce the recent research development of FinFET, including the experimental research progress and the analytical model research progress.

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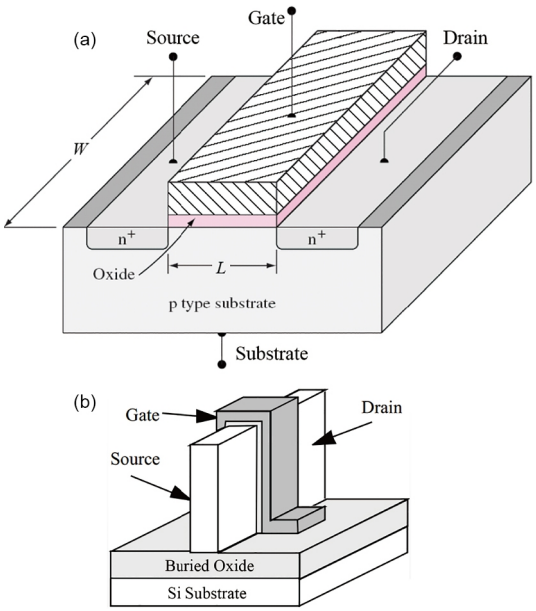

Figure 1 (Color online) Schematic view of classical planar bulk *n*-channel MOSFET (a) and FinFET (b).

(1) Experimental demonstration

FinFET with Si channel. Silicon is the main channel material in semiconductor industry. Intel, the company who first released the production of FinFET technology, published a 14 nm logic technology featuring 2nd-Generation FinFET with strained Si channel [8]. L_{gate} scaled from 26 nm in the 22 nm node to 20 nm in the 14 nm node. It is enabled by fin profile optimization and a novel subfin doping. At 0.7 V

V_{dd}, off current is 10 nA/μm, and saturated drive currents are 1.04 mA/μm for both NMOS and PMOS. Sub-threshold slope is ~65 mV/decade. DIBL is ~60 mV/V and ~75 mV/V for NMOS and PMOS, respectively. High-density SRAM featuring 0.0588 μm^2 cell size are fabricated usi ng all 14 nm process features.

FinFET with high mobility material channel. III-V materials attract much interest to be adopted as the channel material since they have potential advantages as high mobility, high injection velocity (small m^*), and near-ballistic performance. Lu et al. [9] demonstrated and published the first InGaSb p-channel FinFET. They developed a fin dry-etch technology which yields fins as narrow as 15 nm with vertical sidewalls and realized Si-compatible ohmic contacts with ultra-low contact resistivity of 3.5×10^{-8} $\Omega\cdot cm^2$. Gate oxide is Al_2O_3 with an EOT of 1.8 nm. g_m of 122 μS/μm is obtained in devices of W_f = 100 nm and L_g = 100 nm, while g_m of 78 μS/μm is achieved in the smallest devices with W_f = 30 nm and L_g = 100 nm.

FinFET with TMD channel. At ultra-thin body thickness, novel two-dimensional transition-metal dichalcogenide (TMD) is a very attracting channel material for its unique sub-nm monolayer ultra-thin body potential and good transport property at nanometer thinness. For the first time, Chen et al. [10] proposed and demonstrated a 4 nm thin transition-metal dichalcogenide (TMD) body FinFET with back gate control. Two key processes in the demonstration of TMD FinFET are CMOS-compatible CVD conformal MoS_2 growth and Hydrogen plasma treatment of MoS_2 for low contact resistance. The front gate MoS_2 FinFET device has on/off current ratio larger than 10^5. I_{on} for 1 V V_{dd} is 200 μA/μm.

(2) Analytical model

Long channel *I-V* model. Analytical model is of great importance in depicting the physical insight of device, serving as the guideline for device design and circuit analysis, predicting the future trend of device development, and serving in the circuit simulator. Long channel model is the core model depicting the basic operating behavior of device. Depending on the thickness of top gate insulator compared to that of the side gates, FinFET includes double-gate (DG) and triple-gate (TG) structure. Taur et al. [11] presented a continuous analytical *I-V* model for DG MOSFETs, which is derived from closed-form solutions of Poisson's equation, and current continuity equation without the charge-sheet approximation. A complete compact model of FinFETs with the DG MOSFET model has been implemented in SPICE. With cylindrical symmetry, the long channel model of surrounding-gate (SG) can be built based on solving 1-D Poisson's equation. Quadruple-gate (QG) MOSFETs resemble SG MOSFET in many aspects. The *I-V* analytical model of TG FinFETs can be derived based on DG and QG *I-V* model [12].

Short channel effects model. Short channel effects (SCEs) have become a significant issue with the continuous scaling of CMOS technology [13]. Xie et al. [14] published a three-dimensional (3-D) analytical model for SCEs in the nanoscale TG FinFET based on solving a boundary value problem using the 3-D Poisson's equation. This SCEs model can be used to predict the minimum channel length (L_{min}) of a device under the requirement of keeping SCEs at a tolerable level. Based on the analytical model, the insights into the physics of SCEs in nanoscale TG FinFET are discussed, and design considerations are investigated.

GER and FER model. Gate edge roughness (GER) and Fin edge roughness (FER) are two key variability sources in FinFET technology. Jiang et al. [15] proposed a predictive model of GER and FER for the first time. This work well captures the inherent correlations between the variations of device electrical parameters, efficiently predicts that the impacts of GER and FER on circuits are for 16/14 nm node and beyond, and provides helpful guidelines for variation-aware design and technology process development. The GER and FER model has been incorporated into industry standard BSIM-CMG core model.

FinFETs have attracted considerable scholarly attention since proposed around 2000. FinFETs with silicon as the channel material have been adopted by industry, and have achieved high transistor performance and density, which marked the semiconductor industry stepping from conventional 2-D planer world into novel 3-D world. The performance of FinFETs can be increased by adopting novel channel materials. FinFETs with III-V high mobility material and TMD as channel materials have been proposed and demonstrated. Besides experimental demonstration, analytical model plays an important role in the aspects of depicting the physical insight of device and predicting the future device development trend. Completed compact model of FinFETs with the DG MOSFET model including short-channel and quantum mechanical effects has been implemented in SPICE, and the GER and FER model has been integrated into industry standard BSIM-CMG core model.

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