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Carbon nanotube transistors with graphene oxide films as gate dielectrics†

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Carbon nanomaterials, including the one-dimensional (1-D) carbon nanotube (CNT) and two-dimensional (2-D) graphene, are heralded as ideal candidates for next generation nanoelectronics. An essential component for the development of advanced nanoelectronics devices is processing-compatible oxide. Here, in analogy to the widespread use of silicon dioxide (SiO_2) in silicon microelectronic industry, we report the proof-of-principle use of graphite oxide (GO) as a gate dielectrics for CNT field-effect transistor (FET) via a fast and simple solution-based processing in the ambient condition. The exceptional transistor characteristics, including low operation voltage (2 V), high carrier mobility (950 cm^2/V^{-1} s^{-1}), and the negligible gate hysteresis, suggest a potential route to the future all-carbon nanoelectronics.

carbon-based nanoelectronics, graphene oxide, gate dielectrics

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1 Introduction

The realization of encountering both of its technological and physical limitations of silicon metal-oxide-semiconductor field-effect transistor (MOSFET), the modern workhorse of semiconductor industry, has inspired a worldwide effort to develop alternative nanomaterials and device technologies [1]. One of the approaches is to retain the operating principles of the currently used FET, but replace the conventional silicon conducting channel with carbon nanomaterials, such as carbon nanotubes (CNTs) [2–14] and, most recently, graphene [15–18]. Since the pioneering work of Dekker and coworkers [3], CNT-FETs have witnessed tremendous advancements in both device fabrication and characteristics. One of the utmost significant developments in device fabrication is that the gate dielectrics have moved from silicon dioxide (SiO_2) to high-κ dielectrics such as ZrO_2, HfO_2, and Al_2O_3, which delivers high-performance transistors with low voltage and possibly hysteresis-free operation [9,12,13]. On the other hand, several powerful conventional thin-film deposition methods are, however, incompatible with nanotube electronics, i.e., deposition of SiO_2 on nanotubes by sputtering or plasma-enhanced chemical vapor deposition (PECVD) resulted in loss of electrical connection in nanotube devices due to sputtering damage [13]. Yet achieving the compatibility of atomic layer deposition (ALD) with nanotubes is a challenge as well, if its covalent coating nature and the inevitable preparation of hydrophilic nanotube surfaces prior to deposition are considered, both of which conflict with the essential requirements for reserving the pristine electrical properties of nanotubes [11]. To improve the film quality, an increase in the deposition temperature (sometimes higher than 300°C) is also required in ALD, and usually an oxidative H_2O and ion species that will obviously do harm to nanotubes are involved. For these reasons, these sensitive nanotubes easily experience electrical property

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degradation due to structure defects induced during dielectrics deposition, despite exceptional device characteristics have been demonstrated for nanotube transistors with ALD dielectrics.

Graphite oxide (GO) [19–25] with insulating properties can be obtained by oxidizing graphite. Compared with previous reported oxide dielectrics, mono- or few-layer GO films can be deposited and bonded to various substrates through weak non-covalent interactions by solution-based processing at low temperatures [26], which will meet the technological challenges for delivering low-cost, thin dielectric material layers that are inherently compatible with nanotube electronics. So it is a fair question to ask, for carbon-based nanoelectronics, whether the dielectric properties of GO are good enough to act as the equivalence of the widely used SiO_2 in silicon industry, which has strongly supported the evolution and bloom of the silicon MOSFETs during the past decades [27].

In this paper, we reported the electric and dielectric properties of GO films in its out-of-plane direction. And in analogy to the widespread application of silicon dioxide (SiO_2) in silicon microelectronic industry, we demonstrated the proof-of-principle use of high-κ (~12) graphite oxide (GO) thin films (~4 nm) as gate dielectrics for CNT field-effect transistors (FETs) via a fast and simple solution-based processing in ambient condition. The *p*-type transistors exhibited exceptional device characteristics, including high carrier mobility (950 $cm^2\ V^{-1}\ s^{-1}$), low operation voltage (2 V), and greatly reduced gate hysteresis. What is more significant, our solution-based approach affords GO gate insulators with high capacitance while being intrinsically and chemically benign to nanotubes due to its non-covalent coating nature, thus indicating a viable manufacturing technology for future all-carbon nanoelectronics.

2 Experimental methods

2.1 Preparation of GO films

Oxidation of graphite was carried out from nature graphite flakes (325 mesh) by the modified Hummer's method [28,29]. A stable yellow-brown GO in 1:1 water and ethanol mixed suspension (1 mg mL^{-1}) was readily obtained by exfoliation of GO through ultrasonic treatment. Uniform GO thin films can then be reproducibly deposited onto the required substrate via a facile spin-coating process by using the as-prepared GO aqueous dispersions [30]. The unreduced GO is known to have a sheet resistance in the G-range [25]. However, its out-of-plane electronic properties, which are essential for assessing its potential usage as a gate insulator, have seldom been characterized. In order to test the out-of-plane electrical properties of the GO, we deposited ultra-thin GO films onto $Pt/SiO_2/Si$ or SiO_2/Si substrates during spin-casting (4000 r/min) by pipette. The volume of individual droplets released every time was approximately 20 μL. The GO droplets would spread across the surface of the substrate immediately, and dried within a few seconds. The thickness of the GO thin films was controlled on a nanometer level by either varying the concentration of GO in the solution between 0.1 mg/mL to 10 mg/mL, or counting the droplets of the solution. In our experiments, continuous GO thin films with thickness as thin as 3 nm (corresponding to 4–5 monolayers) could be easily achieved with root-mean-square (RMS) roughness about 1 nm as examined by atomic force microscopy (AFM).

2.2 Electrical measurement of GO Films

After the patterning of top electrode (3×3 μm with 1 μm separation) arrays onto $GO/Pt/SiO_2/Si$ substrate, the bottom $Pt/SiO_2/Si$ electrode was grounded, and a Lakeshore commercial tungsten probe with a diameter less than 10 μm was used to perform electrical measurement of the GO capacitors by a random selection of top electrodes. The efficiency of measurements was confirmed by further scanning electron microscopy (SEM) images, which showed a press mark of less than 1 μm size on top electrodes. The *in-situ* high vacuum electrical measurement was performed in a 4-probe scanning tunneling microscopy (STM) chamber under base pressure $<2\times10^{-10}$ torr with an equipped Keithley joint setup. The STM tips were used to directly probe the top electrode current with applied back gate voltage.

2.3 Fabrication of CNT field-effect transistors

CNTs used in this work were synthesized by patterned CVD growth on SiO_2/Si substrates using powdery MgO-supported Fe-Mo bimetallic catalyst island, after which Electron beam lithograph (EBL) was applied to pattern S and D electrodes with 1–2 μm separation to fabricate the original CNT-FET devices. Pd was used for S/D electrodes deposition, which is a well-known metal for achieving high-quality Ohmic contact with nanotubes.

3 Results and discussion

Figure 1(a) shows an AFM image of a corner of the resultant GO film. Pinhole-free multilayered structures with curvatures can be readily seen. The film thickness is estimated to be 4–6 nm, measured by using AFM at the edge of the film. EBL, Pt deposition and a lift-off technique were then used for top electrode (3×3 μm) arrays patterning, thus fabricating micrometer-scale capacitors with ultra-thin GO insulator sandwiched between Pt electrodes. Before measurements, the capacitor devices were baked at 120°C for 4 hours to minimize potential charge traps (such as water molecules) adsorption onto surfaces. Electrical testing was performed by using a B1500A semiconductor analyzer at

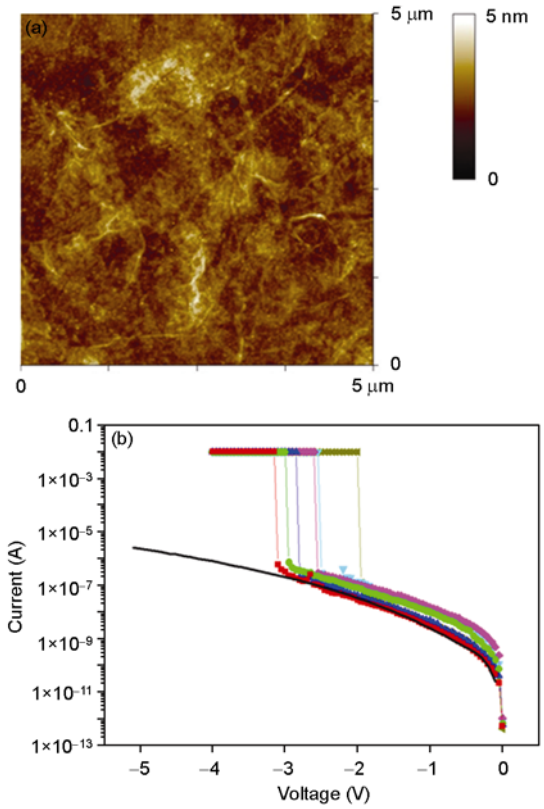

Figure 1 (a) The AFM image of multi-layer GO film deposited on the Pt/SiO_2/Si substrate. (b) Bias dependent leakage current (*I-V*) curves of up to 7 different capacitor devices measured under dry air and vacuum, respectively. The colored ones were recorded in dry air, while the black line was recorded in high vacuum ~1×10^{-9} torr.

room temperature in dry air.

For the sake of characterizing the electrical properties of GO films, we applied a bias to the top electrode of the capacitor, with the bottom electrode grounded. Figure 1(b) shows the bias dependent leakage current (*I-V*) curves of seven devices. The colored ones were recorded in dry air, while the black line was recorded in high vacuum ~1×10^{-9} torr. Insulating properties are observed for all the GO capacitors. A promising electrical behavior in dry air indicates that the dielectric breakdown of the ultra-thin GO films in the out-of-plane direction only occurs at a bias field larger than 3 MV cm^{-1}, sometimes as high as 5 MV cm^{-1}. Such a high dielectric breakdown field is comparable with that of high-quality oxide dielectrics fabricated by using the state-of-the-art ALD method. While when the GO capacitors were measured in high vacuum, no breakdown was found even at 8 MV/cm with a large leakage current in a range of microampere (corresponding to a current density of 25 A cm^{-2}), showing the oxidation nature for GO breakdown mechanism in dry air. The leakage current density can be deduced as 1×10^{-2} A cm^{-2} at 1 MV cm^{-1} bias field, and on the order of 1 A cm^{-2} before the dielectric breakdown. The significantly large leakage current density (which is several orders of magnitude larger than that (10^{-6}–10^{-8} A cm^{-2}) of high-quality oxide dielectrics) could be due to the non-uniform thickness of the GO layer, as shown in Figure 1(a). As a result, the tunneling current could dominate at the place where single layer GO with sub-nanometer thickness is present. We expect much smaller leakage current in our nanoscale devices considering both the nanometer diameter of the tube and the thickness uniformity of the GO layers at such a small size scale.

We have also evaluated the out-of-plane dielectric properties of GO film by fabricating well-oriented GO paper as shown in Figure 2(a). Typical bias dependent dielectric constant (*C-V* curve) of four oriented GO paper sandwiched capacitors shows that the dielectric constant of the GO paper in its out-of-plane direction is bias independent and could be as large as 12 (Figure 2(b)). Moreover, as the bias sweeps upwards (from negative to positive) and downwards continuously, the *C-V* curves exhibit no obvious hysteresis loops, indicating a low electrical trap density of the GO dielectrics. Although GO intrinsically contains many defects induced during oxidization, the hysteric-free characteristics of the *C-V* curves are probably due to the passivation of these defects by oxygen. These preliminary out-of-plane electrical and dielectric properties of GO films, i.e., insulating electrical behavior with a dielectric breakdown field up to 5 MV cm^{-1} and a high dielectric constant around 12, strongly suggest that they are promising candidates as nanoscale dielectrics.

For the construction of CNT-FET devices with GO

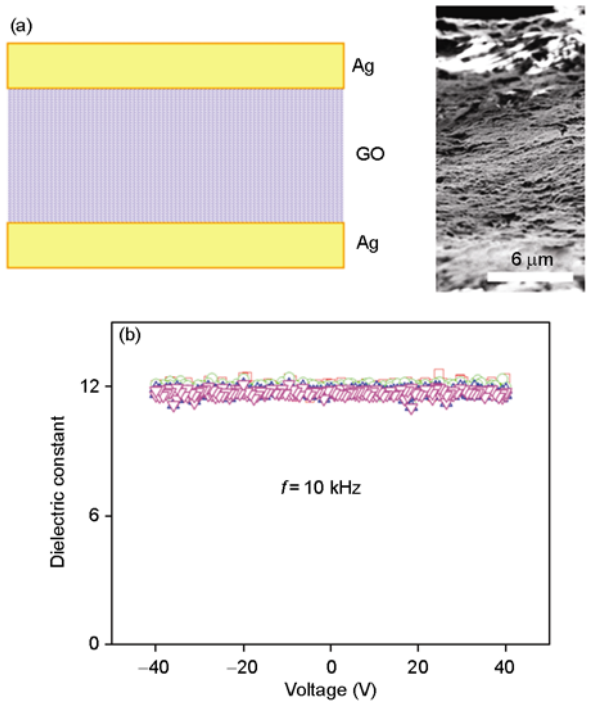

Figure 2 (a) A scheme and a cross-section SEM image of the fabricated capacitor with 20-μm-thick oriented GO paper sandwiched between two Ag electrodes. (b) Typical bias dependent dielectric constant (*C-V*) curves of the oriented GO paper.

dielectrics, we first carried out CVD growth of CNTs on SiO_2/Si substrate with patterned catalyst islands. Source (S) and drain (D) Pd electrodes were then patterned by using EBL. A FET device fortuitously composed of an individual semiconducting CNT is shown schematically in Figures 3(a)–(c), where the ultra-thin GO films are dispersed onto the CNT-FET device through a standard spin coating process. In order to avoid tunneling current in sub-nanometer scale (which is just the thickness of mono-layer GO film), the concentration of GO solution and the times of spin coating process are controlled to obtain few-layer GO films instead of mono-layer ones. Further AFM images show the micrometer-scale GO flakes with a thickness in the range of 3–4 nm (corresponding to 4–6 layer GO films). Top-gate electrodes (G) made of Pt were then patterned onto the GO covered single CNT (between the S and D electrodes) for the transistor (Figure 3(c)). Figure 3(d) is a typical SEM image of the as-fabricated CNT-FETs with top-gate GO dielectrics. Figure 3(e) is the zoom in of the rectangle area of Figure 3(d), showing the nanotube conduction channel underneath the GO films, as imaged by AFM. Again, a four-hour baking at 120°C is performed before transport measurements to minimize absorbed water molecules.

Figure 4(a) gives the typical current (I_D) versus gate voltage (V_G) characteristics (V_D=10 mV) evolution of the *p*-type nanotube transistor before (black triangle) and after (blue circle) the fabrication of the Pt/GO gate stacks. The enlarged I_D-V_G curve of the top-gated nanotube transistor with GO dielectrics is shown in Figure 4(b). Obviously, the on-state current of the top-gated transistor is similar to its back-gated counterpart that did not undergo GO coating. We can analyze the effective carrier mobility of our top-gated CNT-FET with GO dielectrics based on the standard transistor model [31]. The effective carrier mobility is deduced as over 950 $cm^2\ V^{-1}\ s^{-1}$, which is more than 2 times higher than that of *p*-type bulk crystalline Si (~450 $cm^2\ V^{-1}\ s^{-1}$), indicating its promise for the transistor applications. These observations clearly show that the GO films non-covalently assembled through solution processing are chemically benign to the nanotubes, a key to the integration of advanced dielectrics into nanotube electronics.

As shown in Figure 4(b), it is obvious that the operation voltage of the top-gated devices (less than 2 V) is significantly smaller than that of the back-gated one (as high as 40 V). Moreover, unlike its back-gated counterpart, the transfer characteristics of the top-gated FETs show negligible gate hysteresis when the gate voltage sweeps upwards (from negative to positive) and downwards continuously. Such a large reduction in hysteresis is in agreement with the superposition of *C*-*V* loops measured in Figure 2(b), indicating a nanotube/GO interface with a low electrical trap density. The leakage current between the nanotube and the top Pt gate is negligible (<0.05 nA) with the operation voltage up to 2 V, as expected. We notice here that these electrical characteristics are well reproducible in more than twenty devices fabricated from different batches of chips that

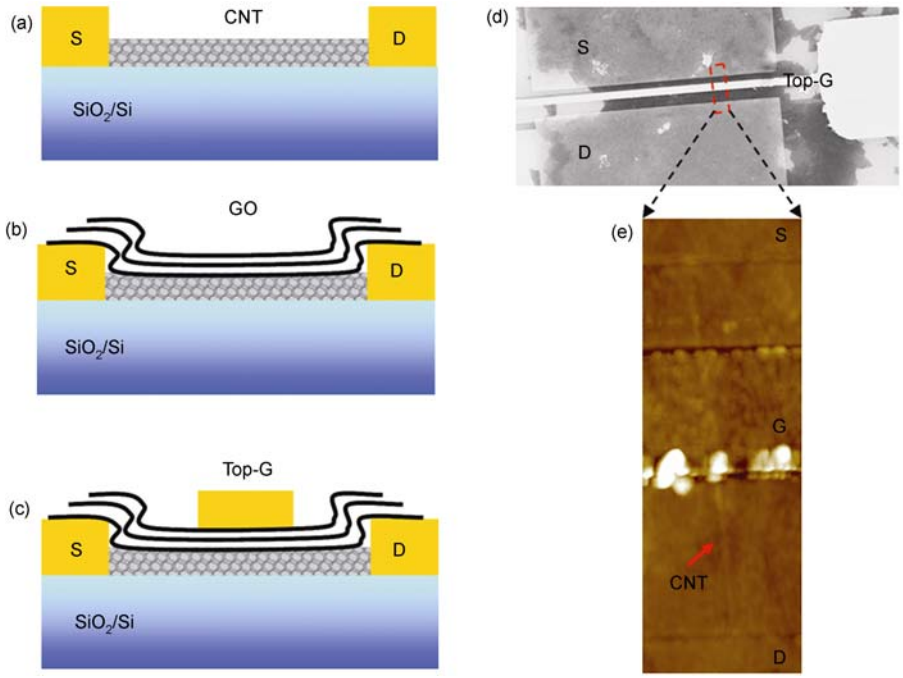

Figure 3 (a)–(c) Schemes of the construction of a CNT-FET with GO gate dielectrics. (a) A FET device fortuitously composed of an individual semiconducting CNT. (b) Ultra-thin GO films are dispersed onto the CNT-FET device through a spin-on processing. (c) The top electrode (G) made of Pt is patterned onto the GO covered CNT by using EBL. (d) An SEM image of the as-fabricated CNT-FET with GO gate dielectrics. (e) An enlarged image of the rectangle area of (d), imaged by AFM.

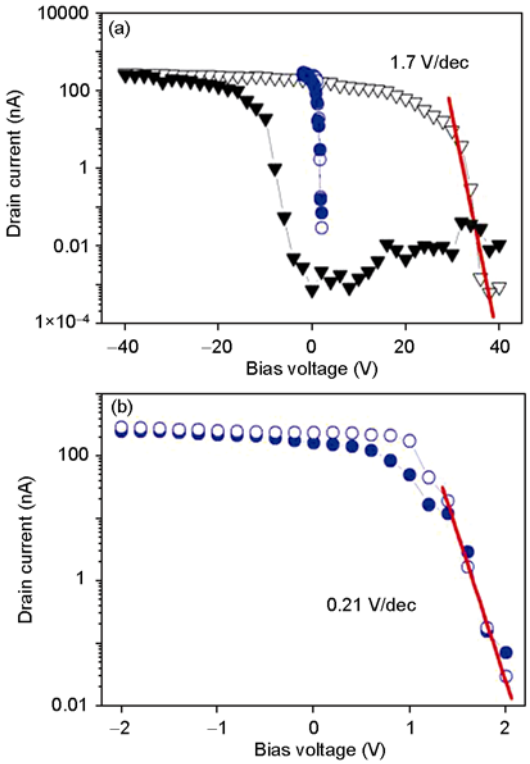

Figure 4 (a) Typical transfer characteristics (I_D-V_G curve at V_D=10 mV) evolution of the *p*-type nanotube transistor before (black triangle) and after (blue circle) the fabrication of the Pt/GO gate stacks. Gate voltages are swept upwards (from negative to positive) and downwards continuously for both cases. Back-gated FET shows the wide hysteresis loop, while no obvious loop is found for the top-gated FET. (b) The enlarged transfer characteristics of the CNT-FET with GO top-gate dielectrics.

experience independent nanotube growth, GO coating and EBL processes. This fact clearly reveals that the exceptional pristine merits of nanotubes are well-retained and possible interface electrical trap between the nanotube and GO dielectrics can be greatly suppressed by careful handling. However, compared with the room-temperature theoretical limit of the subthreshold swing for field-effect transistors (60 mV dec^{-1}), the obtained subthreshold swing of our typical top-gated device (S=ln(10)[dV_G/d(lnI_D)]=210 mV dec^{-1}) is not ideally steep, although it indeed steeps drastically in comparison with that of ~1.7 V dec^{-1} for the back-gated one. Further studies are needed to clarify whether this non-ideal subthreshold swing is due to the unpassivated defect states of GO thin films.

4 Conclusion

Insulating properties in the out-of-plane direction of ultra-thin GO films are studied, and the usage of GO films as gate dielectrics for CNT-FETs is demonstrated for the first time. The exceptional device characteristics, including high carrier mobility (950 cm^2 V^{-1} s^{-1}), low operation voltage (2 V), and largely reduced gate hysteresis, along with the simple solution-based non-covalent GO coating process, suggest the potential of nanoscale GO dielectrics for carbon-based electronics, aiming at future all-carbon nanoelectronics. Considering the room-temperature processing and inherent mechanical robustness, the GO film dielectrics could be promising for flexible electronics as well.

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