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# Flexible printed three dimensional (3D) integrated carbon nanotube complementary metal oxide semiconductor (CMOS) thin film transistors and circuits

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**Abstract** The threshold voltage modulation of carbon nanotube thin-film transistors (TFTs) and flexible three-dimensional (3D) integration circuits has become hot research topics for carbon-based electronics. In this paper, a doping-free gate electrode technology is introduced to significantly modulate the threshold voltage of polymer-sorted semiconducting single-walled carbon nanotube (sc-SWCNT) TFTs in combination with the highly effective gate-controlling ability of solid-state electrolyte thin films as the dielectrics. A systematic investigation was conducted on the impact of printed silver, evaporated silver, and evaporated aluminum (Al) gate electrodes on the threshold voltage of flexible printed bottom-gate and top-gate SWCNT TFTs. The results indicate that the SWCNT TFTs with Al gate electrodes exhibit enhancement-mode characteristics with excellent electrical properties, such as the negative threshold voltages (−0.6 V), high $I_{on}/I_{off}$ (up to $10^6$), low subthreshold swing (61.4 mV · dec$^{-1}$), and small hysteresis. It is attributed to either the formation of lower work function thin films ($Al_2O_3$) at the electrode/dielectric layer interfaces through the natural oxidation of the Al bottom-gate electrodes or the dipole reaction of the Al top-gate electrodes from X-ray photoelectron spectroscopy (XPS) and ultraviolet photoelectron spectroscopy (UPS) data. In addition, 3D complementary metal-oxide-semiconductor (CMOS) inverters with common gate electrodes were constructed using the resulting enhancement-mode P-type SWCNT TFTs and matched N-type SWCNT TFTs, which shows high voltage gain (34), rail-to-rail output and high noise margins (80.04%, $V_{DD} = -1$ V) as well good mechanical flexibility at low operation voltages. It demonstrates that SWCNT TFTs have great advantages for building large-scale 3D flexible integrated circuits.

**Keywords** three-dimensional CMOS circuits, printing technology, polymer-sorted semiconducting carbon nanotubes, enhancement-mode thin-film transistors, threshold voltage modulation

## 1 Introduction

Based on their large area, flexibility, low cost, and other characteristics, printed electronics are developing rapidly for their applications in flexible displays [1, 2], health detection sensors [3, 4], and smart wearable electronics [5]. Among them, printed thin-film transistors (TFTs) play a vital role as the core of electronic circuits and have received more and more attention. The intrinsic properties of the channel materials have a significant impact on the electrical properties of printed TFTs. It has been demonstrated that semiconducting single-walled carbon nanotubes (sc-SWCNTs) are the primary option for manufacturing flexible printed TFTs due to their high carrier mobility, remarkable mechanical flexibility, low processing temperature, exceptional physical and chemical stability, and high solubility and stability

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after modification by polymers and surfactants [6–16]. However, depletion-type characteristics are consistently exhibited in solution-processable SWCNT TFTs, resulting in increased power consumption in carbon-based electronics and circuits.

To overcome this deficiency, developing effective methods for adjusting the threshold voltage to obtain the enhancement-type printed SWCNT TFTs is necessary. The threshold voltage can be regulated by lowering the work function of the gate electrodes by functionalizing the electrode surface and using low-work-function metal electrodes. In general, the threshold voltage is not only related to the work function of the gate electrodes but also the capacitance value of the dielectric layer and the presence of defects. So, it is easier to obtain enhancement-mode p-type SWCNT TFTs with the smaller gate work function, the larger capacitance value of the dielectric layer, and the fewer defects in the dielectric layer. Various methods are reported to adjust the threshold voltage range of transistors, including using double-gated transistors [17, 18], adjusting the W/L ratio [19, 20], chemical doping [21–25], tuning the work function of the gate electrodes by self-assembling [26], and using floating gate structures [27–29]. However, most of them suffer from the increased power consumption [30], larger circuit area, and more complicated fabrication process. Therefore, it is imperative to develop simple and efficient approaches for constructing high-performance enhancement-mode printed SWCNT TFTs. Furthermore, the accuracy (10–100 μm) and feature size (100–200 μm) [31] of the present printing technology limit the integration density of printed circuits in the horizontal direction. As a research hotspot in the field of integrated circuits, three-dimensional (3D) integration technology has good compatibility with printing technology, which can considerably improve the integration density of printed circuits in vertical directions and shorten the interconnection lines [32–35].

Here, we developed a new approach to achieve enhancement-mode flexible printed top-gate and bottom-gate SWCNT TFTs with excellent electrical properties when using aluminum (Al) gate electrodes and the high capacitance ion liquids-poly(4-vinylphenol (IL-c-PVP)) as the dielectrics. The SWCNT TFTs with Al electrodes as bottom gates show threshold voltages of −0.2 V with the subthreshold swing (SS) of 87.9 mV $\cdot$ dec$^{-1}$, on/off ratios of $10^6$, small hysteresis, and Al top-gate devices showed more negative threshold voltages (−0.6 V), smaller SS (61.4 mV $\cdot$ dec$^{-1}$), and similar on/off ratios. It is worth noting that the threshold voltage of printed top-gate SWCNT TFTs can shift significantly from 0.6 to −0.6 V. Furthermore, the 3D complementary metal-oxide-semiconductor (CMOS) inverters based on the enhancement-mode SWCNT TFTs were fabricated using the common-gate structure. The inverters exhibit excellent performance with a maximum voltage gain of 34 at low voltages ($V_{\rm DD}$ = −1.5 V), rail-to-rail output properties, a high static noise margin (80.04%), the peak power consumption of 14.1 nW at $V_{\rm DD}$ of −0.5 V.

## 2 Experimental

### 2.1 Materials and instruments

Arc discharge SWCNTs containing metallic and semiconducting nanotubes were purchased from Shanghai University. The poly (9, 9-dioctylfluorene) derivative (PFIID) (Mn = 6527, Mw = 10686, PDI = 1.637) for sorting semiconductor SWCNTs and printable conductive silver nanoparticle inks were synthesized and prepared by our laboratory [36]. The polarity conversion ink consisting of epoxy resin (128) and the cross-linking agent (F51) were obtained from Xuzhou Zhongyan Technology (China). Ionic liquids (ILs [EMIM] [TFSI]) were purchased from Shanghai Cheng Jie Chemical Co. LTD. Other chemical compounds, such as poly(4-vinylphenol) (PVP) (Mn = 25 kg $\cdot$ mol$^{-1}$), poly(melamine-co-formaldehyde) (PMF) (Mn = 423 g $\cdot$ mol$^{-1}$), and propylene glycol monomethyl ether acetate (PGMEA), were obtained from Sigma. Optical absorption of purified sc-SWCNT inks was measured through a UV-Vis-NIR spectrometer (Perkin Elmer Lambda 750, Inc., USA). The surface morphology of sc-SWCNTs was characterized by Scanning Electron Microscope (SEM, Nova NanoSEM450). X-ray photoelectron spectroscopy (XPS) and ultraviolet photoelectron spectroscopy (UPS) analysis were carried out in a PHI 5000 Versaprobe using Al Ka radiation (1486.6 eV) and He I radiation (21.22 eV), respectively, to investigate chemical compositions and the work functions of the Al gate electrodes. Inkjet printers with model DMP-2831 (Dimatix, USA) and aerosol jet printers (Optomac Inc.) were used for the design and construction of flexible TFTs and logic circuits. All the electrical measurements were carried out by Keithley 2636-SCS or 4200-SCS in ambient conditions. The carrier mobility of SWCNT TFT devices is derived from the standard

formula [37] for the linear region.

$$\mu = \left(\frac{\mathrm{d}I_{\mathrm{D}}}{\mathrm{d}V_{\mathrm{gs}}}\right) \times \frac{L}{W} \times \frac{1}{V_{\mathrm{ds}}C_i}, \tag{1}$$

where $L$, $W$, and $C_i$ represent the channel length (85 μm) and width (120 μm), and the measured areal capacitance for IL-c-PVP dielectrics. The main components of the IL-c-PVP are the mixture of PVP and ILs. The chemical structures are shown in Figure S1(a). Figures S1(b) and (c) show the schematic diagram for measuring the areal capacitance of IL-c-PVP dielectrics and the calculated capacitance value, respectively. Where the capacitance value of 4.7 $\mu\mathrm{F} \cdot \mathrm{cm}^{-2}$ was measured at a frequency of 0.1 Hz. The input signals were produced by a dual-channel arbitrary function generator (Model: Tektronix AFG 3052C).

### 2.2 Preparations of sc-SWCNT inks

6 mg of SWCNTs (purchased from Shanghai University) and 3.6 mg of PFIID (poly (9, 9-dioctylfluorene) derivative, Mn = 6527, Mw = 10686, PDI = 1.637) were dissolved in 10 mL of toluene, which was dispersed uniformly by an ultrasonic probe (Sonics & Materials Inc., Model: VCX 130, 70 W) for 30 min. After that, the dispersed solution was placed in a high-speed centrifuge for 1 h at 10000 $\mathrm{r} \cdot \mathrm{min}^{-1}$, followed by 1 h at 40000 $\mathrm{r} \cdot \mathrm{min}^{-1}$, to remove metallic carbon nanotubes and insoluble impurities. Finally, the high-purity supernatant was extracted to obtain sc-SWCNTs ink. The obtained solution was used for the preparation of carbon nanotube thin film transistors without further purification.

### 2.3 Preparation of IL-c-PVP inks

To completely dissolve the PVP (poly(4-vinylphenol), Mn = 25 $\mathrm{kg} \cdot \mathrm{mol}^{-1}$) powder, 0.223 g of PVP dissolved in 2 mL of PGMEA solution was placed on a hotplate with a magnetic stirrer. The hotplate and stirrer were set to 90°C and 1000 $\mathrm{r} \cdot \mathrm{min}^{-1}$, respectively. The mixture was stirred for 20 min to ensure complete dissolution of the PVP powder. The clarified solution was then cooled down to room temperature. The mixture was then stirred for 30 min after the addition of 0.07 g of PMF to obtain a c-PVP solution. Finally, 36 mg of the ionic liquids (ILs [EMIM][TFSI], purchased from Shanghai Cheng Jie Chemical Co. LTD.) mixed with 1 mL of c-PVP solution was stirred thoroughly to obtain IL-c-PVP solution as the dielectric layer of the SWCNT TFTs.

### 2.4 Fabrication of SWCNT TFTs and common-gate 3D CMOS inverters

Figures 1(a) and (b) show the manufacturing process of CMOS circuits based on sc-SWCNTs and the corresponding optical photographs. The top-gate/top-contact SWCNT TFTs at the bottom layer are P-type, and the bottom-gate/top-contact SWCNT TFTs at the upper layer are N-type. The top-gate/top-contact SWCNT TFTs were firstly prepared on a flexible PI substrate, and then, the bottom-gate/top-contact SWCNT TFTs were constructed on the top-gate SWCNT TFT devices. After that, the bottom-gate SWCNT TFT devices at the top layer were transformed from P-type to N-type by depositing epoxy resin in device channels. Finally, the drain electrodes of the N-type devices were connected to the drain electrodes of the P-type devices to form CMOS inverters.

The specific steps for preparing the top-gate/top-contact SWCNT TFT devices are as follows. In the first step, a layer of c-PVP solution was spin-coated on a rough PI substrate as a flat layer of PI and an adhesion layer of sc-SWCNTs (1600 $\mathrm{r} \cdot \mathrm{min}^{-1}$ for 45 s and annealed at 180°C for 90 min). The samples were then subjected to UV-ozone treatment for 3 min to increase the immobilization efficiency between sc-SWCNTs and the c-PVP. In the second step, sc-SWCNT inks were deposited to form patterned active layers with an aerosol jet printer (after annealed at 120°C for 3 min); after cooling, excess polymer impurities were cleaned off using toluene and annealed again at 120°C for 30 min to further solidify the carbon nanotube sites. In the third step, silver nanoparticle inks were deposited onto the channel region of the sample to construct the source/drain electrodes via the DMP-2831 (after annealing at 150°C for 30 min to improve the printed Ag electrode conductivity). In the fourth step, the IL-c-PVP inks were spin-coated onto the samples (1600 $\mathrm{r} \cdot \mathrm{min}^{-1}$ for 45 s) and the samples were annealed at 180°C for 90 min to form gate dielectric layers with high capacitance. In the fifth step, the patterned mask plates were placed on top of the samples, and the skeletonized area was aligned with the source-drain channel, after which the samples were placed in a vacuum coater to vaporize 120-nm-thick Al gate electrodes. After that, the top-gate/top-contact SWCNT TFT devices are ready.

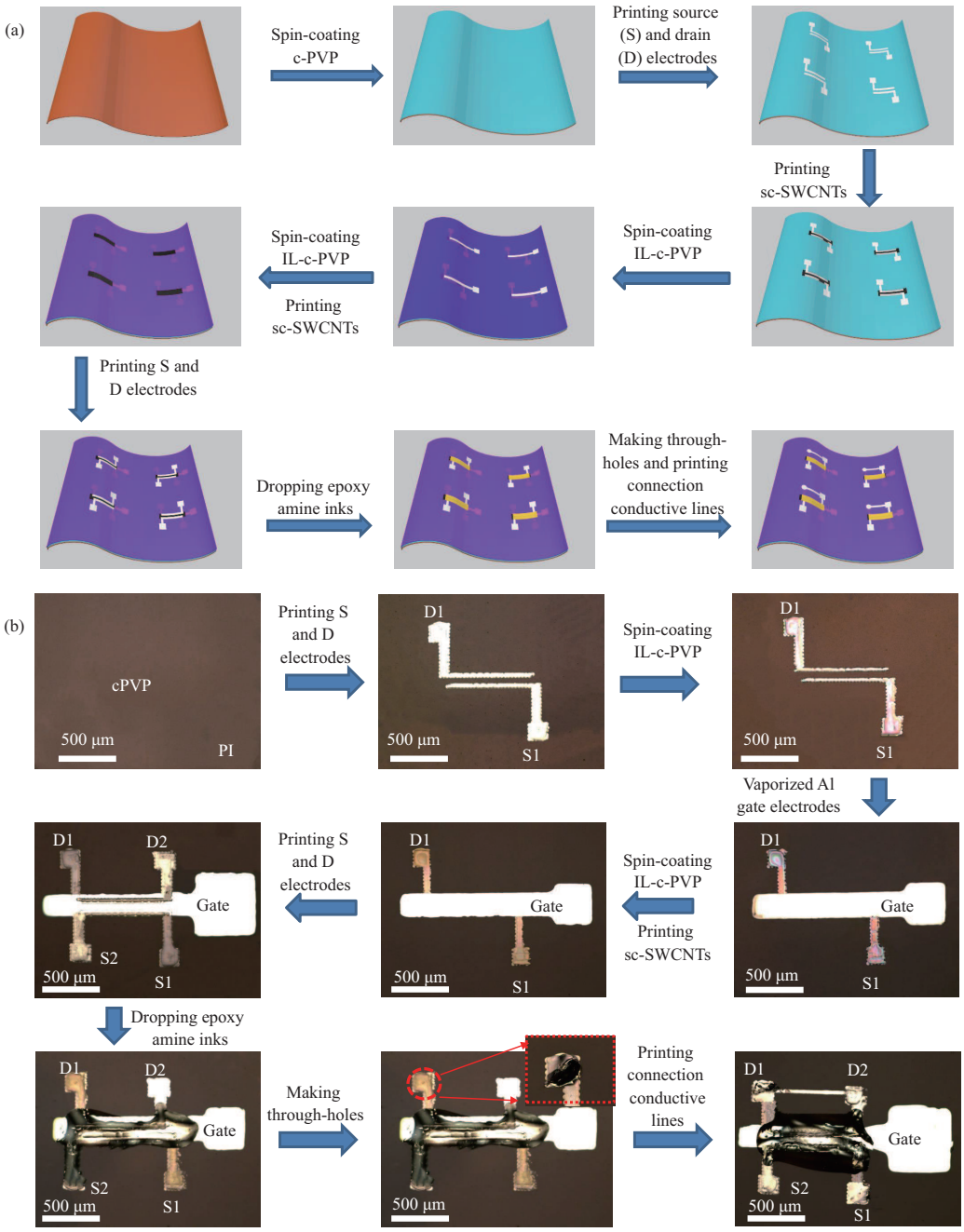


**Figure 1** (Color online) The preparation process of 3D CMOS inverters. (a) Fabrication process and (b) corresponding optical images in the manufacturing process of printed sc-SWCNTs CMOS inverters on PI substrates.

Next, the bottom-gate/top-contact devices were prepared. Here, Al gate electrodes of top-gate/top-contact SWCNT TFTs act as the bottom gates of the bottom-gate/top-contact SWCNT TFT devices. Since it is a common-gate structure, the next step is to spin-coat IL-c-PVP inks (1600 r $\cdot$ min$^{-1}$ for 45 s) directly on Al gate electrodes and obtain the dielectric layers (annealed at 180° for 90 min) of the bottom-gate/top-contact SWCNT TFT devices. The following preparation processes of the active layers and source/drain electrodes are exactly the same as those of the top-gate/top-contact devices. Electron-doping epoxy amine inks were then applied to the device channels of the bottom-gate/top-contact SWCNT TFT devices to obtain N-type SWCNT TFT devices. The through-holes were prepared by laser drilling shown in Figure 1(b), and 3D common-gate CMOS inverters were connected by silver conductive lines printed by an inkjet printer.

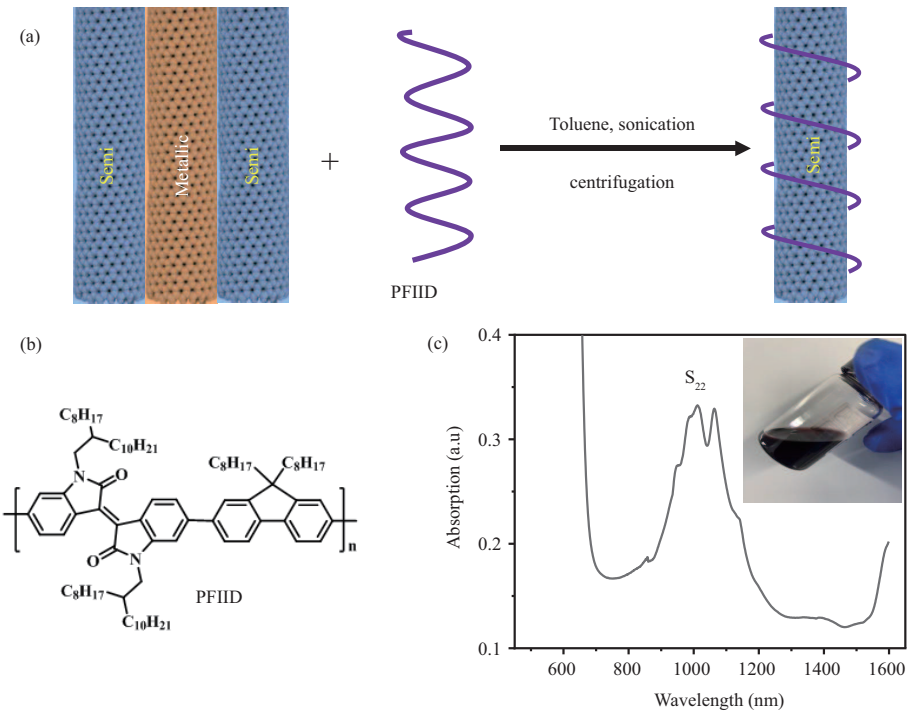


**Figure 2** (Color online) Process for sorting sc-SWCNTs by polymer wrapping. (a) Preparation principle of sc-SWCNT inks; (b) chemical structure of PFIID; (c) absorption spectrum and optical image of sorted sc-SWCNT suspension by PFIID.

## 3 Results and discussion

### 3.1 Characterization of sorted SWCNT inks and electrical properties of enhancement-mode SWCNT TFTs

As SWCNT TFTs based on polymer-sorted sc-SWCNTs exhibit excellent electrical properties, polymer wrapping is one of the ideal methods to sort sc-SWCNTs from commercial SWCNTs [32–35]. Figure 2(a) shows the schematic diagram of the preparation method of sc-SWCNT ink, in which sc-SWCNTs are selectively wrapped and sorted from commercial arc discharge SWCNTs by conjugated organic polymers, and the sc-SWCNT inks can be obtained after sonication and high-speed centrifugation. Figure 2(b) illustrates the chemical structure of the polymer (PFIID) used to wrap and separate sc-SWCNTs. UV-Vis-NIR spectroscopy is widely used to analyze whether the metallic carbon nanotubes are effectively removed from the raw SWCNTs. Figure 2(c) shows the UV-Vis-NIR absorption spectrum of sc-SWCNT ink after separation and purification. It can be seen that there are obvious peaks protruding in the range of 800–1300 nm, which belong to the absorption peaks of sc-SWCNTs ($S_{22}$). Whereas, in the range of 700–800 nm, no distinct peaks can be observed, indicating the absence of metallic SWCNTs in the separated SWCNT ink.

The threshold voltage of the SWCNT TFTs is effectively tuned by using metal gate electrodes with different work functions [38]. Here, we investigated the effect of three kinds of gate electrodes (the printed and evaporated Ag, and the evaporated Al gate electrodes) on the threshold voltages of top-gate and bottom-gate devices with high capacitance IL-c-PVP dielectric layers. Figures 3(a) and (b) represent the typical device structures of the top-gate/top-contact and bottom-gate/top-contact TFT devices. Figure 3(c) shows the transfer characteristic curves of top-gate and bottom-gate SWCNT TFTs with the printed and evaporated Ag, and the evaporated Al gate electrodes. From Figure 3(c), the on/off ratios of the SWCNT TFT devices are at a level of about $\sim 10^6$, and the threshold voltages are 0.6 V (the evaporated Ag as the bottom gate), −0.1 V (the evaporated Al as the bottom gate), −0.6 V (the evaporated Al as the top gate), and 0.5 V (the printed Ag as the top gate and bottom gate), respectively. It demonstrates that SWCNT TFT devices with different metal electrodes exhibit distinct threshold voltages.

To verify it, the work functions of different metal electrodes were measured by using UPS, and calcu-

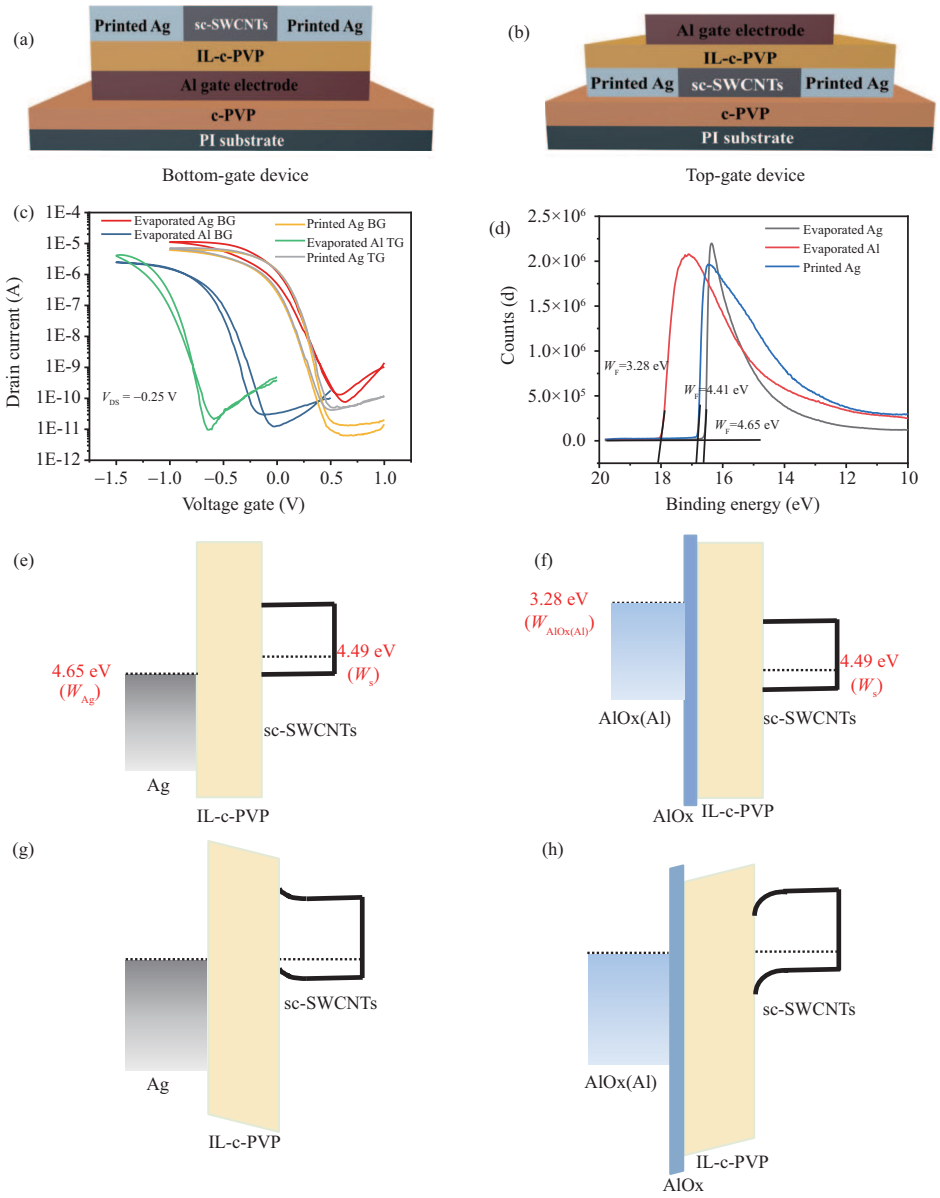


**Figure 3** (Color online) Structures and transfer characteristic curves of bottom-gate and top-gate SWCNT TFT devices with different metals as gate electrodes. Schematic diagrams of (a) bottom-gate and (b) top-gate SWCNT TFT structures. (c) Transfer characteristic curves of SWCNT TFTs with different metal gate electrodes (bottom-gate (BG) and top-gate (TG)). (d) The work functions of printed Ag, evaporated Al, and Ag electrodes. Vertical schematic energy band diagrams of the SWCNT TFTs with the Ag and Al gate electrodes ((e) and (f)) before and ((g) and (h)) after equilibration.

lated according to the equation [39]

$$\Phi = h\nu + E_{\text{cutoff}} - E_{\text{Fermi}}, \tag{2}$$

where $h\nu = 21.21$ eV, $E_{\text{cutoff}}$ refers to the secondary electron cut-off side energy level, and $E_{\text{Fermi}}$ refers to the Fermi energy level. Figure 3(d) shows the measured work functions corresponding to the gates exposed to air, respectively. The work functions of printed Ag, evaporated Ag and Al are 4.41, 4.65, and 3.28 eV, respectively. The threshold voltages of the top-gate and bottom-gate SWCNT TFTs using the printed Ag as the gate electrodes are essentially the same (0.5 V), while there is a notable difference in the threshold voltages between the top-gate and bottom-gate devices with the evaporated Al gates (−0.6 and −0.2 V). It is obvious that the threshold voltages of P-type transistors decrease with the work function decreases of the gate electrodes, which is consistent with that of the traditional metal-oxide-semiconductor

transistor given [40] by

$$V_{\rm th} = \frac{\Phi_{\rm MS}}{q} + 2\varphi_{\rm f} - \frac{Q_{\rm f}}{C_{\rm ox}} - \frac{Q_{\rm it}(2\varphi_{\rm f})}{C_{\rm ox}} - \frac{Q_{\rm B}(2\varphi_{\rm f})}{C_{\rm ox}}, \tag{3}$$

where $\Phi_{\rm MS}$ and $\varphi_{\rm f}$ represent the differences between the work function of the gate and semiconducting channel, and the Fermi level and intrinsic Fermi level of semiconductors, $Q_{\rm f}$, $Q_{\rm B}$, and $Q_{\rm it}$ are the fixed charge in the gate oxide layer and in the depletion region, and the interface trap at the semiconductor/dielectric interface, respectively, and $C_{\rm ox}$ is the oxide gate capacitance [38].

Generally, the Al electrode work function is about 4.20 eV. However, the measured Al gate work function in our experiments is 3.28 eV, which causes the threshold voltage of the Al gate P-type SWCNT TFT to negatively shift. The threshold voltage of the Al top-gate TFT (−0.6 V) is significantly more negative than that of the Al bottom-gate device (−0.2 V) as shown in Figure 3(c), due to the fact that the evaporated Al electrode of the bottom-gate TFT is naturally oxidized when exposed to air, resulting in the formation of the lower work function $Al_2O_3$ layer at the top of the Al gate (ranging from 3.2–3.8 eV due to different oxidation levels) and leading to a significant decrease of the work function from 4.2 to 3.28 eV [41]. As for the top-gate TFT with the Al gate electrode, the Al electrodes will not only be directly oxidized by oxygen but also interact with the ILs ([EMIM]X[TFSI]) at the Al/IL-c-PVP interface by taking the oxygen atoms from IL ([EMIM]X[TFSI]) (see Figure S1(a) for the chemical structure formula) to form the dense $Al_2O_3$ layers with low work function, resulting in more oxygen vacancy ($V_{\rm o}$) [42, 43], which is prone to form dipoles in the $Al_2O_3$ thin films. It is known from the literature that $V_{\rm th}$ can be modified by the interface charge impurities or dipoles in the dielectric layer [22, 44], which results in a more negative shift of the threshold voltage of the Al top-gate TFTs than that of Al bottom-gate TFTs.

Combined with the metal-semiconductor contact and their energy band diagram, we further study the reason for different threshold voltages of SWCNT TFTs with different work function gate electrodes. The work function of the sc-SWCNTs is around 4.49 eV [45], while the work function of silver is at 4.65 eV. It is noted that $Al_2O_3$ acts as not only the modification layer to reduce the work function of Al gate electrodes but also part of the whole dielectric. At the zero-gate bias, the energy band bends upward and holes tend to flow out of the sc-SWCNTs along with adjusting the sc-SWCNTs channel as a hole depletion channel, as shown in Figures 3(e) and (f). In contrast, for the Al gate electrode, the presence of an extremely thin $Al_2O_3$ film on the Al gate surface results in the decrease of the work function down to ∼3.28 eV and a downward bending of the energy band, causing the accumulation of holes to flow into the sc-SWCNTs channel, as shown in Figures 3(g) and (h). As a result, the threshold voltages of the Al gate electrode SWCNT TFTs are negatively shifted in contrast to the Ag gate electrode SWCNT TFTs.

To verify the effect of the IL-c-PVP dielectric layer on the oxidation effect of the Al electrodes, chemical element analysis was performed on the surfaces of the Al electrodes before and after being immersed in IL-c-PVP inks for 0.5, 2, and 4 h. The Al electrode was immersed in IL-c-PVP inks and then rinsed with PGMEA solution (the solvent of IL-c-PVP inks) to remove the residual chemical reagents on the electrode surface, and then the oxidation effect was observed by XPS. Figure 4(a) shows the elemental analysis of the Al electrode surfaces under different conditions. Figures 4(b)–(e) show XPS data of different Al gate electrode samples before and after immersion in IL-c-PVP inks for 0.5, 2, and 4 h. The peaks located at 75 and 72 eV represented AlOx and Al, respectively. The oxidation degree of Al gate electrodes can be judged by calculating the area ratio of these two peaks. It means that the ratio of the peak areas of AlOx to Al is larger along with the higher oxidation degree of Al gate electrodes. It can be seen from Figures 4(b)–(e) that the ratios of these two peak areas are 1.82, 2.06, 2.22, and 2.77 for Al gate electrodes before and after immersion in IL-c-PVP inks for 0.5, 2 and 4 h, respectively. It can be seen from Figure 4(f) that the ratios of these two peak areas for the samples immersed in IL-c-PVP inks are positively correlated with the immersion time, suggesting the denser alumina films with low work function are formed with the longer immersion time in IL-c-PVP inks. In a word, the more negative shift of the threshold voltage of the Al top-gate TFTs than that of Al bottom-gate TFTs is because of the formation of the low-work-function $Al_2O_3$ and the dipole reaction.

Furthermore, the SS and hole mobility were extracted from the transfer characteristic curves of top-gate and bottom-gate SWCNT TFTs with the Al gate electrodes according to the following equation:

$$\mathrm{SS} = \frac{\mathrm{d}V_{\rm gs}}{\mathrm{d}(\log I_{\rm ds})}. \tag{4}$$

It can be calculated from (1) and (4) that the SS and mobility of the TFTs are 61.4 mV $\cdot$ dec$^{-1}$ and 8.54 cm$^2$ $\cdot$ V$^{-1}$ $\cdot$ s$^{-1}$ for the top-gate SWCNT TFTs, and 87.9 mV $\cdot$ dec$^{-1}$ and 2.70 cm$^2$ $\cdot$ V$^{-1}$ $\cdot$ s$^{-1}$ for

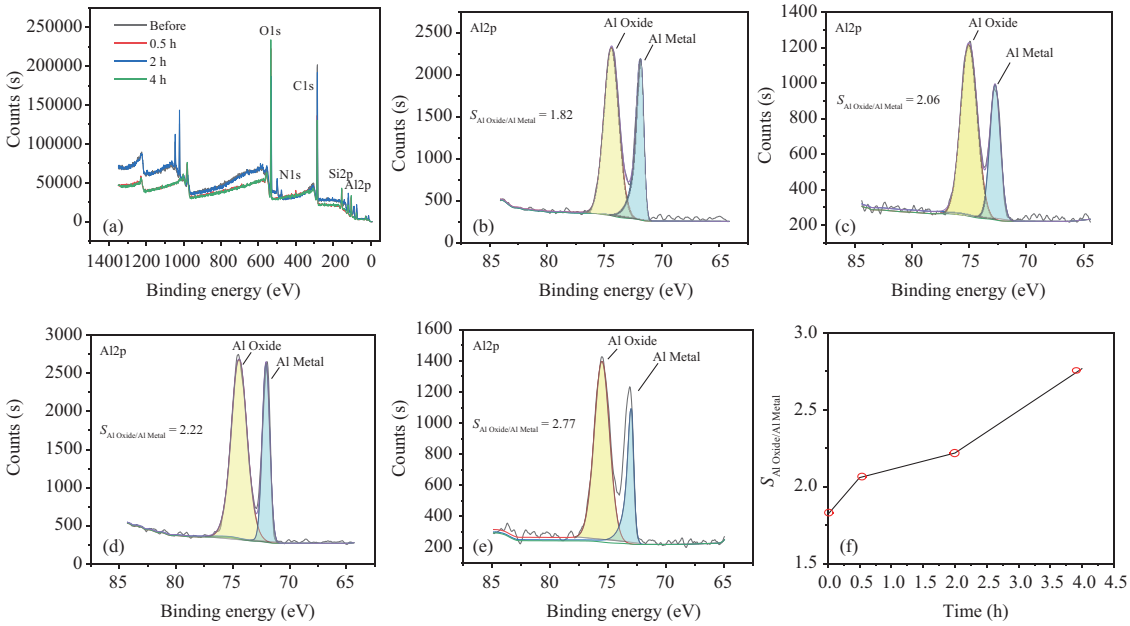


**Figure 4** (Color online) (a) Elemental analysis of the Al electrode surfaces under different conditions by XPS. (b)–(e) Al elemental analysis of Al electrodes before and after immersed IL-c-PVP ink for 0.5, 2, and 4 h. (f) The relationship between the immersion time and the area ratios.

the bottom-gate SWCNT TFTs, respectively. Figures S2(a) and (b) show the contact areas between sc-SWCNTs and the dielectric layers, and hole distributions in the two structures. It can be seen from Figures S2(a) and (b) that sc-SWCNTs are completely wrapped by the dielectrics in the top-gate devices, so the top-gate SWCNT TFTs have higher gate control efficiency, smaller SS, and higher mobility than bottom-gate SWCNT TFTs. To further demonstrate the advantages of our SWCNT TFTs, we compare the electrical properties among previously reported P-type SWCNT TFTs shown in Table S1. Our top-gate SWCNT transistor with Al gate electrodes not only has more negative threshold voltages but also has high on/off ratios ($\sim 10^6$) and smaller SS (Table S1), indicating that our top-gate and bottom-gate SWCNT TFTs have great advantages for constructing low power consumption carbon-based circuits.

### 3.2 Stability and mechanical flexibility of top-gate and bottom-gate SWCNT TFTs with 3D common-gate structure

The 3D CMOS inverters with the common-gate structure were constructed using our top-gate and bottom-gate SWCNT TFTs shown in Figure 5(a). Figure 5(a) shows the 3D CMOS inverter structure and the typical SEM image of sc-SWCNT thin films in the TFT channels. It can be seen from Figure 5(a) that sc-SWCNTs are distributed densely and relatively uniformly. Figures 5(b) and (c) show the transfer characteristic curves of top-gate and bottom-gate P-type SWCNT TFT devices before and after 3D integration, and keep in the air for 1 week. At the same time, since the bottom-gate TFT is vertically stacked on the top-gate TFT and shares a common gate electrode, there is a possibility that the performance of the TFT devices will be affected during the course of TFT fabrications. Therefore, we compared the electrical properties of top-gate and bottom-gate TFT devices before and after 3D integration. It can be seen from Figure 5(b) that there are no significant changes in on/off ratios and on currents along with the considerable shifts of the threshold voltage from $-0.5$ V in the standalone top-gate device to 0 V after 3D integration. The essential reason for the shift of the threshold voltage is that the bottom device suffered long-time high-temperature annealing during the preparation of top-gate TFT devices, and the threshold voltages of top-gate SWCNT TFTs shift right after annealing at high temperatures. After that, the top-gate device remains relatively stable after storage in the air for one week. The standalone bottom-gate and the bottom-gate SWCNT TFT devices in the 3D integration system have high stability shown in Figure 5(c). It is worth noting that both top and bottom SWCNT TFT devices in the 3D integrated system operate properly and still show enhancement-mode properties, with only the positive shift of the threshold voltage for the top-gate TFT devices, indicating the 3D common gate structure has high reliability.

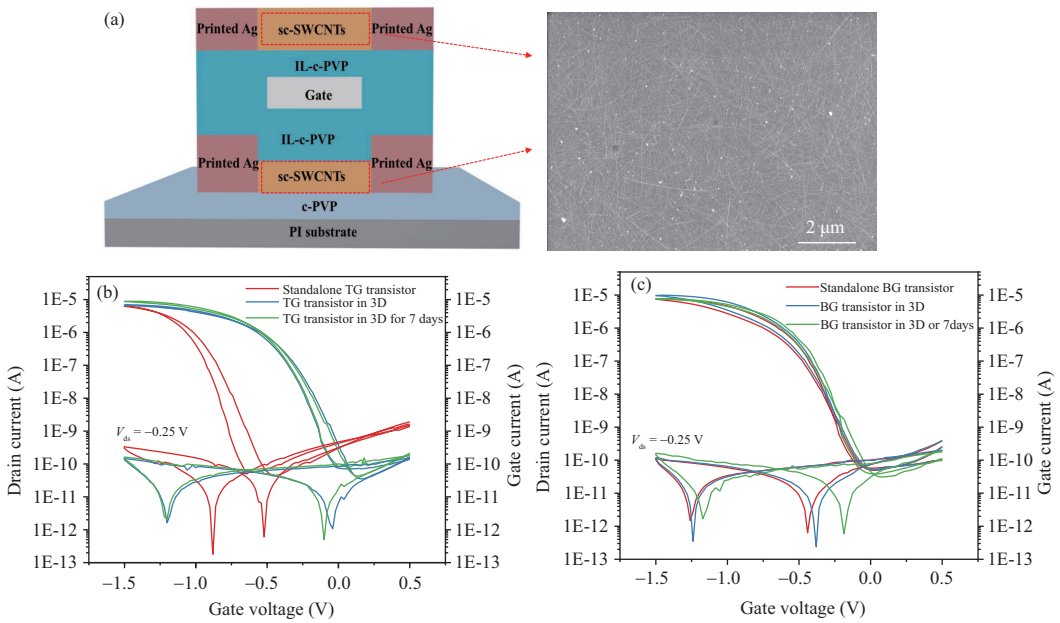


**Figure 5** (Color online) (a) Cross-sectional structure of a 3D integration system with the common-gate structure and the SEM image of sc-SWCNT thin films in the TFT channel. The transfer characteristic curves of (b) the top-gate and (c) the bottom-gate P-type SWCNT TFT devices.

The $I_{ds}$-$V_{gs}$ of the top-gate devices and the bottom-gate devices in the 3D integration system with the common-gate structure were measured (Figure 6). Figure 6(a) shows the transfer characteristic curves of the 16 top-gate devices at the bottom layer, and Figures 6(b) and (c) are the electrical parameters (the calculated SS and carrier mobility) extracted from the 16 devices in Figure 6(a). The transfer characteristic curves are essentially same with the on/off ratios of $10^6$, small hysteresis, and the threshold voltages near 0 V (enhancement mode) with no significant deviations. The SS and carrier mobility of the devices are shown in Figures 6(b) and (c), where the SS is concentrated between 80 and 90 mV $\cdot$ dec$^{-1}$ with only very few greater than 100 mV $\cdot$ dec$^{-1}$, and the carrier mobility is concentrated between 5 and 8 cm$^2 \cdot$ V$^{-1} \cdot$ s$^{-1}$ with only one exceeding 10 cm$^2 \cdot$ V$^{-1} \cdot$ s$^{-1}$, where the capacitance value of 4.7 μF $\cdot$ cm$^{-2}$ measured at a frequency of 0.1 Hz is used to calculate the device mobility. It is noted that the mobility is expected to be in the range of 70–110 cm$^2 \cdot$ V$^{-1} \cdot$ s$^{-1}$ when using the capacitance value (0.34 μF $\cdot$ cm$^{-2}$) at 1 Hz to calculate the transistors' mobility. Figure 6(d) shows the transfer characteristic curves of the 16 bottom-gate devices at the top layer. The SS and carrier mobility of the devices are shown in Figures 6(e) and (f), where the SS is concentrated between 70 and 90 mV $\cdot$ dec$^{-1}$ and the carrier mobility is concentrated between 5 and 11 cm$^2 \cdot$ V$^{-1} \cdot$ s$^{-1}$. The results demonstrate that our bottom-gate and top-gate TFT devices in 3D integrated systems are excellent homogeneous.

To verify the mechanical flexibility of the devices on a PI substrate, the top-gate and bottom-gate devices were bent 10000 times with a bending radius of 20 mm. The photo taken during the bending test is shown in Figure S3. After undergoing 10000 bending cycles, the transfer characteristic curves of both bottom-gate and top-gate devices exhibited negligible decreases in the open-state currents and a slight shift in threshold voltages shown in Figures 7(a) and (c). It can be seen from Figure S4 that the current switching ratios ($5 \times 10^5$), SS (85 and 90 mV $\cdot$ dec$^{-1}$), and mobility ($\sim$5 cm$^2 \cdot$ V$^{-1} \cdot$ s$^{-1}$) have no obvious changes, indicating their good mechanical flexibility. Figures 7(b) and (d) show the transfer characteristic curves of the top-gate and bottom-gate devices under a continuous bias voltage with $V_{gs}$ of −0.7 V and $V_{ds}$ of −0.25 V. The top-gate TFT device behaves almost exactly as it did initially (all curves overlapping almost exactly shown in Figure 7(b)), while the on-state currents of the bottom-gate TFT device show a slight drop after the bias test for 7200 s, demonstrating that the top-gate TFT device is more stable than the bottom-gate device due to the isolation from oxygen and water in air for top-gate TFT devices. In all, both top-gate and bottom-gate devices in the 3D integration system show enhancement mode with high on/off ratios, small hysteresis, small SS, and good mechanical flexibility and bias stability.

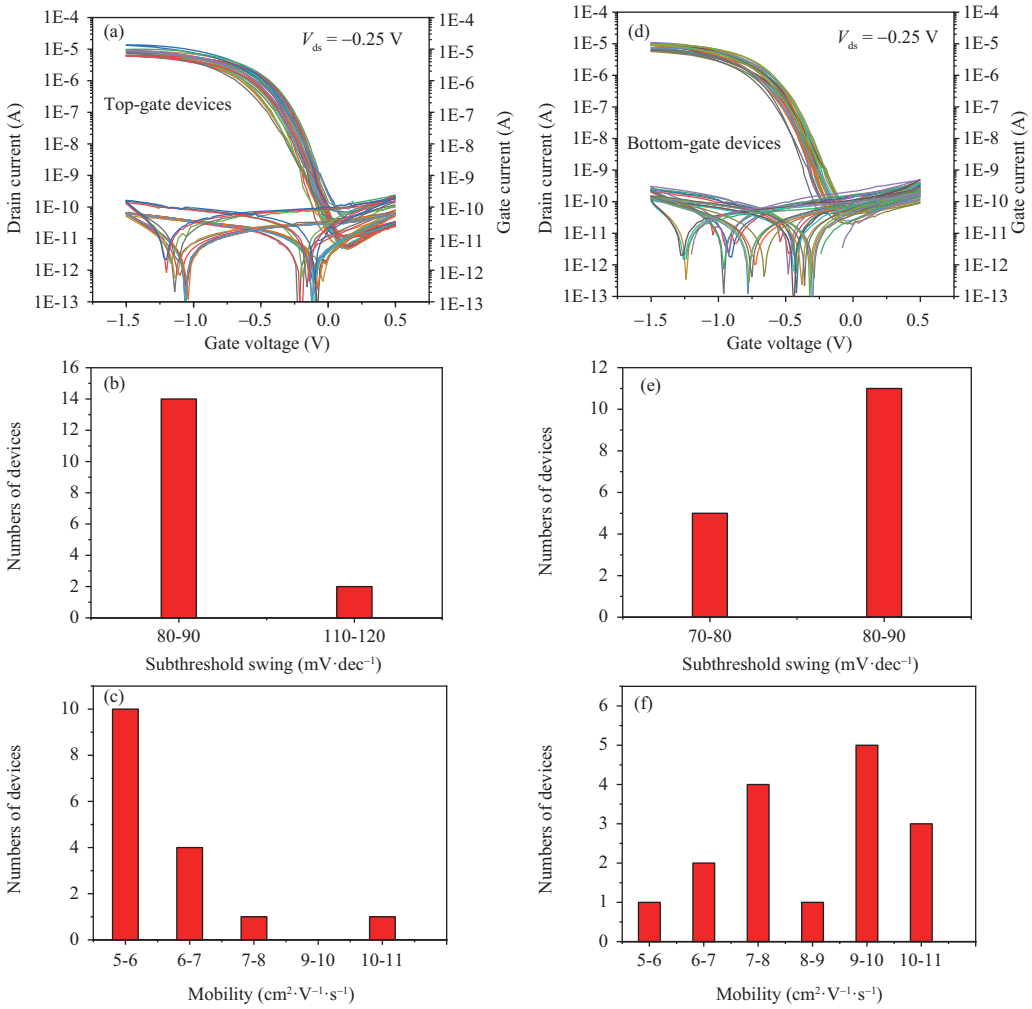


**Figure 6** (Color online) Electrical properties of top-gate and bottom-gate P-type TFT devices in the 3D integration system. (a)–(c) are the top-gate devices located in the bottom layer of the 3D integration system. (d)–(f) are the bottom-gate devices located in the upper layer of the 3D integration system. Transfer characteristic curves of (a) 16 top-gate and (d) 16 bottom-gate devices. (b) SS and (c) mobility for the top-gate devices. (e) SS and (f) mobility for the bottom-gate devices.

### 3.3 Flexible 3D integrated CMOS inverters

It is well known that the CMOS inverter is the heart of all digital designs. A clear understanding of inverter operation and properties greatly simplifies the design of complex structures such as logic gates, adders, multipliers, and microprocessors [46–48]. The electrical characteristics of these complex circuits can be inferred almost entirely from the results obtained by the inverter. Figure 8(a) shows a photo of the 4 × 4 3D common-gate CMOS inverter arrays on the PI substrate, the enlarged photo of a CMOS inverter, and a circuit diagram of a CMOS inverter. As shown in Figure 8(a), the inverter consists of an N-type transistor and a P-type transistor. As-prepared top-gate and bottom-gate SWCNT TFTs always show P-type characteristics when exposed to air and water. The cross-linking agent (F51) and epoxy resin (128) are mixed with sufficient stirring to obtain chemically modified epoxy amine ink, in which the epoxy resin provides encapsulation and the cross-linking agent containing a large number of amide groups is combined with the epoxy resin for electron injection. Therefore, the bottom-gate TFT devices at the top layer can be converted from P-type to N-type after depositing the epoxy amine ink [49]. Figure 8(b) shows the transfer characteristics of the bottom-gate SWCNT TFT from P-type to N-type ($V_{ds} = -0.25$ V for P-type and $V_{ds} = 0.25$ V for N-type) after the polarity conversion. It can be seen from Figure 8(b) that the change in open-state current is less than one order of magnitude after the transistor changes from P-type to N-type, and the output characteristics of P-type and N-type SWCNT TFT devices are shown in Figure S5, indicating that both P-type and N-type TFTs possess good ohmic contact characteristics. Figure 8(c) shows the voltage characteristic curves of the 3D CMOS inverter for different input voltage

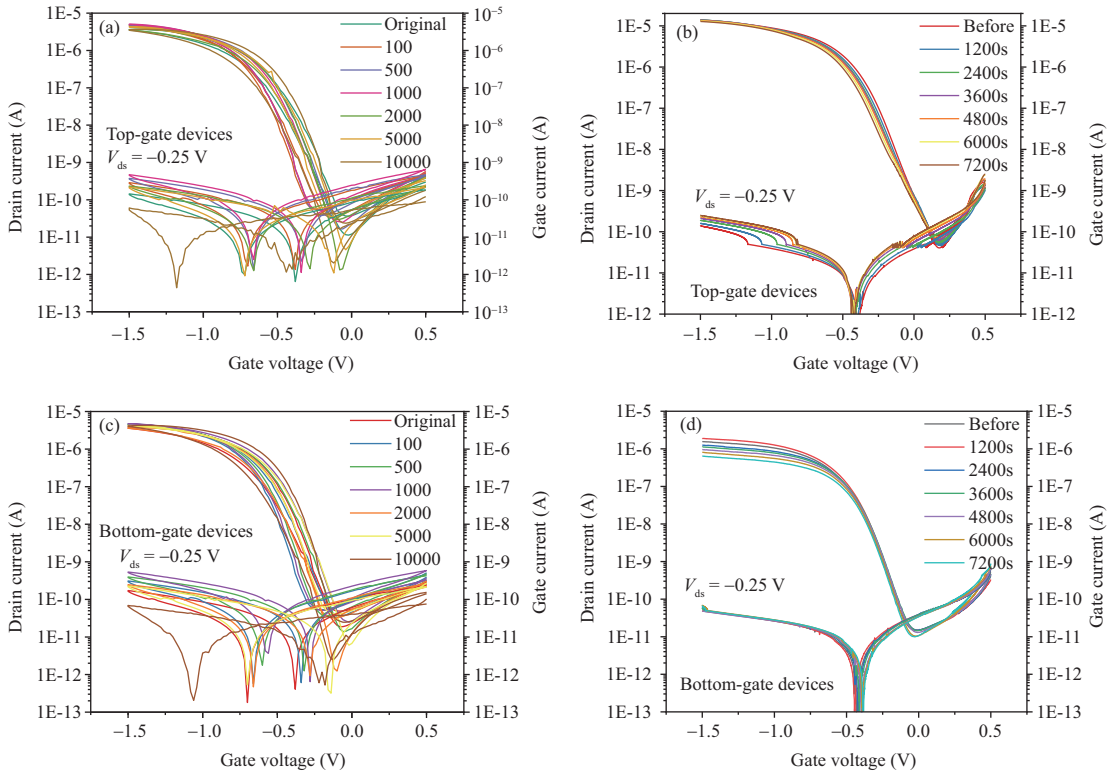


**Figure 7** (Color online) Mechanical flexibility and bias stability of top-gate and bottom-gate P-type TFT devices in the 3D integration system. Transfer characteristic curves of (a) the top-gate device and (c) the bottom-gate device before and after bending 10000 times with a radius of 20 mm, and of the bias stability of (b) top-gate and (d) bottom-gate devices (measured every 120 s under continuous bias at $V_{ds} = -0.25$ V and $V_{gs} = -0.6$ V).

ranges. The inverter can achieve rail-to-rail output when the input voltage is from −1 to 0 V. The input-output characteristic curve and noise tolerance of the 3D CMOS inverter at an input voltage of −1 V are shown in Figure 8(d), indicating a high noise tolerance of 80.04%. The voltage gains of the 3D CMOS inverter at different input voltages are shown in Figure 8(e). The voltage gains increase with increasing the $V_{DD}$ and can reach 34 at $V_{DD}$ of −1.5 V. Figure 8(f) shows the power consumption of the 3D CMOS inverter at different input voltages, and the peak power consumption of 14.1 nW when $V_{DD} = -0.5$ V. Compared to recently reported studies [9, 50], the power consumption of 3D CMOS inverter remains relatively high due to the dissipation-mode N-type TFT and the mismatch threshold voltages between the P-type and N-type transistors. The next work is to develop the enhancement-mode N-type SWCNT TFT devices with lower off currents and smaller SS, in order to achieve ultralow power consumption 3D CMOS inverters and circuits. To verify our 3D CMOS technology can integrate the higher-level circuits, flexible SWCNT NAND and NOR gates have been constructed, and the output characteristics are shown in Figure S6. It can be seen from Figure S6 that both of them can work well. As the density and integration of the SWCNT TFT devices are not high enough, we find that through-holes have no negative effect on the performance of the SWCNT TFT devices.

## 4 Conclusion

In this work, a valid method to modulate the threshold voltages of SWCNT TFTs from 0.6 to −0.6 V has been developed by using the low work function Al as the gate electrodes and high capacitance IL-c-PVP as dielectric. Meanwhile, the SWCNT TFTs have good electrical characteristics with a high $I_{on}/I_{off}$ (5–6 orders), small low SS (61.4 mV · dec$^{-1}$), and a small hysteresis and good mechanical flexibility characteristics and bias stability. Furthermore, 3D CMOS inverters are capable of rail-to-rail outputs at low operating voltages with a voltage gain of 34 at $V_{DD}$ of −1.5 V, a noise tolerance of 80.04% at $V_{DD}$ of −1 V, and a peak power consumption of 14.1 nW at $V_{DD}$ of −0.5 V. To conclude, this work has great significance for the future development of complex carbon-based digital circuits. In our future work, we

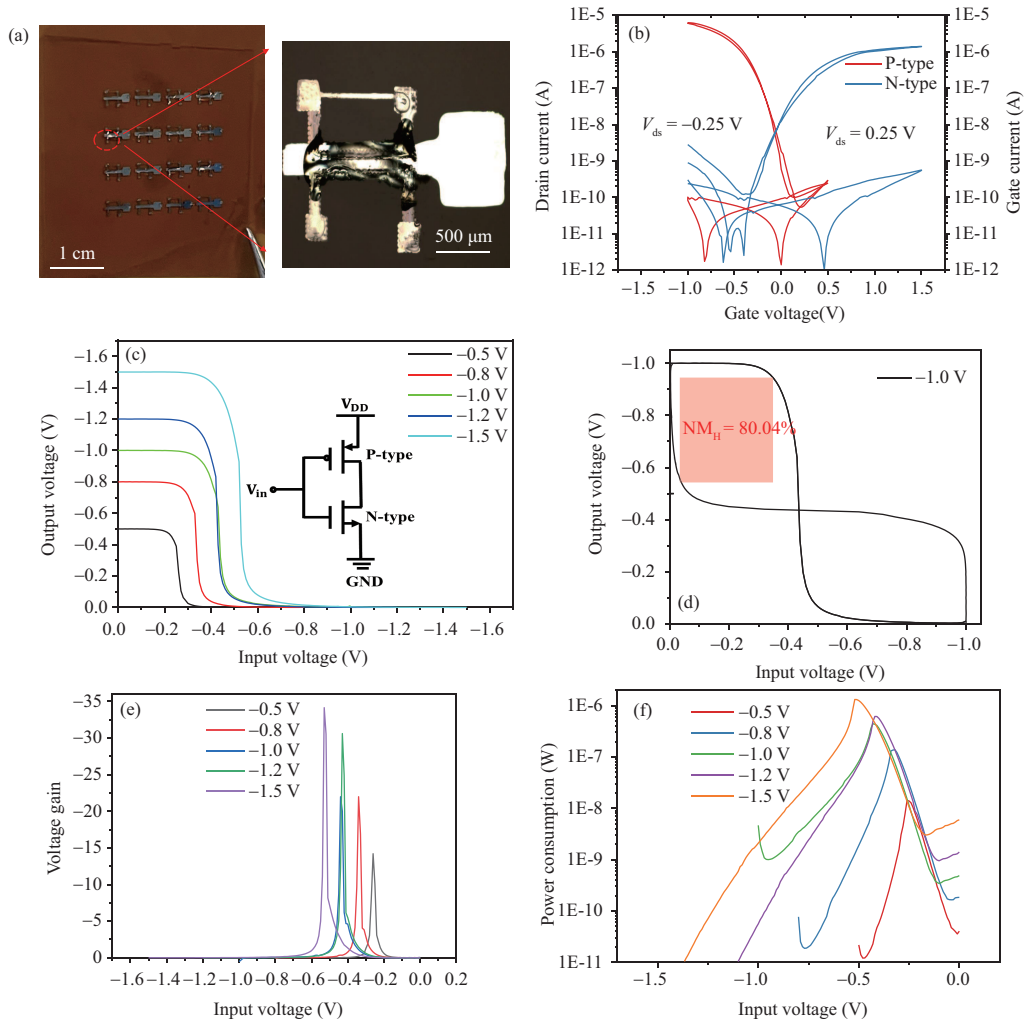


**Figure 8** (Color online) (a) Optical photograph of the 3D common-gate CMOS inverters and circuit diagram of the CMOS inverter. (b) Transfer characteristic curves of P-type and N-type SWCNT TFT devices. (c) Voltage transfer curves of the 3D CMOS inverter when $V_{in}$ = −0.5, −0.8, −1, −1.2, and −1.5 V, respectively. (d) Noise tolerance of a 3D CMOS inverter at $V_{in}$ = −1 V. (e) The voltage gains of the 3D CMOS inverter when $V_{in}$ = −0.5, −0.8, −1, −1.2, and −1.5 V, respectively. (f) Static power consumption of 3D CMOS inverters at $V_{in}$ = −0.5, −0.8, −1, −1.2, and −1.5 V, respectively.

will focus on improving the device mobility by using aligned carbon nanotube films as channel materials, and reducing device size (ballistic transport), the density of interface states, and so on [51, 52].

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**Supporting information** Figures S1–S6 and Table S1. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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