SCIENCE CHINA
Information Sciences

• REVIEW •

October 2021, Vol. 64 201402:1–201402:16
https://doi.org/10.1007/s11432-021-3271-8

Carbon nanotube-based CMOS transistors and integrated circuits

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Received 31 March 2021/Revised 11 May 2021/Accepted 24 May 2021/Published online 20 August 2021

Abstract Over the last sixty years, the scaling of silicon-based complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) have promoted the rapid development of microelectronic technology. However, the development of Si CMOS technology is currently subject to serious challenges from various aspects such as physics limit, cost, and power consumption, and is becoming increasingly difficult. Material innovation is exerting an ever-greater role in the integrated circuit design. By looking for thinner semiconductor materials with higher mobility as the active layer to construct smaller and higher-performance transistors, it is possible to further stimulate transistors and integrated circuits on performance, density, power dissipation, and functions. In 1991, Iijima discovered carbon nanotubes (CNTs). Due to its excellent electrical properties and intrinsic nano-scale size, CNT has been considered by academia and industry to have great potential to replace silicon materials in the future for the extremely scaled technology nodes or novel electronic applications. This paper reviews the latest advancements in CNT-based electronics research. Finally, the challenges and pathways for nanotube transistors to transition into commercial applications are discussed.

Keywords carbon nanotube, transistor, integrated circuit, scaling, nanoelectronics

Citation Xie Y N, Zhang Z Y. Carbon nanotube-based CMOS transistors and integrated circuits. Sci China Inf Sci, 2021, 64(10): 201402, https://doi.org/10.1007/s11432-021-3271-8

1 Introduction of carbon nanotube-based CMOS integrated circuits

Since Kilby invented the first integrated circuit (IC) in 1958, the continuous scaling of silicon-based complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) has promoted the rapid development of microelectronic technology and at the same time, mankind has entered the information society [1]. All kinds of high technologies in modern society, such as smartphones, supercomputers, intelligent drivers, and high-performance central processing units (CPUs) are supported by chips [2].

However, the development of silicon-based CMOS technology is now subject to serious challenges from various aspects such as physical limit, cost, and especially power consumption [3, 4]. It is becoming more and more difficult for devices to shrink and is necessary to find new technical approaches. Material innovation is exerting an ever-greater role in the IC advancing [5–8][1)].

Sun [9], the former chief technology officer (CTO) of TSMC, has pointed that the core problem of IC development is how to continuously obtain high-performance and low-power transistors (Figure 1). The conventional scaling down behavior confronts the limit of performance improvement, and becomes no longer valid. Additionally, the specific manifestation of low power consumption is that the transistor has a steep subthreshold slope (SS), indicating that the FET can be turned between on and off states within a narrower range of voltages, which plays a key role in lowering the power consumption of ICs. Since silicon materials are facing various restrictions, naturally, the industry has turned its attention to material innovation as a direct "life-saving" method of Moore's Law. By looking for thinner

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1) International Technology Roadmap for Semiconductors (2013 edition).

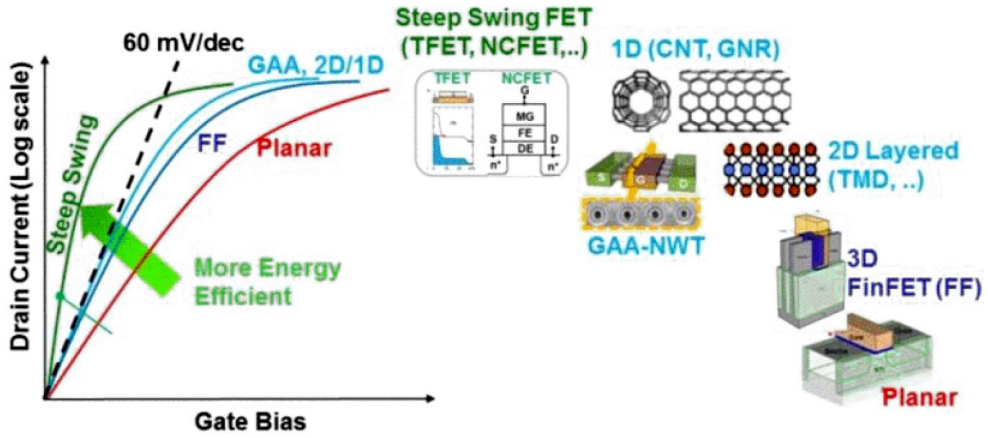

Figure 1 (Color online) Transistor scaling trend and innovation opportunities [9] @Copyright 2017 IEEE.

semiconductor materials with higher mobility as the active layer to construct smaller transistors with higher-performance enabling further scaling of transistors. In the beginning, numerous nanomaterials entered the candidate list of alternatives to silicon materials, including graphene, carbon nanotube (CNT), various transition metal dichalcogenides (TMD) represented by molybdenum disulfide, and black phosphorus [10]. Compared with other candidates, CNT has the following unique advantages for electronics applications [11–22]. At first, CNT has an intrinsically ultra-thin body (with a diameter of 1–2 nm) [23], which gives excellent electrostatics in FETs and can thus effectively avoid the short channel effect (SCE) in ultra-scaled FETs. Second, CNT exhibits high room-temperature carrier mobility ($\sim$100000 cm^2/Vs) for both electrons and holes [24–28]. Mobility represents the drift speed of carriers in the electric field, and corresponds to the potential of key performance parameters of transistors. Materials with higher intrinsic mobility have higher device transconductance, faster speed, and are easier to achieve higher on-state current. As a result, when carbon nanotube materials are used to replace silicon as a transistor channel, good performance can still be achieved at scaled technology nodes even using planar device structure [29–32].

In 1998, Dekker et al. [33] from Delft University in the Netherlands and Martel et al. [34] from IBM each prepared the first CNTFET. The device structures are extremely simple: a semiconductor-type carbon nanotube is lapped between two Pt or Au electrodes. A silicon substrate is used as the bottom gate electrode. Pt or Au are metals with high chemical stability. However, a large Schottky barrier will form at the contact between carbon nanotubes and these metals. Thus, the output current was extremely small, and its performance was far from the traditional silicon-based devices at the technology node in the same period, not presenting the electrical advantages of carbon nanotube materials at all.

In 2007, the team of Peng and Zhang in Peking University [35] developed a simple technique for fabricating CNT-based CMOS devices, where high-work-function metal Pd was used as the source/drain contacts to form high-performance P-type CNTFETs; and low-work-function metal Sc or Y was used as the source/drain contacts to form high-efficiency N-type CNTFETs. The entire process does not need the source and drain heavily doped like silicon-based technology. Thus, the carbon nanotube-based CMOS process was called a "doping-free" process. The electrical measurement results display that the main parameters of the as-fabricated P-type CNTFET and the N-type CNTFET are highly symmetrical with the mobility of the electrons and the holes are simultaneously greater than 3000 cm^2/Vs [36].

After years of development until 2017, the Peking University scientific research group [37] published an article on Science, which demonstrated for the first time that the CNT-based CMOS transistors with a channel length less than 5 nm can still maintain good gate control (Figure 2 [37–39]). Considering the key parameter of a transistor, the energy-delay product (EDP), it has a one-order-of-magnitude advantage over similar-sized devices that are based on silicon. This experimental result strongly confirms that carbon nanotube-based transistors perform better than silicon-based transistors, making up for the lack of research on CNTFETs. The important reported FETs based on individual CNTs are listed in Table 1 [33–37, 40], which clearly shows the development of CNTFETs in the past two decades. Additionally, the results of simulation analysis also show that at extremely scaled technology nodes, CNTFETs adopting a three-dimensional structure (CNT FinFET) with optimal threshold voltages are capable of imparting an about 50-fold EDP advantage over the Si FinFETs at a low supply voltage ($V_{\rm dd}$)

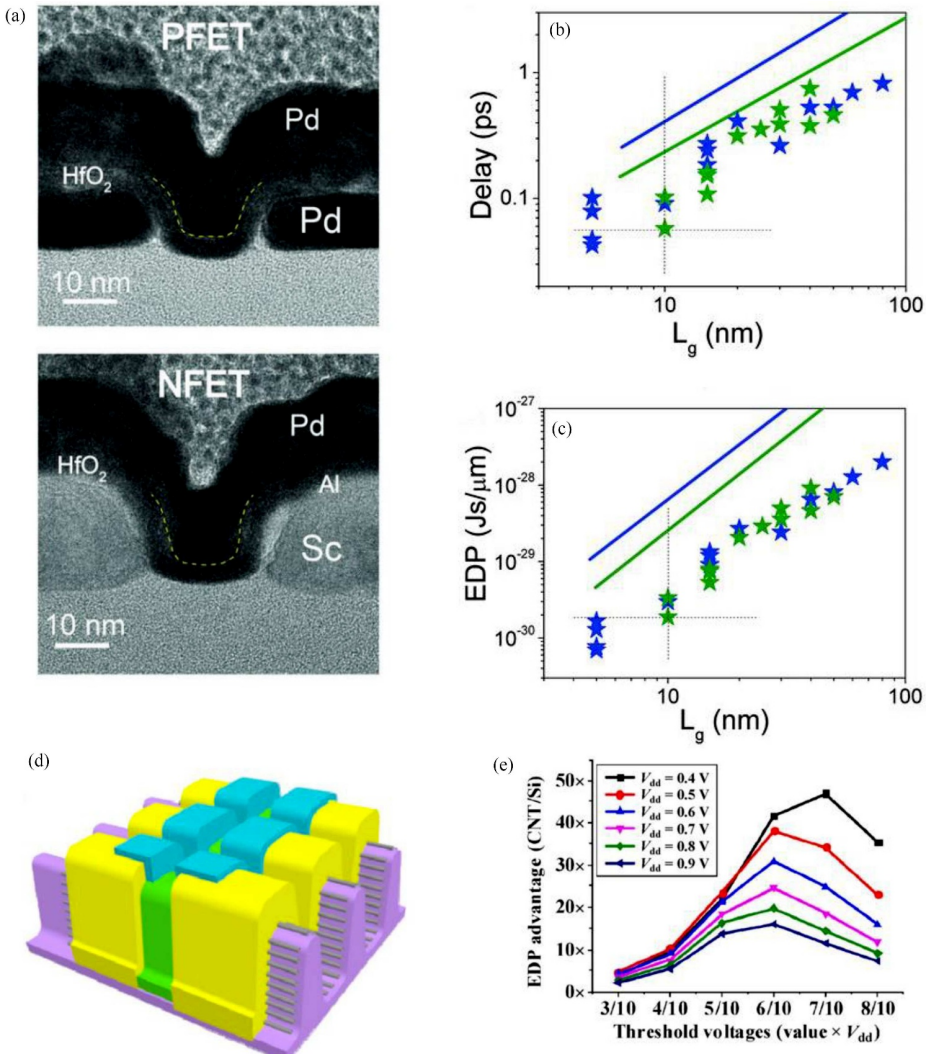

Figure 2 (Color online) (a) Cross-sectional TEM micrographs of P- and N-type FETs, where the channel and gate lengths are respectively 20 and 10 nm @Copyright 2017 AAAS. (b) and (c) Comparisons of gate delay and EDP scaling patterns between CNT- and Si-CMOS FETs. The blue solid line indicates the experiment data fitting for the P-type Si-MOSFETs [39], whereas the green solid line indicates the N-type Si-MOSFETs. Data assessments are all performed at a $V_{\rm dd}$ of 0.4 V for the CNT CMOS FETs. Besides, the blue and green stars respectively represent the P- and N-type CNTFETs [37] @Copyright 2017 AAAS. (d) Structural illustration of the CNT FinFET device @Copyright 2016 Springer Nature. (e) Graphs depicting the drastic effects of small persistent $V_{\rm th}$ changes on the EDP advantages of CNT FinFET versus Si FinFET at varying supply voltages, where $V_{\rm dd}$ = 0.9 V [38] @Copyright 2016 Springer Nature.

Table 1 Comparison of various FETs based on individual CNTs

Ref.	Polarity	Contact type	Gate structure	$I_{\rm on}$	SS (mV/dec)	d (CNT) (nm)	L_g	μ (cm^2/V·s)
[33]	P	Schottky contact	Bottom gate	∼nA	–	1.4	400 nm	–
[34]	P	Schottky contact	Bottom gate	∼nA	–	1.6	1 μm	20
[35]	N	Ohmic contact	Top gate	20 μA ($V_{\rm gs}$ = −2 V)	250	2	300 nm	–
[36]	P, N	Ohmic contact	Top gate	11.5/11 μA (P/N) ($V_{\rm gs}$ = −2 V)	90/100 (P/N)	2	3 μm	3300/3000
[37]	P, N	Ohmic contact	Top gate	15 μA ($V_{\rm gs}$ = −0.4 V)	60/70 (P/N)	1.3	10 nm	–
[40]	P	Ohmic contact	Local bottom gate	10 μA ($V_{\rm gs}$ = −0.5 V)	85	1–1.2	20 nm	–

of 0.4 V, suggesting great potential of the integrated circuits based on CNTFETs (Figure 2) [38].

Not only has an enormous performance advantage, but carbon nanotubes can also form new electronic

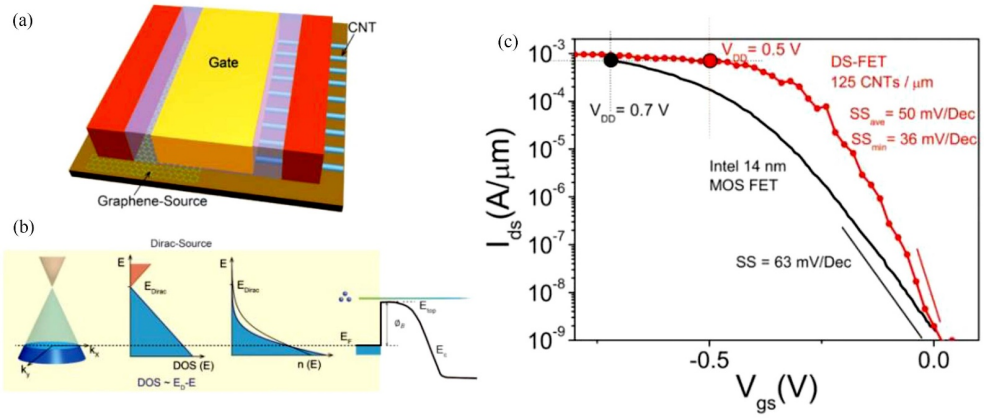

Figure 3 (Color online) (a) Structural illustration of a DS-FET with CNT array channel [41]. (b) Trends of a superexponentially-decaying Dirac source (DS) regarding schematic band structure, DOS, the density of electrons, as well as thermionic emission over a potential barrier in conducting channel. Accordingly, a narrower electron density localization is noted around the Fermi level. Besides, $n(E)$ represents the electron density, and the solid line in $n(E)$ indicates a Boltzmann distribution, where the exponential decay points towards higher energy [41]. (c) Graphs comparing a 400-nm DS-FET (red, 125 CNTs/mm) powered by a 0.5-V low bias with a 14-nm Intel Si MOSFET (black) powered at 0.7 V [39, 41] @Copyright 2018 AAAS.

device structures beyond traditional MOSFETs. The Peking University research team further discovered that if the electrode material of CNTFET is replaced by graphene, the high-efficiency graphene band tunneling can be applied to form a "cold" electron source, which is the so-called "Dirac-source" (Figure 3) [41]. Compared with the general metal electrode, the electron density distribution near the Fermi level in the Dirac-source is narrower, and thus a smaller SS can be obtained, indicating that this Dirac-source field-effect transistor is composed of carbon-based materials and thus can break through the Boltzmann limit of the sub-threshold swing of traditional field-effect transistors. SS can not only be less than 60 mV/dec, but can even be below 40 mV/dec in room temperature condition. The most direct benefit of super-low SS value is the reduction in operating voltage. Based on data released by Intel, the operating voltage of silicon-based technology at the 14 nm technology node is 0.7 V [39]. While maintaining the same on-state performance and off-state performance as the silicon-based FET, the operating voltage of the Dirac-source FET is only 0.5 V, suggesting that its power consumption is only one-third of the silicon-based FET, a promising feature for the integrated circuit development in the future.

The performance and power consumption advantages of CNTFETs will be further amplified in the case of large-scale integration. Simulation results show that even using CNTFETs with unoptimized performances (on-state current $I_{\rm on}$ is 0.75 mA/μm, off-state current $I_{\rm off}$ is 2.1 μA/μm) to form a CPU, there is still a huge improvement in energy efficiency in comparison with silicon technology. The performance improvement of each generation of technology nodes of CNTFETs is much greater than that of Si FETs [40]. It is worth emphasizing that the carbon nanotube-based technology is a low-temperature process, which is very suitable for the new circuit architecture of monolithic three-dimensional integrated circuits. The N3XT system proposed by the group from Stanford University in the United States, based on CNTFETs, combined with the latest storage technologies, such as RRAM, STTRAM, stacks multiple circuit layers in the vertical direction, significantly increasing the integration per unit area [42]. In the meanwhile, high-density inter-layer interconnects are adopted to realize signal transmission between different layers, breaking through the computing power bottleneck of the "storage wall" existing in the planar circuit architecture. Through theoretical calculation and simulation analysis, it is shown that from silicon-based planar circuits to CNT 3D ICs, the computational efficiency can increase by approximately 1000 times (Figure 4(a)). On overlapping vertical layers, a laboratory prototype of such computational system has been fabricated, which encompasses Si FET and CNTFET computing units, RRAM arrays, memory access circuitry, and over one million CNTFET gas sensors for inputs, with an emphasis on how novel nanotechnologies can be applied for significant and considerable advancement in the computing realm (Figure 4(b)) [43].

In addition to traditional circuit applications, some special application scenarios such as outer space and nuclear reactors also require transistors that are aimed specifically at various development objectives [44]. This is because, in these applications, radiation can result in transistor failure due to the damage of the semiconductor channel, gate oxide, and peripheral insulators, such as isolation or substrate oxidation [45].

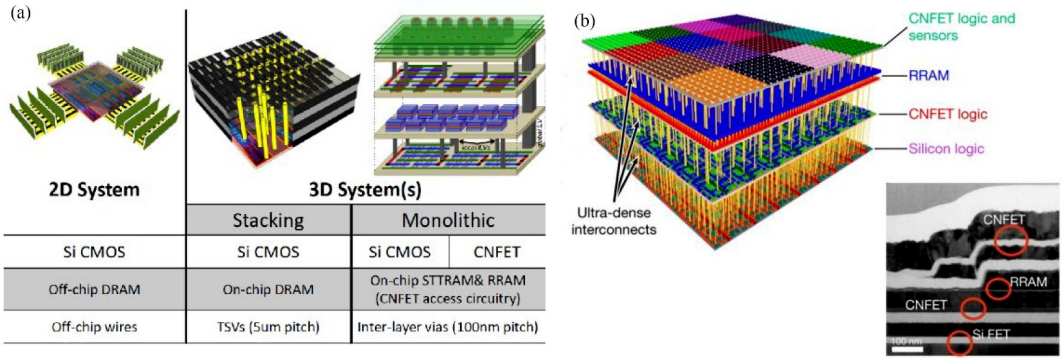

Figure 4 (Color online) (a) Comparison between different circuit architectures [42]. (b) Schematic illustration of a monolithic 3D-integrated chip with nanotube sensors and logic circuits fabricated on top of a silicon chip with high-density interconnects for high bandwidth interlayer communications. In the bottom right part, a cross-sectional TEM micrograph of the four-layer chip is displayed, where each layer is stressed (scale bars = 100 nm). Darker areas of the TEM micrograph represent various oxides like inter-layer or gate dielectrics, whereas brighter areas are wire cross-sections [43] @Copyright 2017 Spring Nature.

Fabrication of a radiation-hardened FET via component redesign has been reported, which is invulnerable to total ionization irradiation (TID) [46]. The transistor comprised semiconducting CNTs (channel material), as well as an ion gel gate and a thin polyimide substrate (Figure 5). The carbon-carbon bond in carbon nanotubes is extremely strong, coupled with its small scattering cross-section, and therefore, the use of CNTs as the channel material can avoid the impact of high-energy radiation particles on the device channel. The ion gel serves as the gate of CNTFET, which is conductive owing to the movable ions. Meanwhile, the electrical double layers (EDLs) formed on the CNT surfaces offer an ultrahigh gate efficiency by serving as the gate dielectric. Since the heavy ions with short diffusion lengths in the ion gel, which are attributed to a radiation source, do not permeate easily through the EDLs, a drastic decrease in the ion-inducted interface trap density is noted at the layer below EDLs (Figure 5). The thin polyimide substrate can be penetrated by highly energized radiation particles without inducing current leakage paths or charge traps. At a 66.7 rad $\cdot$ s^{-1} dose rate, the FETs show a radiation tolerance reaching 15 Mrad, a value prominently higher than the silicon-based devices' 1 Mrad [47]. Furthermore, the radiation-damaged FETs can be restored by 10 min of annealing at a 100°C moderate temperature.

2 Possible application areas of carbon nanotube-based CMOS integrated circuits

The future development of digital integrated circuits puts forward the following requirements for transistors, as shown in Figure 6. To maximize the use of existing resources, CMOS technology is still the first choice. Transistors require both low power consumption and high performance. In addition, the process of fabrication should be simple enough to minimize the cost and improve the yield.

As mentioned above, carbon nanotubes have super high carrier mobility ($>$ 100000 cm^2/Vs) and saturation velocity as well as symmetrical band structure. In addition, carbon nanotube-based doping-free CMOS technology is capable of obtaining high-performance P-type devices and N-type devices at the same time without complex manufacturing procedures. Additionally, experiments have also confirmed that this process allows the fabrication of devices with channel lengths below 5 nm. Especially, carbon nanotube-based circuits have lower supply voltage which is conducive to reducing dynamic power consumption [48]. Briefly, carbon nanotubes are suitable to construct high energy-efficiency digital ICs [49–51].

On the scale of digital integrated circuits, the medium-scale PMOS and CMOS integrated circuits have been reported recently, where stochastically oriented CNT films are used. Figure 7 displays three examples, namely a 2-to-1 multiplexer, a D-latch, and a T flip-flop circuit, which show outstanding rail-to-rail outputs [52, 53]. For integrated circuits, speed characterization is accomplished with a ring oscillator circuit (Figure 8). This is also the standard experimentation for the evaluation of new material-based electronics and their compatibility assessment with conventional circuit structures. The CNT film-based integrated circuits were shown capable of working at an oscillation frequency of 5.54 GHz after scaling down of channel length to the deep sub-micrometer range, such as 115 nm [54]. This implies an 18 ns gate delay, which approximates that of 0.18-μm silicon CMOS process with a 130 nm gate length [55].

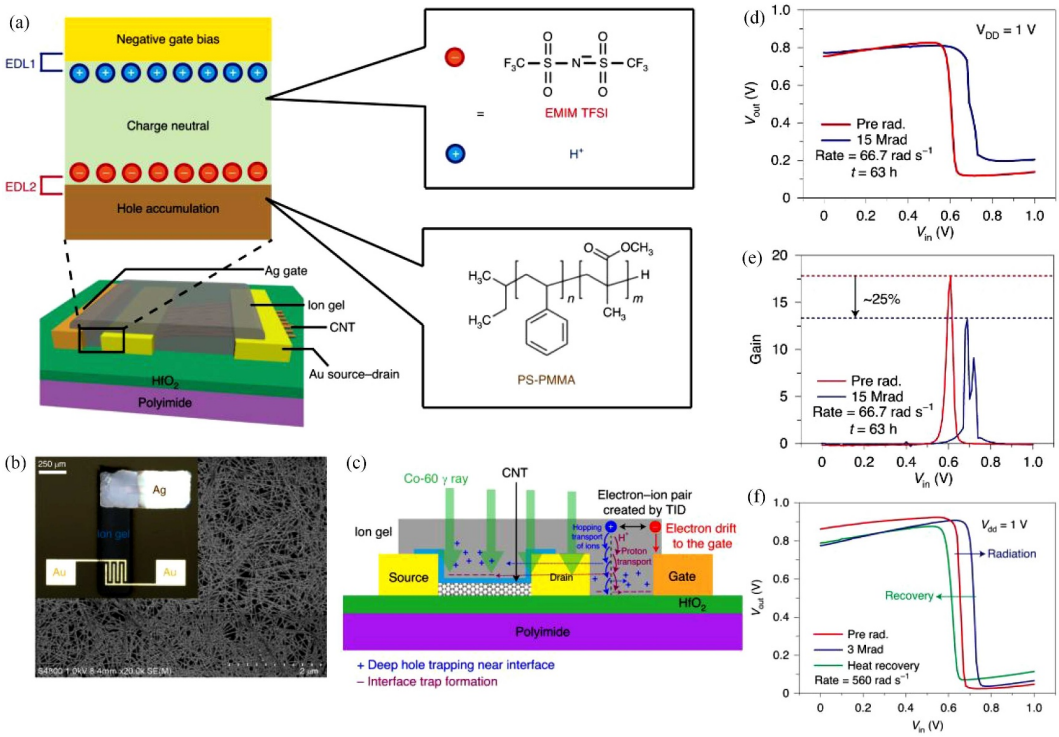

Figure 5 (Color online) (a) Schematic of a radiation-immune ion gel-gated CNTFET, whose substrate is polyimide. (b) SEM micrograph of solution-processed CNT film on a polyimide substrate. Inset is an optical image of a finger-structure CNTFET, whose dielectric layer is a printed ion gel. (c) Irradiation schematic of radiation-immune CNTFET with Co-60 γ ray. (d) VTC plots of a CMOS-like inverter ($V_{\rm dd}$= 1 V) before and after low-dose-rate irradiation. (e) Voltage gain plots of an inverter ($V_{\rm dd}$= 1 V) against $V_{\rm in}$ before and after low-dose-rate irradiation. (f) Heating-triggered recovery of VTC performance for the CMOS-like inverter [46] @Copyright 2020 Springer Nature

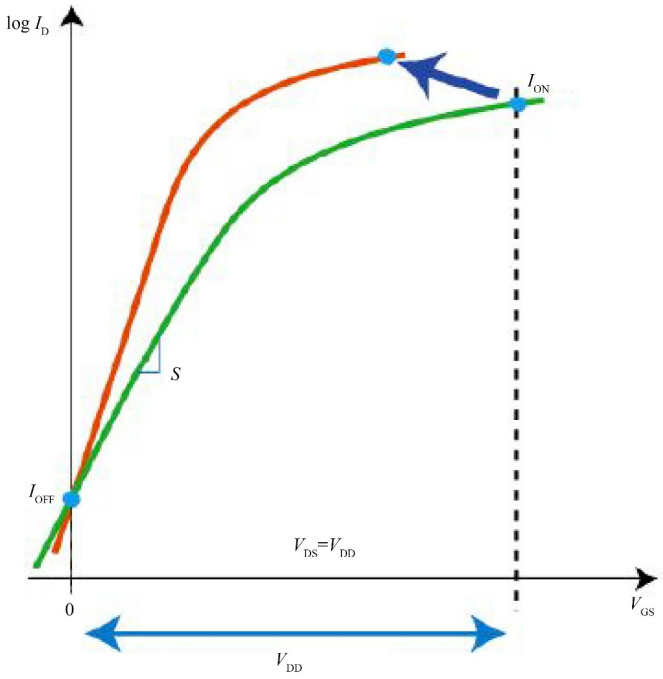

Figure 6 (Color online) Requirements for transistors in the development of digital integrated circuits.

In 2013, the demonstration of an intact digital system was introduced benefited from the progress in CNT technology. Being a microcomputer consisting of 178 CNTFETs, the system only executed a single instruction, which was operating solely on a single data bit [56]. After years of efforts, the same team at the

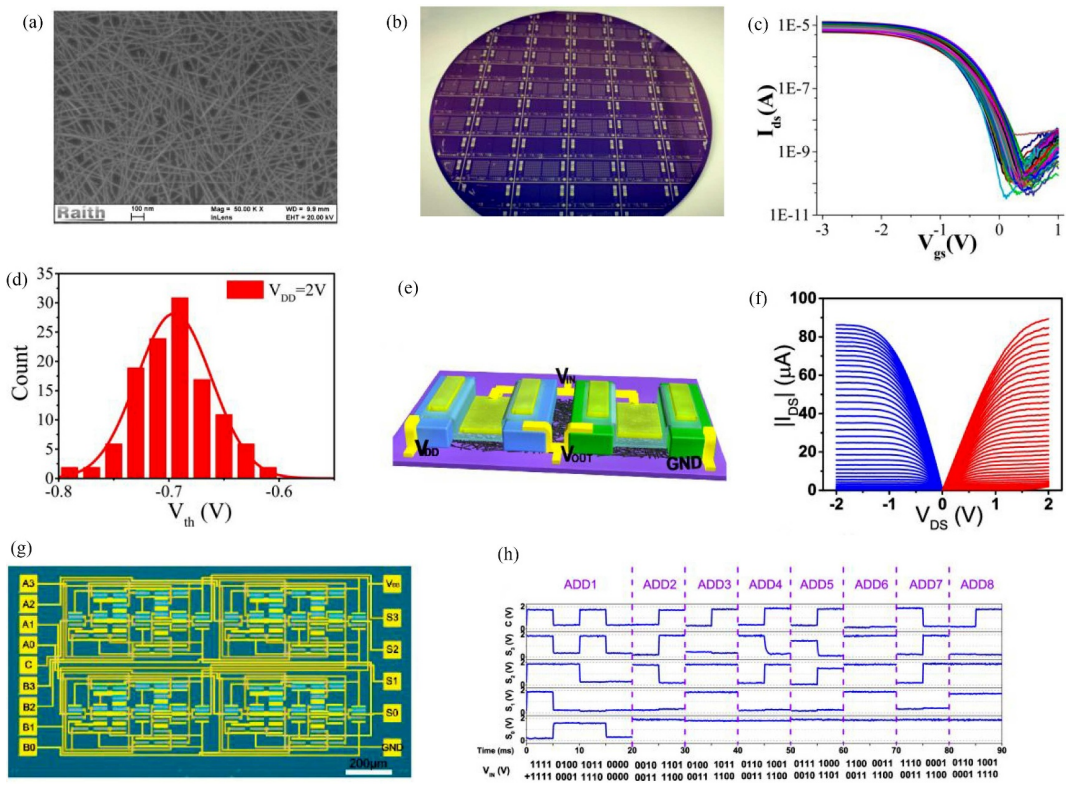

Figure 7 (Color online) (a) SEM image of deposited CNT network on Si/SiO_2 substrate. (b) Batch production of CNTFETs on a 4-inch wafer. (c) Transfer characteristics of 120 typical top-gate FET, the voltage bias $V_{DS} = -1$ V. (d) Statistic distribution histograms of V_{th}, where the average value is -0.7 V and the standard deviation $\sigma = 34$ mV from these 120 CNTFETs [52]. (e) Structural illustration of CMOS FET based on CNT network films. (f) Output patterns of the P-type FET (blue lines) and the N-type FET (red lines) over a $|V_{GS}|$ range from 0 (bottom) to 2 V (top) with a 0.05-V step size. (g) Micrograph depicting a 4-bit adder [53]. (h) Functionality measurements of eight 4-bit adders at a 2-V V_{DD} @ Copyright 2016, 2017 American Chemical Society.

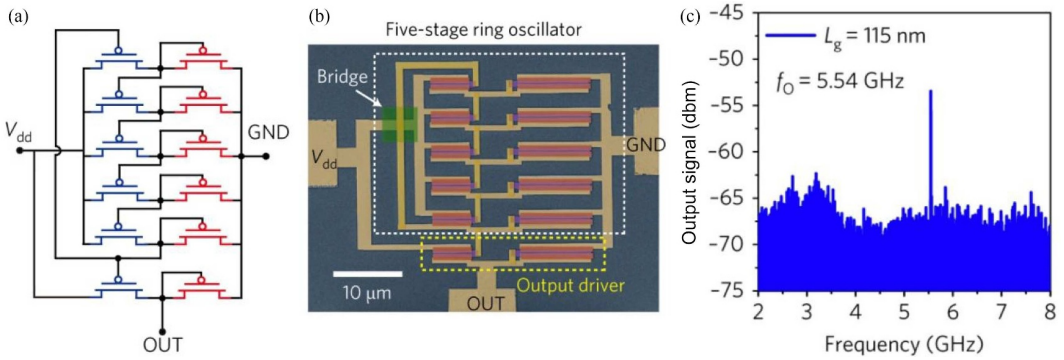

Figure 8 (Color online) Circuit schematic (a) and SEM micrograph (b) of a five-stage CNT RO based on stochastically-oriented top gate CNTFET (scale bars = 10 μm). In these images, V_{dd} denotes the supply voltage and GND represents the ground. The loading transistors (red) on the left have 2-folds greater W_{ch} than the driving transistors (blue) on the left. (c) The output spectrum of a representative five-stage RO with a 115-nm L_g, where the oscillation frequency is 5.54 GHz [54] @Copyright 2020 Springer Nature.

American Massachusetts Institute of Technology (MIT) eliminated the influence of undesirable carbon nanotube materials by further exploiting the circuit design and processing technologies and employed industry-standard tools and techniques to successfully show a 16-bit microprocessor called RV16X-NANO with 14000 CNTFETs, which can perform the same tasks as commercial microprocessors (Figure 9) [57].

Except in the field of digital circuits, the radio frequency (RF) properties of CNTFETs are promising because of their high saturated velocity, high carrier mobility, as well as the small intrinsic capacitance of CNTs, which is particularly conducive to attaining a higher f_T/f_{max} cut-off frequency ratio than the RF transistors that are based on such traditional bulk semiconductors as Si and III-V compound semicon-

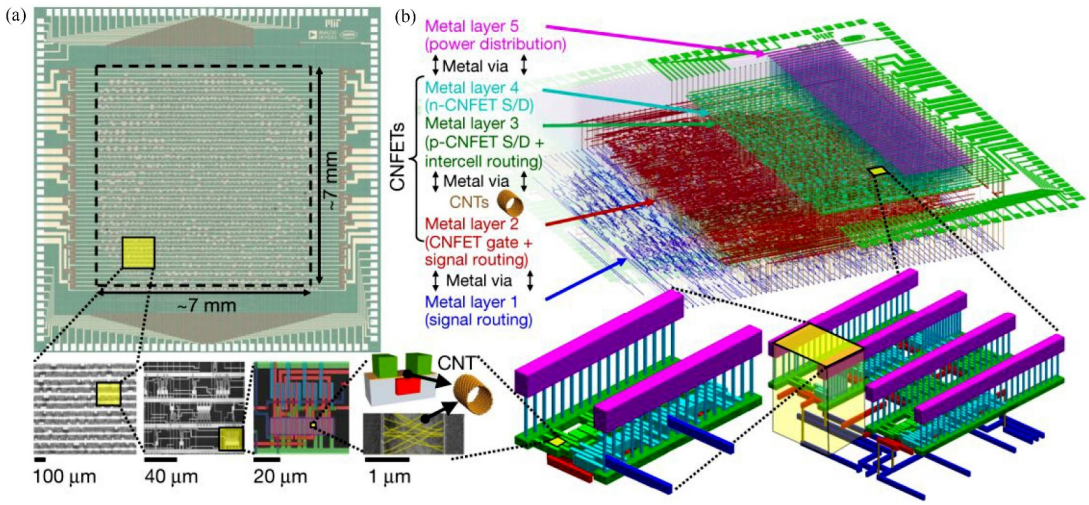

Figure 9 (Color online) (a) Illustration describing an RV16X-NANO chip, where the die size is 6.912 mm × 6.912 mm, with I/O pads arranged in the surroundings. SEM micrographs with rising magnification are displayed below. Wafer-scalable fabrication of RV16X-NANO is achieved fully from the CNFET CMOS in a Si-CMOS- and VLSI-compatible manner. (b) 3D scaled schematic depicting the physical layout of RV16X-NANO, which leverages a novel 3D architecture. The CNFETs in the 3D architecture is arranged in the stack center, where the metal routing is utilized both above and below the device layer [57] @Copyright 2019 Spring Nature.

ductors [58]. CNTFETs can be fabricated on completely insulated substrates such as diamond, quartz, glass, which can avoid the influence of substrate parasitic and further increase the speed. Additionally, inheriting the unique transport behaviors and state density of quasi-1D CNTs, the CNT RF transistors exhibit outstanding intrinsic linearity, which is exceptionally desirable in analog RF transistors [59]. For the CNTFETs based on solution-processed CNT films with scaled gate lengths and high semiconducting purity, they possess excellent DC properties. A peak g_m reaching 0.38 mS/μm, in particular, is higher than all of the reported CNT RF devices. Furthermore, the CNTFETs present the intrinsic f_T and $f_{\max}$ of 281 and 190 GHz, respectively for different gate lengths. Specifically, the CNTFETs with a 50 nm L_g so far outperform all of the CNT RF transistors from a comprehensive perspective, which has an 85 GHz $f_{\max}$ and an 86 GHz pad de-embedding f_T (Figure 10) [60]. There are also reports concerning the CNTFET-based analog radio systems and high-speed circuits. Interface circuits integrating a commercial temperature sensor and CNT VCOs for semi-digital sensing were demonstrated in [61], which possess remarkable energy efficiency, ultrahigh temperature/frequency sensitivity, as well as a broad scope of tunable frequencies between 0.4–1.5 GHz that covered the required frequency bands of NB-IoT or GSM devices (Figure 11). The demonstration of an interface system for real-time wireless temperature sensing has also been attributed to a Li-ion battery (150 mAh) and a flexible antenna (center frequency 915 MHz). As suggested by this work, the energy-efficient high-speed electronics based on CNT CMOS FETs are expected to be broadly applicable, particularly in the cloud computing, smart sensor, and IoT areas.

Carbon nanotube-based doping-free CMOS technology can also be used to make large-scale biosensors that are highly sensitive, uniform, and reliable (Figure 12). Improvements have been made for the CNTFET biosensors to achieve quantitative and selective detection of specific DNA sequences and microvesicles (MVs). With extrapolated limits of detection (LODs) of 60 aM and 6 particles/mL, respectively, the improved devices set the record sensitivities of FET biosensors for examining DNAs and MVs [62]. In traditional sensing fields such as gas detection, CNTs are also a perfect material for fabricating highly-sensitive sensors primarily ascribed to their ultrahigh surface/volume ratio, which implies the physical accessibility of each atom in ambient scenarios. The H_2 sensor fabricated based on CNTs shows an 890-ppb LOD and a 7-s exceptionally fast response at 311 ppm, which represents the very first demonstration of sub-ppm room-temperature H_2 detection and the highest response among existing CNT H_2 sensors [63]. As a result, by the mature CNT material system — high semiconducting purity solution-derived CNT film, innovative but compatible structure as well as stable process, batch fabrication of ultrasensitive CNT sensors is possible and ready to assist in the initial applications of CNT devices in a few specialty areas. Besides, through on-chip integration of sensor arrays with the signal processing protocols, the CNT sensors could be extended as a multiplexed universal platform for ultra-sensitively detecting a variety of gas species and biological molecules.

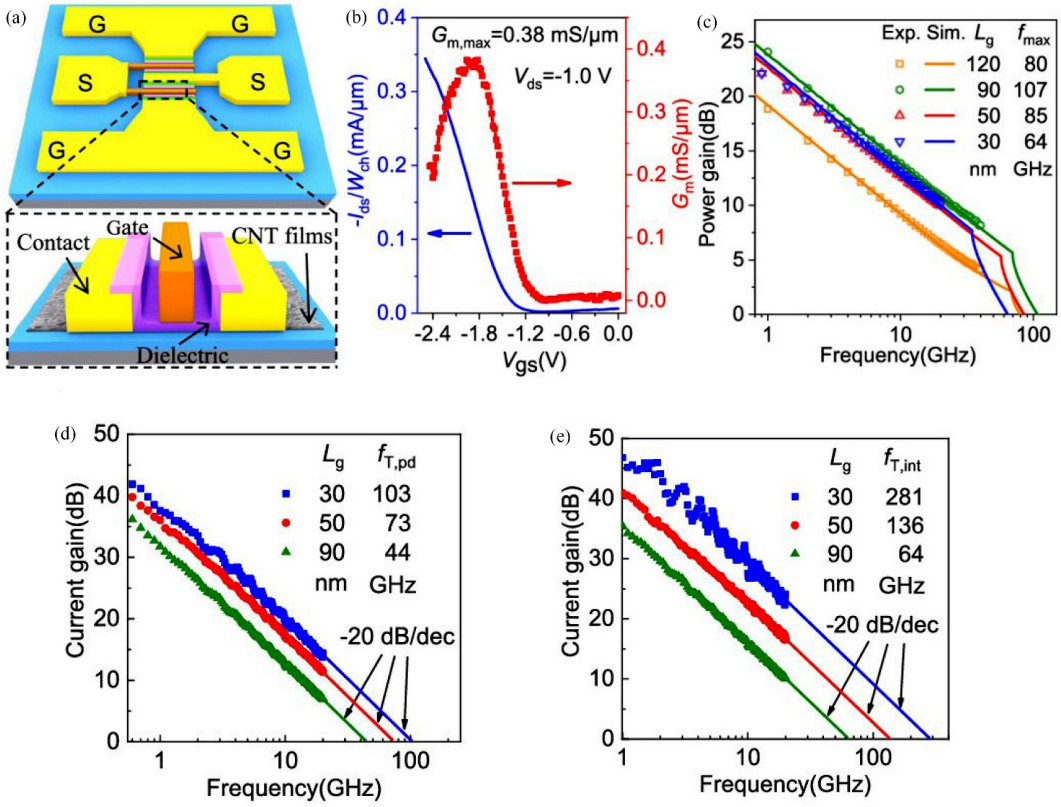

Figure 10 (Color online) (a) Structural illustration of GSG pads in a CNTRFT. Inset depicts the channel zone architecture, where the air gaps facilitate the parasitic capacitance reduction. (b) Transfer characteristic plot of the CNTRFT. (c) Graphs of pad embedding power gain against gate length, where the lines and dots respectively indicate simulation findings and experimental data. (d) Graphs of pad de-embedding current gain, as well as of (e) intrinsic current gain against the transistor frequency at various gate lengths (90, 50, and 30 nm). The extended lines have a −20 dB/dec slope [60] @Copyright 2019 American Chemical Society.

3 Recent important breakthroughs in carbon nanotube-based electronics

As mentioned earlier, despite the possibility of CNTs in producing integrated circuits sized below 10 nm, it remains necessary to scalably produce electronically pure dense semiconducting nanotube arrays (A-CNTs) on the wafers. A-CNTs with both high purity and density have yet to be demonstrated, although their fabrication has been achieved by growing nanotubes on the quartz or sapphire with high semiconducting purity (99.9999% at maximum, obtained by post-treatment) or high density (100 CNTs/mm at maximum) via the chemical vapor deposition (CVD) process [64,65]. Treatment with the "purified-and-placed" solution can endow the CNTs with high semiconducting purity. This simple and scalable method enables a capability of wafer-scale assembly [66], albeit challenges remain. It is necessary to elevate the level of semiconducting purity from 99.99% to 99.9999%, which should be achieved by upgrading the strategy of purity characterization and further sorting the CNTs. Alignment of solution-processed CNTs is required into arrays that have full wafer coverage and consistent pitch (5 to 10 nm). For the assemblage of such CNTs into arrays on the substrates, various techniques have been put forward. However, the density of these CNT arrays is either too sparse and unable to fully cover the substrate ([67] by Arnold and colleagues) or too high (> 400 CNTs/mm), causing serious screening effects from deleterious inter-tube interactions [68] (the Langmuir-Schaefer-based method [69] or the vacuum filtration method [70]). Recently, there has been a breakthrough in carbon nanotube materials. A multi-dispersion sorting technique for the preparation of a CNT-containing solution with a semiconducting purity of > 99.9999% is reported [71]. Next, well-aligned arrays of CNTs are fabricated on a 10-cm wafer having tunable densities between 100–200 CNTs/mm, which is accomplished by formulating a dimension-limited self-alignment (DLSA) technique. The produced arrays conformed to the fundamental application requirements for fabricating large-scale ICs. For the DLSA-processed A-CNT-based FETs and ICs, they outperform the traditional Si CMOS devices regarding on-state current, transconductance, and lower gate delays in terms

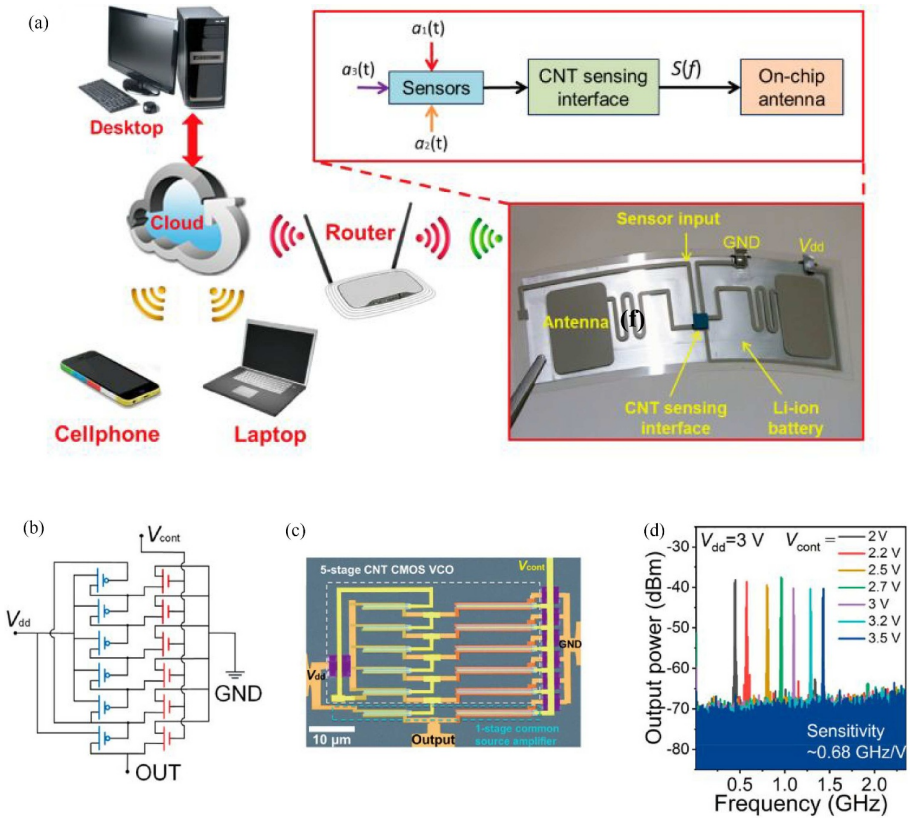

Figure 11 (Color online) (a) Illustration of a CNT IC-based universal interface system of wireless sensors. (b) Circuit schematic of a 5-stage CNT CMOS VCO. (c) Pseudo-colored SEM micrograph of a 5-stage VCO with an extra 1-stage CS amplifier (scale bars = 10 μm). The gate is 220 nm in length, and the six N-type FETs (right) all exhibit 2-fold wider channels than the six P-type FETs (left). (d) Graphs describing the oscillation frequency and output power for a representative VCO circuit. The power of the output signal, with a constant value of −40 dBm, is nearly independent of $V_{\rm cont}$, while regarding the $V_{\rm cont}$-dependent frequency, the relevant average sensitivity value is 0.68 GHz/V [61] @Copyright 2019 American Chemical Society.

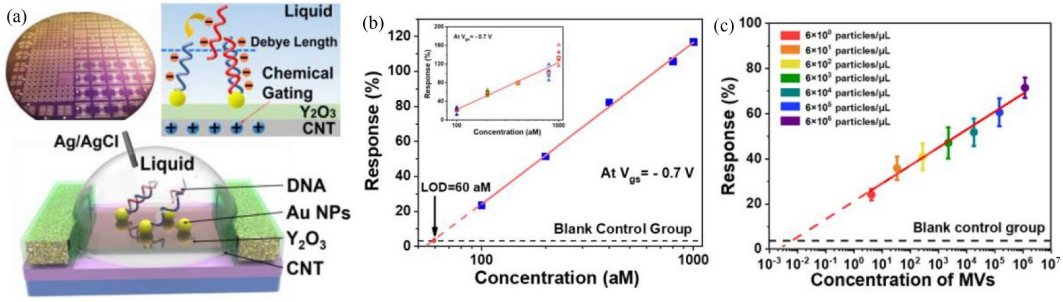

Figure 12 (Color online) (a) The top left part shows a picture of CNT floating-gate (FG) FET produced on a 10-cm wafer for biosensor applications. The top right part represents the sensing principle of an FG-FET biosensor. The bottom gives an overall biosensor schematic. (b) DNA detection calibration graph at a $V_{\rm ds}$ of −0.1 V and a $V_{\rm gs}$ of −0.7 V. Black dashed line refers to the blank control immersed in 0.1 × PBS. A 60-aM theoretical LOD is yielded by extending the linear fit plots. Inset describes the correlation between the concentration and the response for five different biosensors. The mean responses of the five devices are linearly fitted against the DNA concentration logarithmic. (c) Calibration graphs of CNT FG-FET biosensors modified with aptamer, which can achieve MV detection at concentrations varying from 6 to 6 × 10^6 particles/μL under $V_{\rm ds}$ and $V_{\rm gs}$ of −0.1 and −0.7 V, respectively. The black dashed line indicates the noise intensity (∼3.7) during a test of the blank control in 1 × PBS [62] @Copyright 2020 American Chemical Society.

of circuits (Figure 13).

Due to light carrier effective mass and small bandgap, CNTFETs usually encounter ambipolar problems, such as high off-state currents and serious SS degradation with the rising of drain bias voltage [72]. The static power consumption caused by this may offset the advantages of CNTFETs in dynamic power consumption, which is not conducive to satisfying the application criterion for the low-static-power logic electronics or the standard performance requirement of ultra-large-scale integrated circuits (ULSICs). To

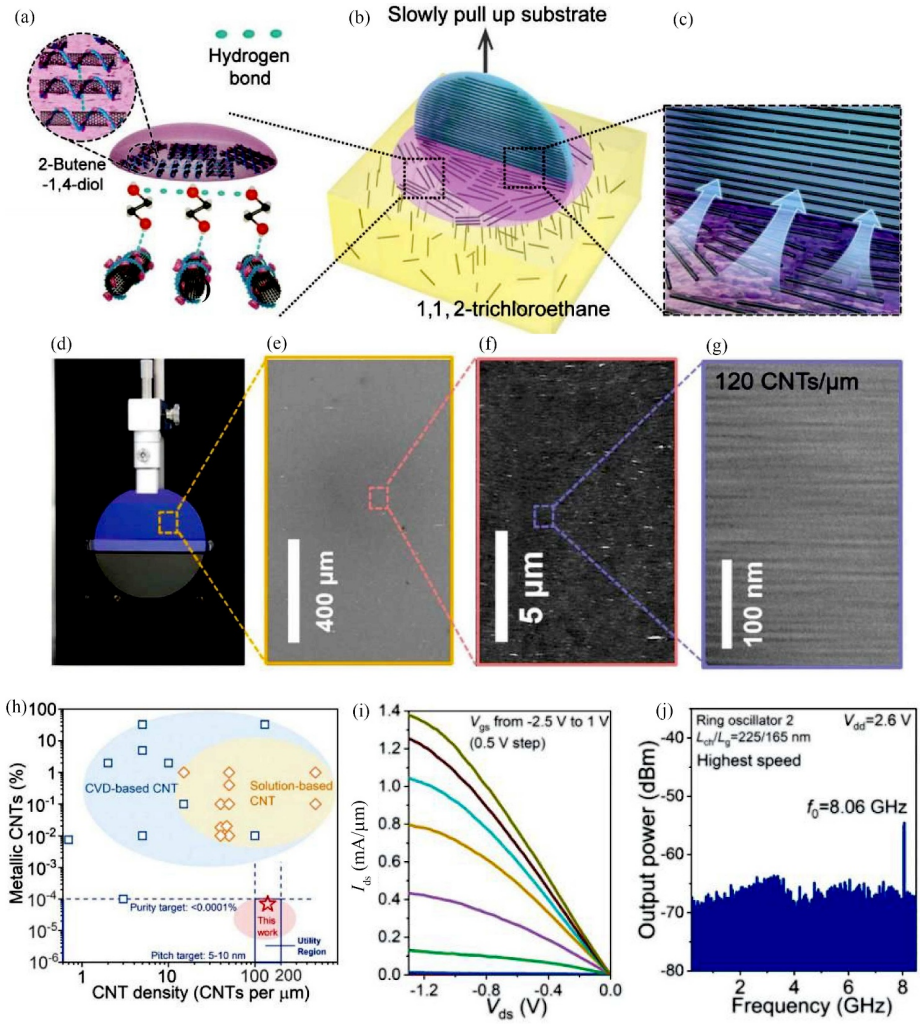

Figure 13 (Color online) (a)–(c) Process schematics for a wafer-scale A-CNT fabrication. (d) Optimal image of the deposition setup for depositing CNTs on a 4-inch silicon wafer. (e) to (g) SEM micrographs of an as-deposited A-CNT, which are acquired at various magnifications by adopting a 40-mg/ml optimal concentration of CNT solution. (h) Graph of semiconducting purity against array density. The blue hollow box represents the utility zone. Our results are within the pink zone, where a typical result is denoted as a red hollow star. (i) Output patterns for the CNTFET. (j) Power spectrum of an RO having an 80.6-GHz highest-stage switching frequency [71] @Copyright 2020 AAAS.

overcome these problems, a feedback gate (FBG) architecture, which enabled the drain region extension to the proximate CNT channels from the CNT/metal contact, has been adopted. This drain-engineered method can inhibit the tunneling current by sustaining the potential barrier thickness at the drain in an off state. The experimental results on the solution-processed CNT film-based transistors demonstrate that this gate structure is effective for improving their off-state performance. At a high drain bias V_{DS} of -2 V, the drain-engineered CNTFET having a 375-nm channel length exhibits at least 4 orders-of-magnitude on/off ratio and a sub-200 mV/dec SS, while keeping a 0.2-mS/μm peak transconductance and a high (0.2 mA/μm) on-state current (as presented in Figure 14(d)) [73]. In contrast, the SS of the self-aligned gate FET is 450 mV/dec in the same condition. This indicates that at a 1.5-V supply voltage, the CNTFETs having a sub-μm gate length can conform to the static power requirement of the normally performing ULSICs ($<$ 10 nA/μm leakage current) owing to the FBG-based architecture integration (Figure 14).

According to this idea, the demonstration of a relevant CMOS-based IC has been achieved as well. All of the CNTFETs in this IC scheme (known as the strengthened CMOS (SCMOS) logic) are arranged with an extra control gate in the drain vicinity, which is responsible for potential barrier tuning in an off state inspired by the FBG structure mentioned above. Meanwhile, IC building is achieved according to the SCMOS logic, where the extra gates of pull-down transistors in the SCMOS ICs are all connected

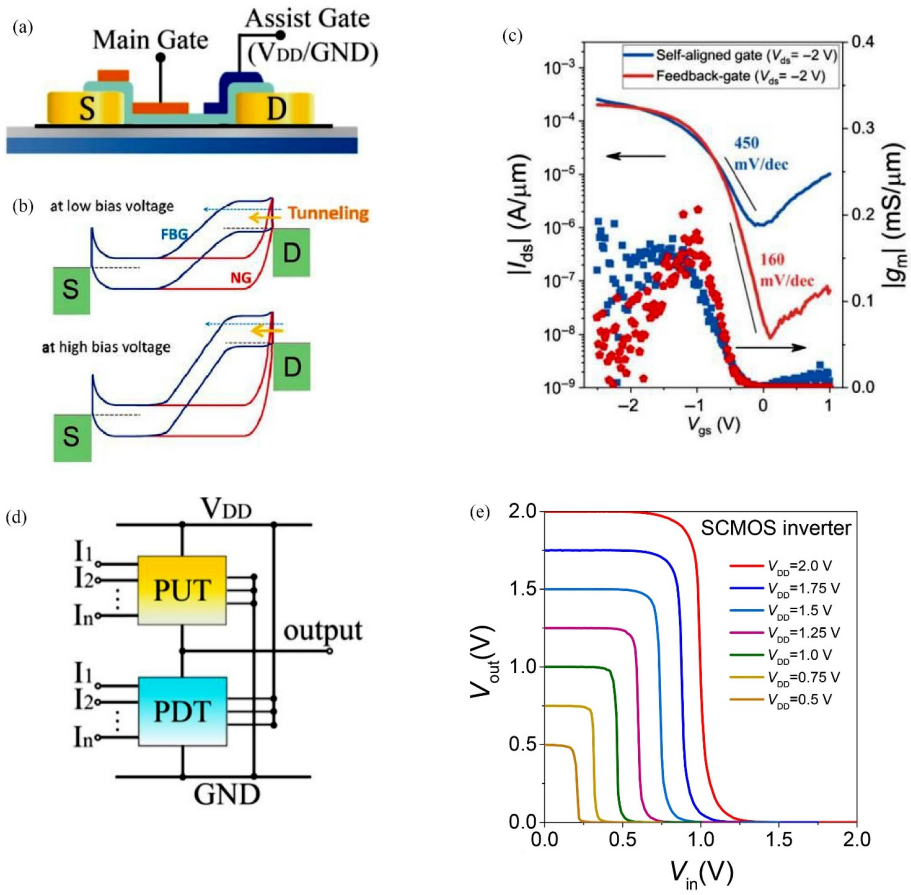

Figure 14 (Color online) (a) Structural illustration of an FBG-FET. (b) Schematic band structures of normal (red curves) and FBG (blue curves) CNTFETs at small (upper) and large biases (lower). (c) Transfer patterns of a self-aligned (SA) gate versus an FBG CNTFET under a high bias V_{ds} of −2 V. (d) Circuit schematic of a SCMOS logic gate. (e) Voltage transfer curves of an inverter based on CNT SCMOS at various supply voltages [73] @Copyright 2019 Springer Nature, and [74] @Copyright 2020 American Chemical Society.

to the power supply and those of pull-up transistors are all connected to the ground. A few typical SCMOS gates are presented, such as NAND, inverter, NOR, and multi-stage inverter strings. Compared to the CMOS gates, all of the above SCMOS gates exhibit stringent rail-to-rail outputs with 3 orders-of-magnitude static power inhibition and ignorable voltage losses at operating speeds that are similar or even higher. For transistors based on narrow-band-gap semiconductors, the transistor architecture and SCMOS logic are valuable for years, which satisfy the high-performance and low-power requirements of ULSICs concurrently as an optimal scheme (Figure 14) [74].

4 Challenge and outlook

CNT-based high-performance planar CMOS devices have been scaled down to sub-10 nm nodes. Meanwhile, CNT-based integrated circuits with performance comparable to that of silicon-based 0.18 μm CMOS have been demonstrated till the present.

Moreover, CNT-based devices are abundant in form and function. For instance, due to the excellent mechanical flexibility, high transparency, and substrate compatibility of carbon nanotube, it can realize flexible, transparent, transient, and other special chips and can construct a variety of functional devices such as sensing, storage, and logic as well as analog circuits, satisfying the needs of different applications and scenarios.

More importantly, due to the low processing temperature and low power consumption of CNT-based transistors, it is easy to overcome the main challenge of three-dimensional integrated circuits: thermal budget requirement. Thus, CNTFETs are the ideal technology to realize 3D heterogeneous integration. The theoretical simulation results demonstrate that carbon nanotube-based monolithic three-dimensional

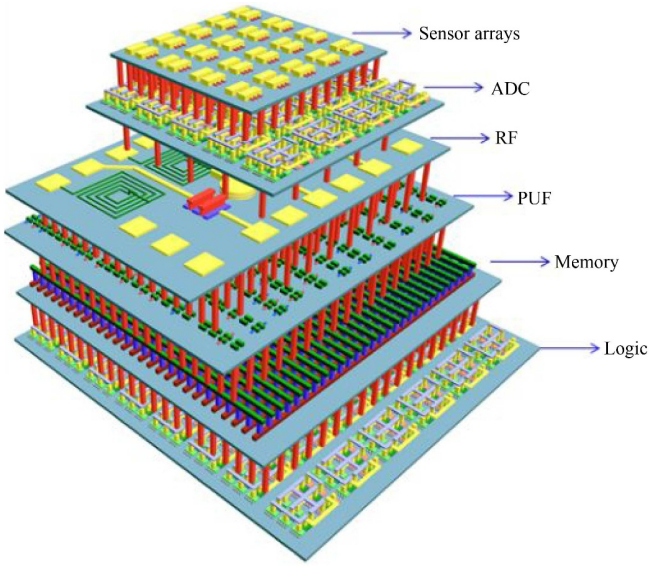

Figure 15 (Color online) Schematic diagram of three-dimensional integration of sensing, storage, and computing based on carbon nanotube-based technology.

integrated circuits have 1000 times performance and power consumption advantages over the traditional integrated circuits. Combined with the feature mentioned above that carbon nanotube can be used to construct a variety of functional devices, it is conducive to realizing the integration of sensing, memory, and computing chip in three-dimensional architecture just like the structure shown in Figure 15 [75–81].

Despite the impressive progress made by the whole community, it remains a grand challenge with a lot of obstacles to overcome. Taking the material challenges into consideration, it is essential to obtain well-aligned, all-semiconducting, single-walled CNT films with high uniformity, high array density, and low defect density on large wafers for the immediate future. In the process of preparing carbon nanotube materials, structural defects of nanotubes might be induced by high-power sonication and/or strong-acid treatments during purification and suspension processes [82]. However, such defects do not affect the quality of contacts between the nanotube and metal source/drain electrodes. Therefore, solution-processed SWNTs are still competitive in ultimately scaled field-effect transistors, where contacts will dominate electron transport rather than electron scattering in the channel region. Previous work has shown that post-deposition rinsing and annealing, for example, in vacuum or oxidizing environments, can be used to desorb and/or decompose spurious adsorbates and surfactants from the surfaces of CNTs to optimize the interface of CNT devices [83].

Correspondingly, high-throughput and high-sensitivity techniques to detect metallic nanotubes and the structural defects in assembled nanotube arrays must be developed. On the device level, the $2R_c$, $I_{\rm on}$, V_T, and SS variations of nanotube transistors need to be dramatically reduced. Thus, metalanguage and nanotube-dielectric interfaces should be carefully designed to optimize the variations of nanotube transistors. Stability and reliability are important concerns to CNT electronics. Few works focused on the stability of CNTFETs [84, 85]. CNTFETs, especially the N-type CNTFETs implemented by low work function metal contact, would be sensitive to air, and/or gradually degrade or even fail when exposed to the air without a package. Although researchers have found that the stability of CNTFETs can be improved through passivation [84, 85], some factors, especially including polymer residues in the most mature solution-derived CNTs and interface trapping states, will induce instability during the enduring operation. Additionally, fabricating CNT CMOS FETs with standard industry processes, which are compatible with conventional CMOS processes, is a significant necessity for developing CNT-based integrated circuits. In the same way, design tools for CNT-based integrated circuits are essential for the further advancement of CNT integrated circuits. In addition, the development of these tools could take years. Moreover, it should also be pointed out that almost all explorations of CNT circuits are limited to simple interconnection technology containing only 1–2 metal layers, while most modern silicon CMOS integrated circuits involve more than 10 layers of metallic interconnects.

Based on the above discussion, it can be known that carbon nanotube-based electronics has developed to a stage in which there are no fundamental bottlenecks that are foreseen to build large-scale systems

while enormous engineering challenges remain. To get through this stage smoothly, a strong public-private partnership and collaborations across different sectors of the semiconductor industry are more important than ever.

Acknowledgements This work was supported by National Key Research & Development Program (Grant No. 2016YFA0201901) and Beijing Municipal Science and Technology Commission (Grant No. Z181100004418011).

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