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A threshold voltage and drain current model for symmetric dual-gate amorphous InGaZnO thin film transistors

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Abstract Based on the drift-diffusion theory, a simple threshold voltage and drain current model for symmetric dual-gate (DG) amorphous InGaZnO (a-IGZO) thin film transistors (TFTs) is developed. In the subthreshold region, most of the free electrons are captured by trap states in the bandgap of a-IGZO, thus the ionized trap states are the main contributor to the diffusion component of device drain current. Whereas in the above-threshold region, most of the trap states are ionized, and free electrons increase dramatically with gate voltage, which in turn become the main source of the drift component of device drain current. Therefore, threshold voltage of DG a-IGZO TFTs is defined as the gate voltage where the diffusion component of drain current equals the drift one, which can be determined with physical parameters of a-IGZO. The developed threshold voltage model is proved to be consistent with trap-limited conduction mechanism prevailing in a-IGZO, with the effect of drain bias being also taken into account. The gate overdrive voltage-dependent mobility is well modeled by the derived threshold voltage, and comparisons of the obtained drain current with experiment data show good verification of our model.

Keywords amorphous InGaZnO, drift-diffusion current, dual-gate, thin film transistors, threshold voltage

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1 Introduction

Amorphous InGaZnO (a-IGZO) thin film transistors (TFTs) are becoming preference for high-quality and large-size display applications, for their reasonably high electron mobility (>10 $cm^2 \cdot V^{-1} \cdot s^{-1}$) even though fabricated at room temperature [1], good device uniformity, and relatively low fabrication costs [2]. Moreover, the high optical transmittance and flexibility of a-IGZO films have enabled various novel electronic applications based on a-IGZO TFTs, such as flexible transparent displays [3], virtual reality displays [4], transparent RFID logic chips [5], and wearable electronics [6]. However, the electrical stability, especially bias stability under illumination evaluated mainly by threshold voltage shifts turns out to be a great concern [7–9]. It is found that a-IGZO TFTs with dual-gate (DG) driving not only improve device stability significantly, but also gain higher drain current and sharper subthreshold slope while maintaining low off-state current, which is superior to the single-gate (SG) driving devices [10–16]. So far, a few studies on DC and stability performance of DG a-IGZO TFTs have been made using empirical models of MOSFETs [13–15]. Nevertheless, to the best of our knowledge, no DG a-IGZO TFTs

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DC model concerning physical properties of a-IGZO is proposed, and device models with simple, analytic and yet fairly accurate forms are required for DG a-IGZO TFTs-based circuit simulation.

Threshold voltage is an important parameter for describing electrical stability and switching behaviors of transistors. And the threshold voltage of a-IGZO TFTs is greatly influenced by density of states (DOS) in the bandgap of a-IGZO [2], which also have an effect on carrier transport in a-IGZO films. There have been three conduction mechanisms reported in a-IGZO TFTs [17–21]: (1) Trap-limited conduction (TLC) usually prevails when gate bias is not high enough to elevate the fermi level into the conduction band, under which carriers trapped in defect states are thermally activated into the conduction band and become free carriers. (2) When the fermi level enters conduction band under high gate bias, carriers transport in potential barriers above conduction band minimum (CBM), thus the dominant conduction mechanism shifts to percolation conduction, which is not found in traditional amorphous covalent semiconductors (i.e., amorphous Silicon). (3) Variable-range hopping (VRH) might be able to characterize the performance of a-IGZO TFTs under very low temperature [18]. However, the low DOS compared with amorphous Silicon causes higher free-carrier density in a-IGZO, thus the fermi level under thermal equilibrium lies in tail states and is 0.1∼0.3 eV below CBM [2]. In addition, because of the incompatibility of VRH with the other two mechanisms [21], dominant conduction mechanisms under a wide range of temperature are still TLC and percolation conduction for a-IGZO TFTs [19–21]. In the bandgap of a-IGZO, the fermi level is located in conduction band tail states under low gate bias, in which most of the induced free carriers are trapped. As the fermi level moves toward CBM with increasing gate bias, free-carrier density increases drastically and gradually surpasses the density of ionized trap states (i.e., the trapped carriers). Given the two different kinds of charge in a-IGZO TFTs, threshold condition is defined in [17] when the ratio of free-carrier density to the total gate bias-induced charge density is around 0.2, where TLC prevails. Another threshold condition called percolation threshold is also defined in [17] when the ratio reaches 0.8, indicating the transition from TLC to percolation conduction. It is proposed that degenerate conduction takes place when free-carrier density in a-IGZO channel reaches 10^{18} cm^{-3}, and the corresponding gate bias is regarded as threshold voltage [22]. Note that the above threshold voltage definitions are essentially based on charge, which are made in the linear region, with drain bias being neglected. What is more, switching behavior of a-IGZO TFTs may not be properly described with only free carriers being evaluated.

In this paper, we develop a threshold voltage model for DG a-IGZO TFTs based on drift-diffusion current, which not only takes into account the physical properties of a-IGZO films, but can describe more accurately the effect of applied electric fields on device switching behavior. Moreover, the gate overdrive voltage-dependent mobility can be obtained with the derived threshold voltage, resulting a self-consistent drain current model for DG a-IGZO TFTs.

2 Drift-diffusion theory based drain current

The schematic of DG a-IGZO TFTs is illustrated in Figure 1(a). Top gate (TG) and bottom gate (BG) electrodes are synchronized during device operation, ohmic contacts are assumed between the source/drain (S/D) metal and a-IGZO, $t_{\rm ox}$, $t_{\rm IGZO}$, and L are gate oxide thickness, the a-IGZO layer thickness, and channel length respectively, $\varphi_{\rm s}$ and φ_0 represent the surface and central potential in a-IGZO along the x-coordinate. Note that for synchronized dual-gate transistors, the effective total gate oxide capacitance is the sum of top and bottom gate oxide capacitance [13]. Different thickness of two gate oxide layer should result no change on total device drain current, as long as the effective total gate oxide capacitance remains the same value. However, big discrepancy between top and bottom oxide layer thickness may induce negative effects, e.g., gate-oxide tunneling related leakage current.

Thus symmetric gate configuration is preferred to avoid weakening on device characteristics associated with DG driving. And symmetric DG oxide TFTs have been proved experimentally with almost identical thickness of top and bottom gate oxide (the discrepancy is within several nanometers) [23]. For DG a-IGZO TFTs with typical gate oxide thickness of hundreds of nanometers, symmetric gate configuration

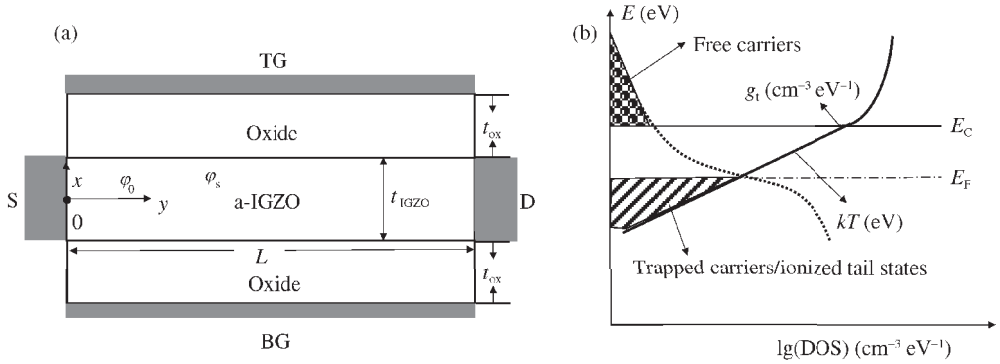

Figure 1 Schematics of (a) DG a-IGZO TFT and (b) sub-gap DOS model of a-IGZO, the dotted and solid lines are sketches of free-carrier and trap-state distributions in the bandgap of a-IGZO.

can be achieved to optimize device performance.

DC characteristics of DG a-IGZO TFTs are mainly influenced by acceptor-like trap states below the CBM of a-IGZO, and gradual channel approximation is valid for long-channel device. Thus the Poisson's equation takes the 1-D form of

$$\frac{\mathrm{d}^2\varphi(x)}{\mathrm{d}x^2} = \frac{q}{\varepsilon_\mathrm{s}}\left(n_\mathrm{free}(\varphi) + n_\mathrm{trap}(\varphi)\right), \tag{1}$$

where φ is the potential along x direction, q is electron charge, ε_s is the a-IGZO permittivity, n_free and n_trap are free-carrier and ionized trap-state density, which can be expressed as the function of potential in a-IGZO [24],

$$n_\mathrm{free} = N_\mathrm{C}\exp\left(\frac{\varphi-\varphi_\mathrm{F0}-V}{\varphi_\mathrm{th}}\right), \tag{2}$$

$$n_\mathrm{tail/deep} = \begin{cases} g_\mathrm{t/d}\dfrac{\pi kT}{\sin\left(\pi T/T_\mathrm{t/d}\right)}\exp\left(\dfrac{\varphi-\varphi_\mathrm{F0}-V}{\varphi_\mathrm{t/d}}\right), & T < T_\mathrm{t/d}, \\ g_\mathrm{t/d}\dfrac{kT}{T/T_\mathrm{t/d}-1}\exp\left(\dfrac{\varphi-\varphi_\mathrm{F0}-V}{\varphi_\mathrm{th}}\right), & T > T_\mathrm{t/d}, \end{cases} \tag{3}$$

$$n_\mathrm{trap} = n_\mathrm{tail} + n_\mathrm{deep}, \tag{4}$$

where $n_\mathrm{tail/deep}$ represent the ionized trap density of acceptor-like tail/deep states, N_C=5×10^{18} cm^{-3} is the effective conduction band DOS, $g_\mathrm{t/d}$ is the density of tail/deep states at CBM, $\varphi_\mathrm{F0} = (E_\mathrm{C}-E_\mathrm{F0})/\mathrm{q}$, E_C and E_F0 are energy of CBM and fermi level under thermal equilibrium, V is channel potential along the y-axis direction, k is Boltzmann's constant, T and $T_\mathrm{t/d}$ are temperature and characteristic temperature of tail/deep states, with $\varphi_\mathrm{th} = kT/q$ and $\varphi_\mathrm{t/d} = kT_\mathrm{t/d}/q$. Even though acceptor-like states in a-IGZO include exponentially distributed tail and deep states [25], effect of deep states on carrier transport is insignificant considering that the initial position of fermi level (E_F0) lies in tail states, and g_d is much lower than g_t, thus we only consider the ionized trap density of tail states in (1) (i.e., $n_\mathrm{tail}\approx n_\mathrm{deep}$) [26]. Boundary conditions are obtained using Gauss's law,

$$\varepsilon_\mathrm{s}\frac{\mathrm{d}\varphi}{\mathrm{d}x}\bigg|_{x=\frac{t_\mathrm{IGZO}}{2}} = C_\mathrm{ox}\left(V_\mathrm{GS}-V_\mathrm{fb}-\varphi_\mathrm{s}\right), \tag{5}$$

$$\frac{\mathrm{d}\varphi}{\mathrm{d}x}\bigg|_{x=0} = 0, \tag{6}$$

where $C_\mathrm{ox} = \varepsilon_\mathrm{ox}/t_\mathrm{ox}$ is the gate oxide capacitance per unit area, ε_ox is the oxide permittivity, V_GS is the gate bias, $V_\mathrm{fb} = (W_\mathrm{m}-\chi_\mathrm{IGZO})/q - \varphi_\mathrm{F0}$ is the flat-band voltage in which W_m and χ_IGZO are gate metal work function and electron affinity of a-IGZO. In subthreshold region, most of the free carriers

are trapped in tail states, thus we only consider the ionized trap states in (1) with (5) and (6), and integrate (1) from 0 to $t_{\mathrm{IGZO}}/2$ once and twice to obtain

$$C_{\mathrm{ox}}\left(V_{\mathrm{GS}}-V_{\mathrm{fb}}-\varphi_{\mathrm{s}}\right)=\sqrt{2q\varepsilon_{\mathrm{s}}n_{\mathrm{t0}}\varphi_{\mathrm{t}}\left[\exp\left(\frac{\varphi_{\mathrm{s}}-\varphi_0}{\varphi_{\mathrm{t}}}\right)-1\right]\exp\left(\frac{\varphi_0-V}{\varphi_{\mathrm{t}}}\right)}, \tag{7}$$

$$\varphi_{\mathrm{s}}-\varphi_0=\varphi_{\mathrm{t}}\ln\left\{\sec^2\left[\sqrt{\frac{qn_{\mathrm{t0}}}{2\varepsilon_{\mathrm{s}}\varphi_{\mathrm{t}}}}\frac{t_{\mathrm{IGZO}}}{2}\exp\left(\frac{\varphi_0-V}{2\varphi_{\mathrm{t}}}\right)\right]\right\}, \tag{8}$$

in which $n_{\mathrm{t0}}=g_{\mathrm{t}}(\pi\mathrm{k}T/\sin(\pi T/T_{\mathrm{t}}))\exp(-\varphi_{\mathrm{F0}}/\varphi_{\mathrm{t}})$, and Eq. (7) can be rewritten as follows by using (8) [27]:

$$C_{\mathrm{ox}}\left(V_{\mathrm{GS}}-V_{\mathrm{fb}}-\varphi_{\mathrm{s}}\right)=\sqrt{2q\varepsilon_{\mathrm{s}}n_{\mathrm{t0}}\varphi_{\mathrm{t}}\exp\left(\frac{\varphi_0-V}{\varphi_{\mathrm{t}}}\right)}\tan\left[\sqrt{\frac{qn_{\mathrm{t0}}}{2\varepsilon_{\mathrm{s}}\varphi_{\mathrm{t}}}}\frac{t_{\mathrm{IGZO}}}{2}\exp\left(\frac{\varphi_0-V}{2\varphi_{\mathrm{t}}}\right)\right]. \tag{9}$$

Then applying Taylor's expansion to (8) and (9) we obtain

$$\varphi_{\mathrm{s}}-\varphi_0=A_1\exp\left(\frac{\varphi_0-V}{\varphi_{\mathrm{t}}}\right), \tag{10}$$

$$V_{\mathrm{GS}}-V_{\mathrm{fb}}-\varphi_{\mathrm{s}}=A_2\exp\left(\frac{\varphi_0-V}{\varphi_{\mathrm{t}}}\right), \tag{11}$$

where $A_1=(t_{\mathrm{IGZO}}/2)^2\mathrm{q}n_{\mathrm{t0}}/2\varepsilon_{\mathrm{s}}$ and $A_2=(t_{\mathrm{IGZO}})\mathrm{q}n_{\mathrm{t0}}/C_{\mathrm{ox}}$, then the relationship between φ_0 and V_{GS} is given as

$$\varphi_0=V_{\mathrm{GS}}-V_{\mathrm{fb}}-(A_1+A_2)\exp\left(\frac{\varphi_0-V}{\varphi_{\mathrm{t}}}\right). \tag{12}$$

Because free carriers are far less than ionized trap states in subthreshold region, electric fields of TG and BG may penetrate into the a-IGZO layer and interact with each other, which can be included by considering the central potential (φ_0). Analytical expression of φ_0 is obtained by using the principal branch of the Lambert W function [28],

$$\varphi_0=V_{\mathrm{GS}}-V_{\mathrm{fb}}-B\varphi_{\mathrm{t}} \tag{13}$$

with $B=W_0\{[(A_1+A_2)/\varphi_{\mathrm{t}}]\exp[(V_{\mathrm{GS}}-V_{\mathrm{fb}}-V)/\varphi_{\mathrm{t}}]\}$. By combining (11) with (13), the surface potential in subthreshold region ($\varphi_{\mathrm{s\_sub}}$) is obtained as

$$\varphi_{\mathrm{s\_sub}}=V_{\mathrm{GS}}-V_{\mathrm{fb}}-A_2\exp\left(\frac{V_{\mathrm{GS}}-V_{\mathrm{fb}}-B\varphi_{\mathrm{t}}-V}{\varphi_{\mathrm{t}}}\right). \tag{14}$$

In above-threshold region, free carriers begin to increase significantly and the amount of ionized trap states is in turn negligible. With free carriers being considered in (1), (5), and (6), we have

$$C_{\mathrm{ox}}\left(V_{\mathrm{GS}}-V_{\mathrm{fb}}-\varphi_{\mathrm{s}}\right)=\sqrt{2q\varepsilon_{\mathrm{s}}n_{\mathrm{f0}}\varphi_{\mathrm{th}}\left[1-\exp\left(\frac{\varphi_0-\varphi_{\mathrm{s}}}{\varphi_{\mathrm{th}}}\right)\right]\exp\left(\frac{\varphi_{\mathrm{s}}-V}{\varphi_{\mathrm{th}}}\right)}, \tag{15}$$

where $n_{\mathrm{f0}}=N_{\mathrm{C}}\exp(-\varphi_{\mathrm{F0}}/\varphi_{\mathrm{th}})$. In the above-threshold region, conducting channels formed at the top and bottom surfaces of a-IGZO layer screen gate electric fields, thus φ_0 stops increasing with gate bias after reaching a maximum value $\varphi_{0\max}$ [29], calculated as $\varphi_{0\max}=V+\varphi_{\mathrm{th}}\ln(2\pi^2\varepsilon_{\mathrm{s}}\varphi_{\mathrm{th}}/(\mathrm{q}n_{\mathrm{f0}}{t_{\mathrm{IGZO}}}^2))$ with (8), which is much smaller than φ_{s}. Therefore, the exponential term in the square bracket of (15) concerning φ_0 is negligible and the surface potential in above-threshold region ($\varphi_{\mathrm{s\_abv}}$) is given as

$$\varphi_{\mathrm{s\_abv}}=V_{\mathrm{GS}}-V_{\mathrm{fb}}-2\varphi_{\mathrm{th}}W_0\left[\sqrt{\frac{q\varepsilon_{\mathrm{s}}n_{\mathrm{f0}}}{2\varphi_{\mathrm{th}}C_{\mathrm{ox}}^2}}\exp\left(\frac{V_{\mathrm{GS}}-V_{\mathrm{fb}}-V}{2\varphi_{\mathrm{th}}}\right)\right]. \tag{16}$$

The surface potential φ_{s} from subthreshold to above-threshold region can be unified by smooth function

$$\varphi_{\mathrm{s}}=\frac{1}{n}\ln\left\{1/\left[1/\exp\left(n\varphi_{\mathrm{s\_sub}}\right)+1/\exp\left(n\varphi_{\mathrm{s\_abv}}\right)\right]\right\} \tag{17}$$

with n (>10) being a good fitting parameter.

According to the drift-diffusion theory [27,30], drain current (I) for symmetric DG transistors can be expressed as

$$I = 2\mu\frac{W}{L}C_{\rm ox}\left[(V_{\rm GS}-V_{\rm fb})(\varphi_{\rm sl}-\varphi_{\rm s0})-\frac{1}{2}\left(\varphi_{\rm sl}^2-\varphi_{\rm s0}^2\right)+\varphi_{\rm t}(\varphi_{\rm sl}-\varphi_{\rm s0})\right], \tag{18}$$

where μ is the field effect mobility, W and L are the channel width and length, the first two terms in the square bracket represent the drift current component ($I_{\rm drift}$) and the last term is the diffusion component ($I_{\rm diff}$), $\varphi_{\rm sl}$ and $\varphi_{\rm s0}$ are surface potential at drain and source respectively. As we have clarified, TLC is the dominant mechanism in subthreshold region, under which the free carriers are far less than the ionized trap states, thus the drain current is dominated by diffusion. In above-threshold region, trap states are generally filled up by electrons, and the drain current is dominated by drift component contributed from free carriers. The drift-diffusion current used in MOSFETs has been widely proved to be applicable to a-IGZO TFTs [31–33]. Thus the drain current ($I_{\rm DS}$) for all operation region is developed as

$$I_{\rm DS} = 2\mu\frac{W}{L}C_{\rm ox}\left[(V_{\rm GS}-V_{\rm fb})(\varphi_{\rm sl}-\varphi_{\rm s0})-\frac{1}{2}\left(\varphi_{\rm sl}^2-\varphi_{\rm s0}^2\right)+\varphi_{\rm th}(\varphi_{\rm sl}^*-\varphi_{\rm s0}^*)+\varphi_{\rm t}(\varphi_{\rm sl}-\varphi_{\rm s0})\right], \tag{19}$$

where

$$\varphi_{\rm sl}^* = V_{\rm GS}-V_{\rm fb}-2m\varphi_{\rm th}W_0\left[\sqrt{\frac{q\varepsilon_{\rm s}n_{\rm f0}}{2\varphi_{\rm th}C_{\rm ox}^2}}\exp\left(\frac{V_{\rm GS}-V_{\rm fb}-V_{\rm DS}}{2m\varphi_{\rm th}}\right)\right], \tag{20}$$

$$\varphi_{\rm s0}^* = V_{\rm GS}-V_{\rm fb}-2m\varphi_{\rm th}W_0\left[\sqrt{\frac{q\varepsilon_{\rm s}n_{\rm f0}}{2\varphi_{\rm th}C_{\rm ox}^2}}\exp\left(\frac{V_{\rm GS}-V_{\rm fb}}{2m\varphi_{\rm th}}\right)\right], \tag{21}$$

m is a parameter controlling the transition of drain current from subthreshold to above-threshold region, and $V_{\rm DS}$ is the drain bias. Therefore, the drift-diffusion theory based drain current of symmetric DG a-IGZO TFTs can be calculated with (19). Transfer and output characteristics from this analytical model and 2D numerical simulations with TCAD tools are compared in Figure 2, related parameters are listed in Table 1. Note that physical parameters of a-IGZO are chosen referring to [2,24,25], and current-voltage characteristics are well described by the drift-diffusion theory based drain current. TFTs in Figure 2(a) and (b) use different trap-state distribution parameter $\varphi_{\rm t}$, $\varphi_{\rm t} = kT_{\rm t}/{\rm q}$, where $kT_{\rm t}$ is the inverse slope of the exponential distribution of conduction band tail states, as shown in Figure 1(b). The greater $kT_{\rm t}$ is, the slower the fermi level moves toward CBM with increasing gate voltage, indicating less steep subthreshold slope, as shown by transfer curves in Figure 2(a) ($kT_{\rm t}$ = 0.05 eV) and (b) ($kT_{\rm t}$ = 0.065 eV), which confirm the leading position of ionized trap states in subthreshold region.

It should be noted that even though the 2D numerical simulation by TCAD tools can reproduce well the device current-voltage characteristics, the numerical procedures are not suited for circuit simulation. Moreover, since the lack of specific mobility model for a-IGZO TFTs in the TCAD environment, field effect mobility (μ) is taken as low field mobility (μ_0) during the simulation, which is not the case for actual devices under high gate electric field. The gate overdrive voltage-dependent field effect mobility will be discussed in Section 4.

3 Threshold definition and discussion

Threshold voltage of DG a-IGZO TFTs is defined as the gate voltage where the drift current equals the diffusion one, corresponding to the dominant charge in a-IGZO channels changes from ionized traps to free electrons. In linear region, $\varphi_{\rm sl}-\varphi_{\rm s0}\approx V_{\rm DS}$, and in saturation region, $\varphi_{\rm sl}\approx V_{\rm GS}-V_{\rm fb}$, thus the drift current term in (18) is given in linear region ($I_{\rm drift}^{\rm lin}$) and saturation region ($I_{\rm drift}^{\rm sat}$) respectively as

$$I_{\rm drift}^{\rm lin} = 2\mu\frac{W}{L}C_{\rm ox}\left(V_{\rm GS}-V_{\rm fb}-\varphi_{\rm s0}-\frac{1}{2}V_{\rm DS}\right)V_{\rm DS}, \tag{22}$$

$$I_{\rm drift}^{\rm sat} = \mu\frac{W}{L}C_{\rm ox}(V_{\rm GS}-V_{\rm fb}-\varphi_{\rm s0})^2. \tag{23}$$

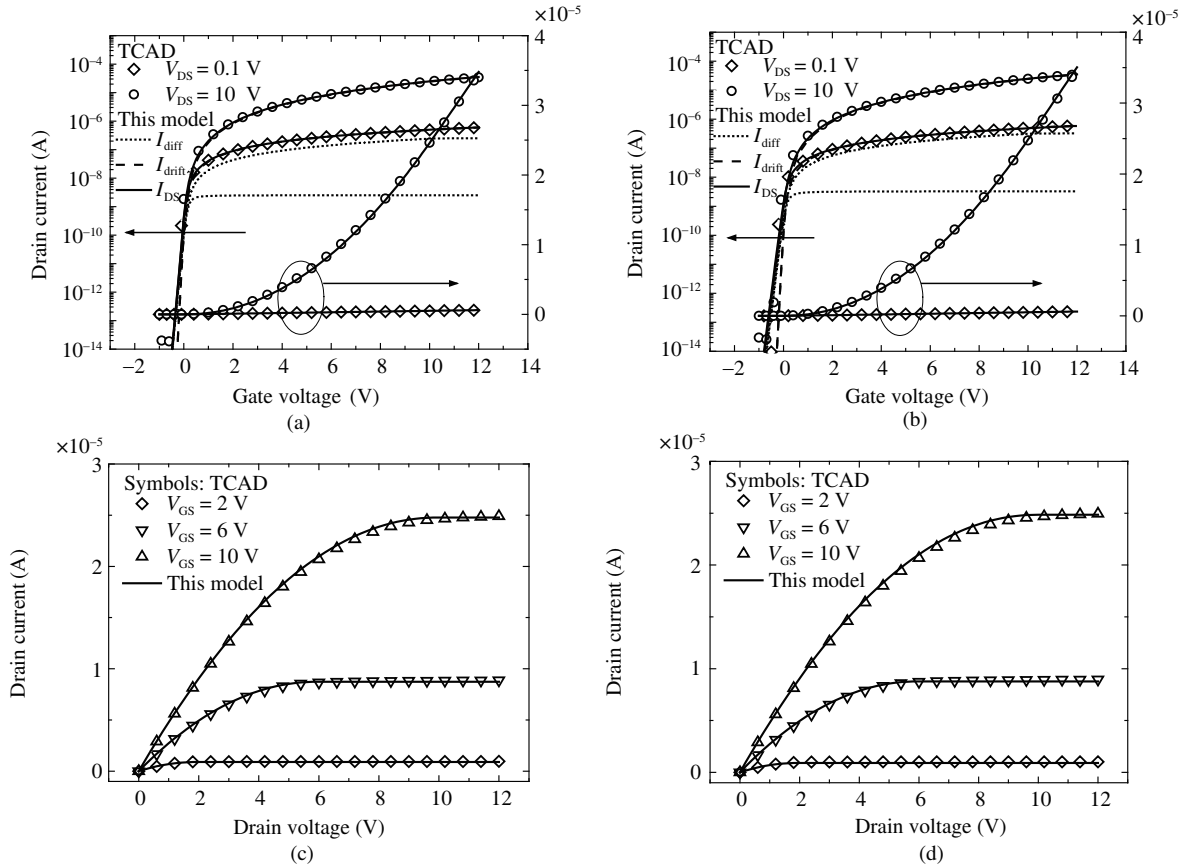

Figure 2 Current-voltage characteristics of DG a-IGZO TFTs from this analytical model (solid lines) and TCAD simulations (symbols) at T=300 K. (a) and (b) are transfer curves with φ_t set as 0.05 V and 0.065 V; (c) and (d) are output curves with φ_t set as 0.05 V and 0.065 V. The dashed and dotted lines represent the drift and diffusion components of drain current respectively.

Table 1 Parameters and the calculated threshold voltage in this model [2, 24, 25]

Symbol (unit)	V_{th}^{lin} (V)	V_{th}^{sat} (V)	W/L (μm/μm)	t_{IGZO} (nm)	C_{ox} (F·cm^{-2})	μ_0 (cm$^2\cdot$V$^{-1}\cdot$s^{-1})	g_t (cm$^{-3}\cdot$eV^{-1})	φ_t (V)	φ_{F0} (V)	V_{fb} (V)	m
TFT in Figure 2(a) and (c)	0.08	−0.01	20/20	50	1.73×10^{-8}	15	1×10^{18}	0.05	0.3	0	0.8
TFT in Figure 2(b) and (d)	0.11	0.14	20/20	50	1.73×10^{-8}	15	1×10^{18}	0.065	0.3	0	0.9

Then the threshold voltage in linear (V_{th}^{lin}) and saturation region (V_{th}^{sat}) are obtained as follows with (18), (22), (23), and I_{drift}=I_{diff}:

$$V_{th}^{lin} = V_{fb} + \varphi_{s0\_th} + \frac{1}{2}V_{DS} + \frac{\varphi_t}{V_{DS}}\left(\varphi_{sl\_th} - \varphi_{s0\_th}\right), \tag{24}$$

$$V_{th}^{sat} = V_{fb} + \varphi_{s0\_th} + \sqrt{\varphi_t\left(\varphi_{sl\_th} - \varphi_{s0\_th}\right)}, \tag{25}$$

where φ_{s0_th} and φ_{sl_th} are φ_{s0} and φ_{sl} respectively at threshold condition. Note that even though the definition of threshold condition is based on current, the derived threshold voltage is independent of field effect mobility as shown in (24) and (25). The calculated threshold voltage in Figure 2(a) and (b) are also given in Table 1.

The channel potential is related to gate bias and DOS of a-IGZO, with (2) to (4) and parameters set as in Figure 2(b), the variation of n_{free} and n_{trap} with gate bias are given in Figure 3. In addition, λ is defined as the ratio of free electron density to the total electron density induced by gate voltage [17]

$$\lambda = \frac{n_{free}}{n_{free} + n_{trap}}. \tag{26}$$

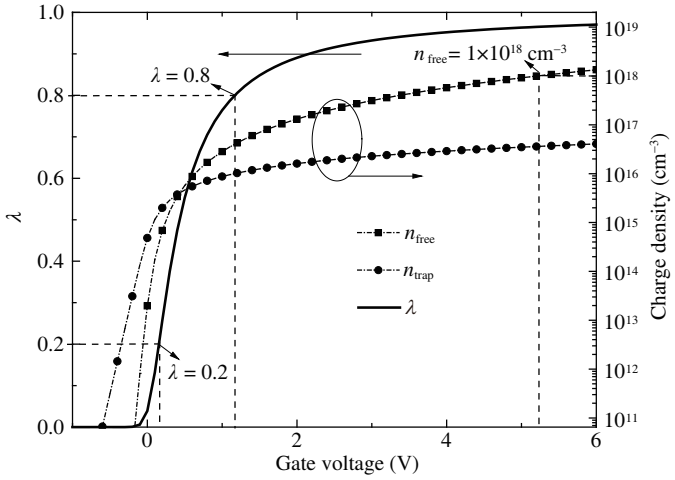

Figure 3 Variations of $n_{\rm free}$, $n_{\rm trap}$ and λ with the gate voltage.

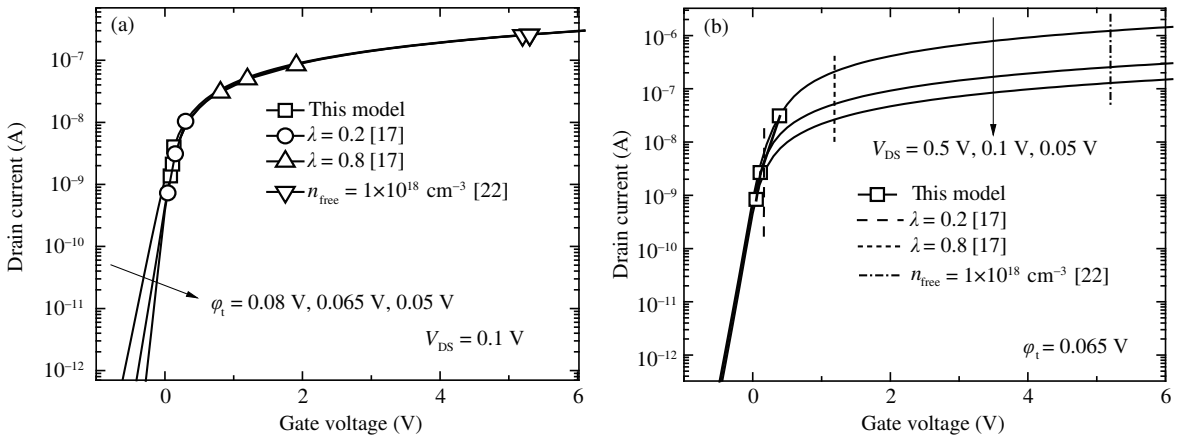

Figure 4 Comparison of threshold voltage obtained by different definition methods under various (a) $\varphi_{\rm t}$ and (b) $V_{\rm DS}$.

The variation of λ with gate voltage is also shown in Figure 3. By involving the conduction mechanisms in a-IGZO, research in [17] defined the threshold and percolation threshold voltage of a-IGZO TFTs when λ is 0.2 and 0.8 respectively, and ref. [22] defined the threshold voltage when degenerate conduction begins to happen in a-IGZO, where $n_{\rm free}$ is around 10^{18} cm^{-3}.

With various $\varphi_{\rm t}$ and $V_{\rm DS}$, Figure 4(a) and (b) show the comparison of threshold voltage of DG a-IGZO TFTs defined by different methods. For the threshold voltage model in this paper, the intersection of diffusion and drift drain current moves toward positive direction with greater $\varphi_{\rm t}$, because of more gradual subthreshold slope of the diffusion component. For the two kinds of threshold voltage defined according to λ, greater $\varphi_{\rm t}$ indicates less free electron density and thus higher gate bias to reach the specified λ value. Threshold voltage defined by λ=0.8 also indicates that percolation conduction begins in a-IGZO, where fermi level moves into conduction band, thus leading to greater threshold voltage values. In addition, the definition of $n_{\rm free}$=10^{18} cm^{-3} derives the highest threshold voltage in Figure 4, and the corresponding threshold drain current ($I_{\rm th}$) is obviously too high to be practical. Thus the definition is only applicable to a-IGZO films with small $\varphi_{\rm t}$ (e.g., $\varphi_{\rm t}$<$\varphi_{\rm th}$), where free electrons can quickly fill the traps and reach a high density under low gate bias. As shown in Figure 4(b), threshold voltage defined by λ and $n_{\rm free}$ do not change with $V_{\rm DS}$, for the two methods neglect the effects of $V_{\rm DS}$ in linear region. On the contrary, $V_{\rm th}$ calculated by (24) changes with $V_{\rm DS}$, and even if $V_{\rm DS}$ keeps increasing that device operates in saturation region, $V_{\rm th}$ can still be obtained by (25). It is shown in Figure 4 that threshold voltage calculated by (24) is closer to that defined by λ=0.2, indicating TLC prevails around the threshold condition, and showing the physical reasonability of our current-based threshold voltage definition.

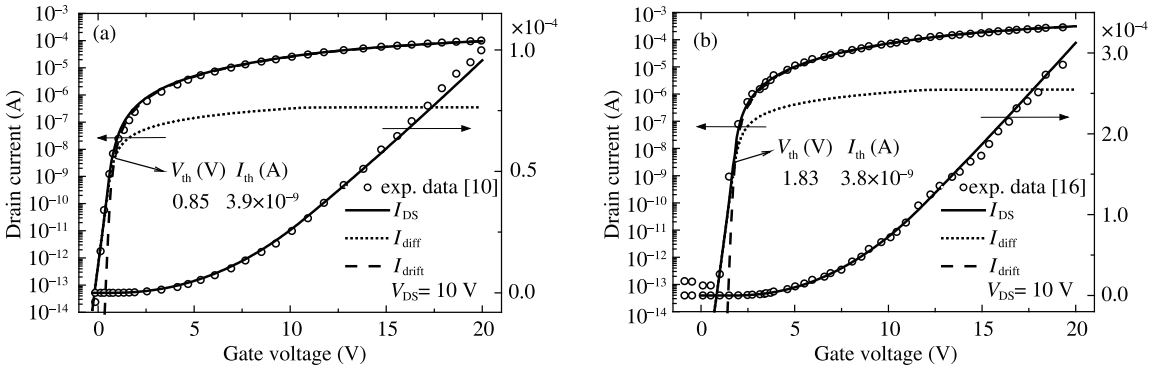

Figure 5 Comparison of transfer curves between this model (solid lines) and experiment data (symbols) in (a) [10], (b) [16], with the dashed and dotted lines being the drift and diffusion drain current respectively. Values of parameters in [10]: t_{IGZO}=30 nm, C_{ox}=1.73×10^{-8} F·cm^{-2}, μ_0=13 cm$^2\cdot$V$^{-1}\cdot$s^{-1}, g_t=8.5×10^{17} cm^{-3}eV^{-1}, φ_t=0.08 V, φ_{F0}=0.5 V, V_{fb}=0.4 V, m=0.7, γ=0.14. Values of parameters in [16]: W/L=40 μm/5 μm, t_{IGZO}=70 nm, C_{ox}=1.73×10^{-8} F·cm^{-2}, μ_0=6.5 cm$^2\cdot$V$^{-1}\cdot$s^{-1}, g_t=8.0×10^{16} cm^{-3}eV^{-1}, φ_t=0.085 V, φ_{F0}=0.2 V, V_{fb}=1.8 V, m=0.9, γ=0.10.

4 Model verification with experiment data

Unlike conventional crystalline semiconductors, in which the carrier mobility usually decease with increasing carrier density because of scattering by ionized donors or acceptors, electron mobility in a-IGZO increases with increasing free electron density for the peculiar band structures of a-IGZO, which is usually characterized by $\mu_0 n_{free}/(n_{free}+n_{trap})$ [19, 34]. Because the density of free electrons is dependent on the gate voltage, the field effect mobility of a-IGZO TFTs can be well modeled by a power function of the gate overdrive voltage, which can be expressed as [17, 18]

$$\mu = \mu_0 (V_{GS} - V_{th})^{\gamma}, \tag{27}$$

where μ_0 is the low-field mobility and γ is a parameter related to trap states and temperature [35–37]. The drift-diffusion current based threshold voltage (V_{th}) is obtained by (25) with parameters given in Figure 5, then the μ in (27) is calculated. Note that the mobility terms in I_{drift} and I_{diff} are cancelled while calculating the threshold voltage, thus Eq. (27) is consistent with (18), (19) and the proposed threshold voltage model. Figure 5 shows comparisons of transfer curves calculated by this model and experiment data [10, 16], good fitting results are achieved with parameters given in the caption. The calculated V_{th} in [10, 16] are 0.85 V and 1.83 V respectively, also displayed in Figure 5, corresponding to the I_{th} of 3.9×10^{-9} A and 3.8×10^{-9} A. The calculated threshold voltage values are approximate to that obtained by extrapolation method from experiment curves (1.1 V in [10] and 1.4 V in [16]), and the fitting results indicate well modeled gate overdrive voltage-dependent mobility, testifying the practicability of our model for describing switching behaviors of DG a-IGZO TFTs.

5 Conclusion

Threshold voltage and drain current model for symmetric DG a-IGZO TFTs based on drift-diffusion theory have been developed in this paper, which involves the ionized trap states and free electrons dominating in subthreshold and above-threshold region respectively. Threshold voltage is defined as the gate voltage where the diffusion drain current component equals the drift one, which can be calculated provided with device parameters and physical parameters of a-IGZO. The threshold voltage model which has clear physical meaning is more accurate and practical compared with models based on charge, showing consistence with the TLC mechanism prevailing in a-IGZO around threshold condition. With the proposed threshold voltage model, gate overdrive voltage-dependent field effect mobility of DG a-IGZO TFTs is well described, and the drain current of device can be modeled with simple analytical expression.

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Conflict of interest The authors declare that they have no conflict of interest.

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