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Terahertz detector for imaging in 180-nm standard CMOS process

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Abstract A CMOS terahertz (THz) detector implemented in a 180-nm standard CMOS process is proposed, and room-temperature detection of 0.94-THz radiation is demonstrated. The detector consists of an integrated on-chip patch antenna and a source-feeding NMOS transistor as the rectifying element. To improve the power transfer efficiency between the patch antenna and NMOS transistor, a novel short-stub matching network is proposed. An open quarter-wavelength microstrip transmission line connecting gate is proposed to eliminate the influence of the bonding wire and pad on the antenna-transistor impedance matching. Illuminated by a 0.94-THz BWO source, the measured voltage responsivity (R_v) and noise equivalent power (NEP) of the detector are 31 V/W and 1.1 nW/Hz$^{1/2}$, respectively.

Keywords terahertz detector, terahertz imaging, CMOS, patch antenna, matching network

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1 Introduction

The terahertz (THz) frequency range (0.3–3 THz) has received a considerable amount attention in recent years. There are many application areas of THz waves such as security check [1–3], nondestructive inspection [4], biology [5], radio astronomy [6], and communication [7]. Due to the capability of THz radiation to penetrate materials such as plastic, wood and paper sheets, the THz imaging technique is a promising alternative to currently non-invasive imaging such as X-ray or millimeter-wave imaging. Compared to X-ray imaging, THz imaging is safe for biological tissues owing to the low photon energy of THz radiation. Compared to millimeter-wave imaging, THz imaging can achieve a much higher resolution because of its relatively short wave length. The lack of low-cost and intensively integrated detectors was once a major obstacle to building low-cost, small volume and high frame-rate THz imaging systems. Most of the THz imaging systems today apply lock-in measurement techniques through mechanical raster scanning to acquire images with very slow frame rates, which are bulky and complicated. Therefore, a fully integrated THz image sensor will be a very intelligent approach to realizing high frame-rate THz cameras in the future. Owing to the advantages of low cost, high yield, and easy integration, CMOS technology is

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becoming an alternative to other technologies such as bolometers [8], photoconductive detectors [9], and high electron mobility transistors (HEMT) [10,11]. THz detectors using field-effect transistors (FET) are based on the plasma wave theory proposed by Dyakonov and Shur [12, 13], which allows the detection of THz radiations far beyond the characteristic frequency (f_{T}) of FET devices. The first silicon FET detector was demonstrated by Knap et al. [14]. Furthermore, a CMOS-based multi-pixel THz detector array with an integrated silicon lens was reported by Hadi and Sherry et al. in 2011 [15]. The array could sense radiation with frequencies ranging from 0.6 to 1 THz. A 1k-pixel THz video camera chip was presented in 2012 [16]. In addition, detectors can also be implemented by adopting a Schottky-diode with the CMOS process, and a 130-nm digital CMOS implementation was presented in [17, 18], which functioned well under the illumination of 280 GHz radiation.

Although CMOS-based THz detectors and imaging arrays are rapidly being developed, there is still much progress to be made in improving the detector performance. CMOS THz detectors are mainly composed of an on-chip antenna and NMOS transistors. Many efforts have been made in designing high-performance on-chip antennae. However, matching networks between antenna and NMOS transistors also play an important role. Antenna-transistor impedance mismatching will significantly decrease the THz power that transistors receive, drastically lowering the detectors output magnitude. The design of matching networks is difficult due to the inaccurate physical model of FETs at THz frequencies.

This paper proposes a CMOS THz detector, which consists of an integrated on-chip patch antenna and an NMOS transistor. A novel matching network inserted between the antenna and NMOS transistor, as well as its design method, is presented. Considering the influence of the bonding wire and pad on antenna-transistor impedance matching, an open quarter-wavelength microstrip transmission line is proposed to eliminate this influence. The detector is implemented in a 180-nm standard CMOS process and achieves a voltage responsivity (R_{v}) of 31 V/W and a noise equivalent power (NEP) of 1.1 nW/Hz$^{1/2}$ at 0.94 THz at room temperature. The paper proceeds as follows: Section 2 presents a theoretical analysis of THz power detection, Section 3 presents the detailed design of the proposed THz detector, Section 4 shows the measurement results and analysis, and Section 5 concludes this paper.

2 Theoretical analysis

This section presents a theoretical analysis of THz power detection. A schematic used for the analysis is shown in Figure 1. A THz signal $U_a \cos \omega t$ is coupled to the source of a non-biased NMOS transistor. As THz frequencies are much higher than the cut-off frequency of the transistor, the THz signal will be attenuated significantly. We assume that the amplitude of the THz signal is zero at the drain. The boundary condition at the drain is subject to $V_{\mathrm{D}} = 0$; therefore, the drain-source voltage is

$$V_{\mathrm{DS}}(t) = -U_a \cos \omega t, \tag{1}$$

and the gate-source voltage is

$$V_{\mathrm{GS}}(t) = V_{\mathrm{G}} - U_a \cos \omega t. \tag{2}$$

The device is operated in the triode region. The drain current $i_{\mathrm{DS}}(t)$ is

$$i_{\mathrm{DS}}(t) = g_{\mathrm{DS}}(t) V_{\mathrm{DS}}(t), \tag{3}$$

where $g_{\mathrm{DS}}(t)$ is channel conductance. For strong inversion, $g_{\mathrm{DS}}(t)$ can be written as [19]

$$g_{\mathrm{DS}}(t) = \mu_n C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{GS}}(t) - V_{\mathrm{th}}) - \frac{1}{2} V_{\mathrm{DS}}(t), \tag{4}$$

where W and L are the width and length of the channel, respectively, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area and V_{th} is the threshold voltage. Combining (1)–(4), we get

$$i_{\mathrm{DS}}(t) = \mu_n C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{th}} - V_G) U_a \cos \omega t + \mu_n C_{\mathrm{ox}} \frac{W}{4L} U_a^2 \cos 2\omega t + \mu_n C_{\mathrm{ox}} \frac{W}{4L} U_a^2. \tag{5}$$

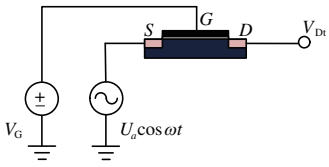

Figure 1 (Color online) Source-coupled NMOS transistor for THz detection.

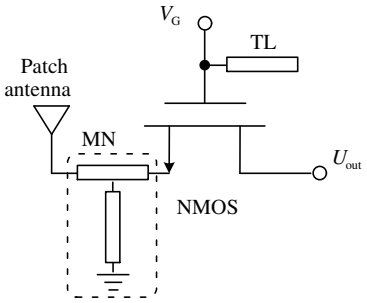

Figure 2 Architecture of the proposed source-driven detector.

There is a direct current (dc) term $\mu_n C_{\rm ox}\frac{W}{4L}U_a^2$ exiting between the drain and source. As the drain of the transistor is open, the drain voltage will decrease, which also makes the dc decrease (similar to a capacitor discharge). Assuming the dc is zero when the drain voltage is $V_{\rm Dt}$, the drain-source voltage can be changed to

$$V_{\rm DS}(t)_2 = V_{\rm Dt} - U_a\cos\omega t. \tag{6}$$

Combining (2)–(4) and (6), we get

$$\begin{aligned} i_{\rm DS}(t)_2 = {} & \mu_n C_{\rm ox}\frac{W}{L}(V_{\rm th} - V_G + V_{\rm Dt})U_a\cos\omega t + \mu_n C_{\rm ox}\frac{W}{4L}U_a^2\cos 2\omega t \\ & + \mu_n C_{\rm ox}\frac{W}{L}\left[\frac{1}{4}U_a^2 - \frac{1}{2}V_{\rm Dt}^2 + (V_{\rm G} - V_{\rm th})V_{\rm Dt}\right]. \end{aligned} \tag{7}$$

As the dc between the drain and source is zero when drain voltage is $V_{\rm Dt}$, we get

$$0 = \frac{1}{4}U_a^2 - \frac{1}{2}V_{\rm Dt}^2 + (V_{\rm G} - V_{\rm th})V_{\rm Dt}, \tag{8}$$

$$V_{\rm Dt} = (V_{\rm G} - V_{\rm th}) - \sqrt{(V_{\rm G} - V_{\rm th})^2 + \frac{1}{2}U_a^2}. \tag{9}$$

When $(V_{\rm G} - V_{\rm th}) >> U_a$,

$$\begin{aligned} V_{\rm Dt} &= (V_{\rm G} - V_{\rm th}) - (V_{\rm G} - V_{\rm th})\left[1 + \frac{U_a^2}{4(V_{\rm G} - V_{\rm th})}\right] \\ &= -\frac{U_a^2}{4(V_{\rm G} - V_{\rm th})}. \end{aligned} \tag{10}$$

This result is identical to that obtained with plasma wave theory [13], which shows that the drain dc voltage depends on the incident THz radiation power proportionally.

The above analyses indicate that the source-coupled non-biased FET can detect THz radiation far beyond its cut-off frequency, and the FET output is a dc voltage signal which depends on the incident THz radiation power proportionally.

3 Design of CMOS THz detector

The architecture of the proposed THz detector is shown in Figure 2. The detector consists of an on-chip patch antenna and a source-feeding NMOS transistor. The THz wave is received by the antenna and then coupled to the transistor. The gate of the transistor is biased to a dc potential of $V_{\rm G}$. A matching network MN is designed to improve the power transfer efficiency between the antenna and transistor. An open quarter-wavelength microstrip transmission line TL is proposed to eliminate the influence of the gate bias supply line on the antenna-transistor impedance matching. In addition, the MN provides a dc ground for the source. The channel length and width of the transistor are 0.35 μm and 1 μm, respectively. Compared to the gate-driven configuration proposed in [20], the source-driven detector herein can achieve broadband operation without any additional tuning elements [18].

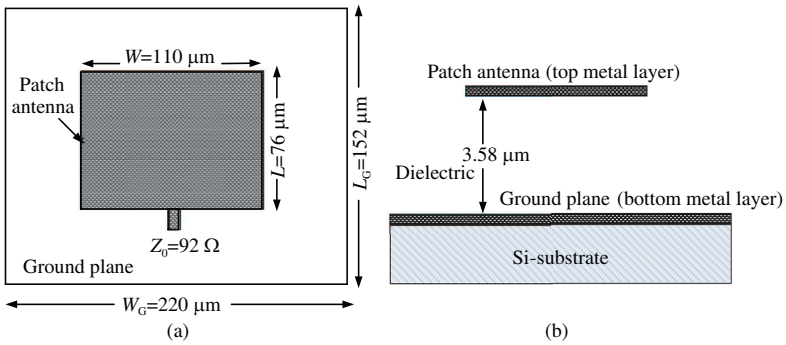

Figure 3 (a) Top and (b) cross-sectional views of the patch antenna.

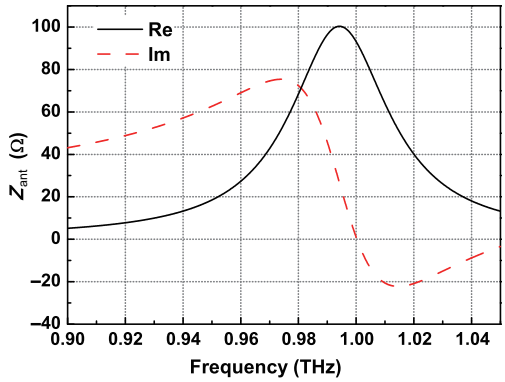

Figure 4 (Color online) Impedance of the patch antenna versus frequency.

3.1 Patch antenna

The detector has an integrated half-wavelength patch antenna, the structure of which is shown in Figure 3. The patch is formed by the top metal layer in the process, the length and width of which are L = 76 μm and W = 110 μm, respectively. The bottom metal layer is utilized to form the ground plane, which eliminates the back lobe and prevents substrate waves from the bulk [20]. The thickness of the dielectric insulator between the patch and ground is 3.58 μm. The antenna performance is simulated with the 3-D electromagnetic solver package HFSS. The impedance of the antenna versus frequency at the feeding point is shown in Figure 4. The simulated resonant frequency and resonant impedance are 1 THz and 92 Ω, respectively.

3.2 Matching network

To improve power transfer efficiency, we propose a short-stub matching network MN inserted between the antenna and transistor utilizing microstrip transmission lines. The structure of MN is shown in Figure 5. It consists of two transmission lines L_1 and L_2. MN is implemented in the top metal layer using the bottom metal layer as the ground plane. Because the transistor requires a dc path, we ground the end of L_2 to provide a dc ground for the source. Compared to [18] which requires an extra bias line connecting the antenna to provide an NMOS gate-source bias, the proposed MN does not require an extra bias line through the antenna, mitigating the system-level complexity for future array implementation.

To design MN, the simulated or measured input impedance Z_m of the transistor should be known. We use the Synopsys TCAD simulator to extract Z_m [21]. Figure 6 shows the simulated 2-D NMOS transistor. The different colors represent different ion doping concentrations. All processing steps such as etching, deposition, ion implantation, thermal annealing, and oxidation were considered. Synopsys TCAD can perform the ac analysis simulation for NMOS [21], which can be used to deduce Z_m. We extracted Z_m at 1 THz using the transistor. Figure 7 shows Z_m as a function of V_G. Both the real

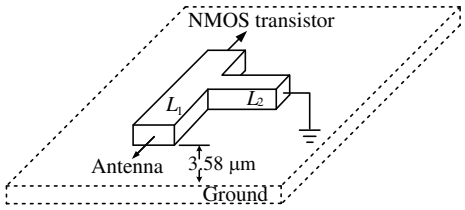

Figure 5 Structure of the short-stub matching network MN.

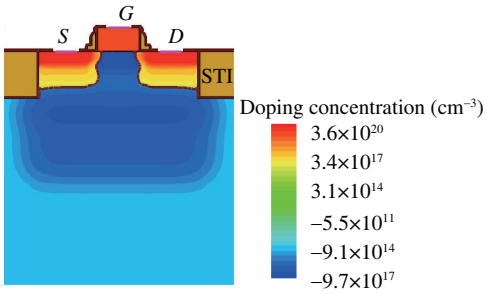

Figure 6 (Color online) Simulation result of the 2-D NMOS transistor. The different colors represent different ion doping concentrations. The shallow trench isolation (STI) process is considered in the simulation. The letters *S*, *G*, *D* denote the source, gate and drain.

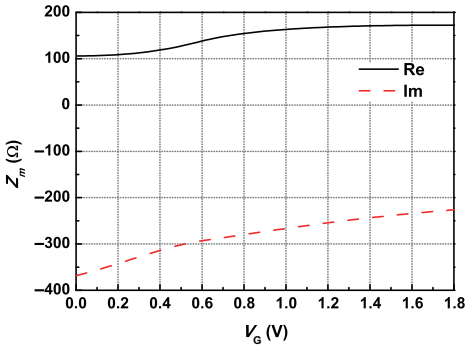

Figure 7 (Color online) Input impedance of the NMOS transistor as a function of gate bias voltage.

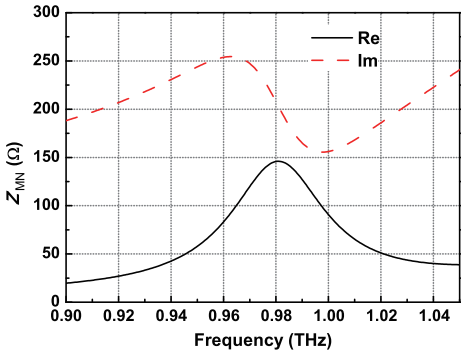

Figure 8 (Color online) Simulated impedance of the antenna with MN versus frequency.

and imaginary parts of the input impedance change slowly with increasing $V_{\rm G}$. We choose $Z_m = (118-{\rm j}280)\ \Omega$ as the impedance for the MN design. With the impedances of the antenna and NMOS transistor obtained, MN can be designed properly.

The matching coefficient $M_{\rm C}$, defined as the ratio of the accepted power by the NMOS transistor and incident power from the antenna, can characterize whether satisfactory matching is achieved. Mathematically,

$$\begin{aligned} M_{\rm C} &= \frac{P_{\rm acc}}{P_{\rm inc}} = \frac{{\rm Re}(Z_m)}{|Z_m + Z_{\rm MN}|^2} \Big/ \frac{1}{4{\rm Re}(Z_{\rm MN})} \\ &= 4{\rm Re}(Z_m){\rm Re}(Z_{\rm MN})/|Z_m + Z_{\rm MN}|^2\ , \end{aligned} \tag{11}$$

where $Z_{\rm MN}$ is the impedance of the antenna together with MN. If there is no MN, $M_{\rm C} = 0.35$.

As the antenna resonant impedance is 92 Ω, the characteristic impedance of MN can be selected as 92 Ω so that it can match the antenna port well. Characteristic impedance determines the width of transmission lines. The simulated width is 1.98 μm. The optimal lengths of L_1 and L_2 are 32.5 μm and 7.42 μm, respectively. The distance between L_2 and the antenna is 5.22 μm. Conjugate matching between the antenna and FET can be achieved using MN, which is the condition of maximum power transfer. Figure 8 shows the simulated impedance of the antenna with MN versus frequency. The impedance is $Z_{\rm MN} = (129+{\rm j}280)\ \Omega$ at 1 THz and the calculated $M_{\rm C} = 0.99$. This indicates that the antenna-transistor impedance matching is achieved well at this frequency. The simulated peak directivity and gain of the antenna with MN at 1 THz are 6.9 dBi and 3.0 dBi, respectively, for a radiation efficiency of 40.9%. The effective area $A_{\rm eff}$ of this patch antenna is 0.035 mm^2, which can be calculated using [22]

$$A_{\rm eff} = D\frac{\lambda^2}{4\pi}, \tag{12}$$

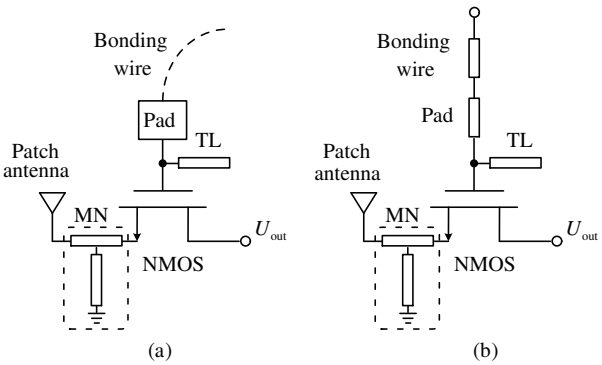

Figure 9 (a) Schematic and (b) equivalent model of the detector with banding wire and pad.

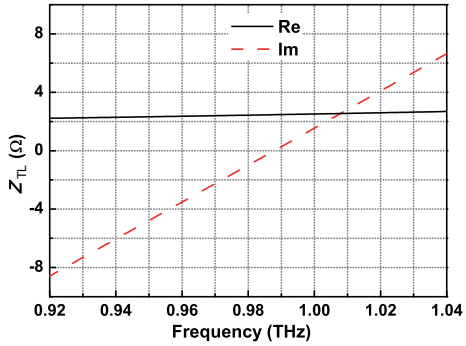

Figure 10 (Color online) Simulated impedance of TL as a function of frequency.

where D is the directivity of the antenna and λ is the electromagnetic wavelength.

3.3 Open quarter-wavelength microstrip transmission line

The gate of the transistor should be biased to a constant potential; it was normally biased directly by an off-chip voltage supply through the bonding wire and pad, as shown in Figure 9(a). For THz frequencies, the pad and bonding wire should be considered transmission lines. The equivalent model is shown in Figure 9(b). As a result of this, the pad and bonding wire will influence the antenna-transistor impedance matching. We propose an open quarter-wavelength microstrip transmission line TL (33 μm× 1.98 μm) to eliminate this influence. One end of TL is connected to the gate and the other is floating. Thus, it forms an ac ground at the corresponding THz frequency [23] and has no impact on the dc bias. TL is also implemented in the top metal layer, and the bottom metal layer is utilized to form the ground plane. Figure 10 shows its simulated impedance. Both the real and imaginary parts are close to 0 Ω around 1 THz. This result indicates that the gate forms an ac ground at 1 THz so that the influence of the bonding wire and pad is eliminated.

4 Measurement results and discussion

4.1 Measurement results

The detector is fabricated using a 180-nm CMOS process. Figure 11(a) shows its die photo. The proposed detector is displayed on the left, which is characterized using the lock-in technique. Figure 11(b) illustrates the measurement setup. A mechanical chopper with a frequency of 377 Hz modulates a BWO source, and at the same time, generates a TTL signal as the reference signal for the lock-in amplifier. The THz radiation is collimated and refocused into the detector by two parabolic mirrors. The output signal of the detector is amplified by a 40-dB low noise amplifier (LNA). The lock-in amplifier is used to capture the amplified signal.

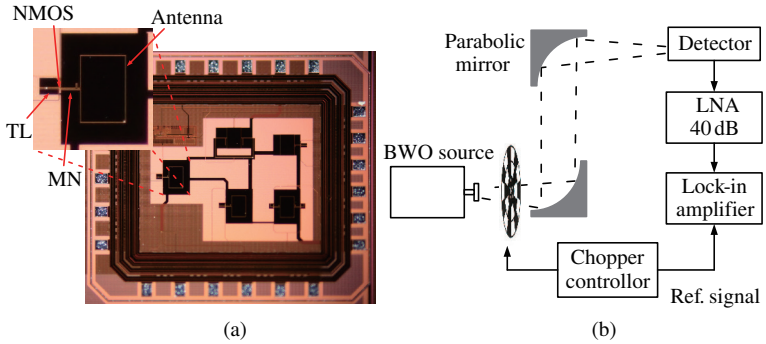

Figure 11 (Color online) (a) Die photo of CMOS THz detector and (b) measurement setup for characterizing the detector.

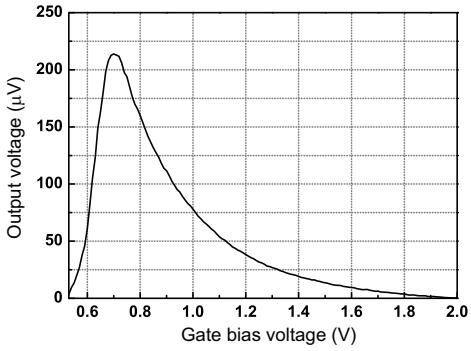

Figure 12 Measured output voltage as a function of gate bias voltage.

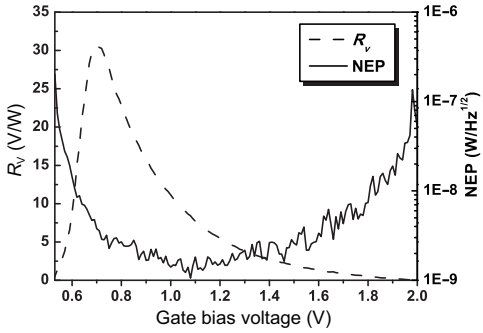

Figure 13 Measured $R_{\rm v}$ and NEP as a function of gate bias voltage.

We must point out that the resonant frequency of this antenna is designed at 1 THz [24], while the BWO source used for testing emits a very low power at this frequency. Therefore, we selected a test frequency of 0.94 THz. At 0.94 THz, the simulated peak directivity and gain of the antenna with MN are 6.93 dBi and −0.26 dBi, respectively, for the antenna efficiency of 21.9%. The effective area $A_{\rm eff}$ is 0.035 mm^2 according to (12).

Figure 12 shows the measured output voltage of the detector with a 40-dB gain. The peak voltage is 214 μV when $V_{\rm G}$ is 0.69 V. The voltage responsivity $R_{\rm v}$ is defined as the ratio between the output voltage of the detector and the power incident on the antenna. Because the THz radiation is modulated by a square wave with a 50% duty cycle, the measured voltage by the lock-in amplifier is the root-mean-square (rms) value of the fundamental frequency component [17]. Based on Fourier analysis,

$$R_{\rm v} = \frac{\frac{\pi}{\sqrt{2}}U_{\rm out}}{G_{\rm LNA}P_{\rm in}} = \frac{\frac{\pi}{\sqrt{2}}U_{\rm out}}{G_{\rm LNA}J_{\rm in}A_{\rm eff}}, \tag{13}$$

where $U_{\rm out}$ is the measured output voltage, $G_{\rm LNA}$ is the gain of LNA and $J_{\rm in}$ is the THz radiation power density incident on the antenna.

The values of $J_{\rm in}$ and $G_{\rm LNA}$ are 4.4 μW/mm^2 and 40 dB, respectively. According to (13), $R_{\rm v}$ versus $V_{\rm G}$ is calculated and plotted in Figure 13. The peak $R_{\rm v}$ is 31 V/W when $V_{\rm G}$ is 0.69 V.

NEP is defined as the input power that results in a signal-to-noise ratio of 1 in a 1-Hz bandwidth [17]. Mathematically, it is the ratio between the output noise voltage spectral density and the detector $R_{\rm v}$. The NEP under different gate-bias conditions at a 377-Hz modulation frequency is also plotted in Figure 13. The minimum NEP is 1.1 nW/Hz$^{1/2}$ when $V_{\rm G}$ is 1.08 V. When $V_{\rm G}$ is 0.69 V, NEP is 4.8 nW/Hz$^{1/2}$.

4.2 Discussion

As mentioned above, the detector is designed at 1 THz whereas the measurement frequency is 0.94 THz. Based on the simulation results, the electromagnetic performance of the antenna (with matching network)

Table 1 Summary of detector performance and comparison with prior work

Freq. (THz)	Technology	R_v (V/W)	NEP (nW/Hz$^{1/2}$)	Optics	Ref.
0.94	180-nm CMOS	31	1.1	–	This work
0.28	130-nm CMOSB (SBD)	250	0.033	–	[17]
0.60	250-nm CMOS	50k	0.4	–	[25]$^+$
0.65	250-nm CMOS	80k	0.3	–	[20]$^+$
0.6–1	65-nm CMOS	800@1 THz	0.066@1 THz	Si lens	[15]
0.65	65-nm SOI CMOS	1.1k	0.05	Si lens	[26]
0.7–1.1	65-nm CMOS	140k@0.86 THz	0.1@0.86 THz	Si lens	[16]$^+$
0.2–30	Golay Cell	0.1k–45k	0.2–0.4	–	[27]

Note:$^+$with amplifier.

at 1 THz is better than that at 0.94 THz. Besides, the antenna and transistor achieved a much better impedance matching at 1 THz. Therefore, we conclude that this detector would reach a much higher R_v and lower NEP at 1 THz than at 0.94 THz.

5 Conclusion

This paper proposes and implements a THz detector in a 180-nm standard CMOS process. The detector consists of an on-chip patch antenna and an NMOS transistor. A novel short-stub matching network is proposed to improve the power transfer efficiency. A design method adopting tools from TCAD is presented. An open quarter-wavelength microstrip transmission line is proposed to eliminate the influence of the gate bias supply line. Measurement results show that the detector achieves a voltage responsivity of 31 V/W and an NEP of 1.1 nW/Hz$^{1/2}$ at room temperature. It is implied that the proposed detector can be further used in a multi-pixel array for THz imaging. The performance of the detector is summarized and compared to that of other published THz detectors in Table 1.

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Conflict of interest The authors declare that they have no conflict of interest.

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