Wireless Personal Communications (2023) 131:2675–2696
https://doi.org/10.1007/s11277-023-10566-2

A Fractional-Order Meminductor Emulator Using OTA and CDBA with Application in Adaptive Learning Circuit

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Accepted: 8 June 2023 / Published online: 30 June 2023
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Abstract
In this paper, a new memristor-less fractional-order meminductor emulator has been presented based on two operational transconductance amplifiers (OTAs), and a current differencing buffered amplifier (CDBA). The integer and fractional capacitors have been utilized in the proposed design of floating and grounded types. It also offers the freedom of conversion between incremental and decremental in both the types i.e., grounded, and floating. The pinched hysteresis loops have been obtained up to 3 MHz for both incremental and decremental setups of the proposed fractional-order meminductor emulator. The simulation results were achieved using the LTSpice tool with 180 nm CMOS technology specifications. The suggested meminductor emulator's performance has also been compared to that of existing emulators reported in the literature. To test the effectiveness of the suggested fractional-order meminductor emulator, an adaptive learning circuit has been simulated.

Keywords Memristor · Meminductor · OTA · CDBA · Fractional · Adaptive learning circuit

1 Introduction

The theory of arbitrary order, real or complex, integrations, and derivatives is known as fractional calculus, and it generalizes the traditional notations for differentiation and integration. It's an extremely handy mathematical tool that was obscured and used very less, but, by the 1980s it was realized that fractional calculus translates the reality of nature better since it has more flexibility in differential order. This feature offers us a language through which we can communicate with nature. Recent years have seen the use of

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fractional calculus in a variety of disciplines, including engineering, material theory, biology, diffusion theory, economics, electromagnetic, control theory, robotics, signal, and image processing [1]. Fractional-order capacitors, also referred to as constant phase elements (CPEs), are becoming increasingly important in a wide range of applications where C_α stands for pseudo-capacitance and for order, also known as the dispersion coefficient. It offers an impedance of $1/C_\alpha s_\alpha$ and a constant phase angle of $-\alpha\pi/2$. The effective manufacturing of this device has recently been investigated by utilizing several materials. A few examples of the many methods used to create CPEs include the usage of graphene most recently in [7], fractal patterns on silicon [2], electrolytic process [3], submerging a polymer-coated capacitive type probe inside a polarizable solution [4–6], and electrolytic technique. All of these options, however, are commercially unavailable and lack the benefit of dynamic customization. Passive RC trees are now being used to simulate CPEs, for which the components may be produced using a variety of approaches, including continuing fraction expansion [8–11]. The Foster form is used to implement the circuit, which uses 5 resistors and 4 capacitors, and the fractional capacitor utilized in this study has been approximated by using continued fraction expansion (CFE) up to the fourth order [12]. The fractional element is halfway between a capacitor and a resistor, as we have a resistor at $\alpha = 0$ and a capacitor at $\alpha = 1$. The ideal CPE has a constant phase at all frequencies, but in practice, the phase is only constant over a small frequency range, which is referred to as the constant phase zone (CPZ). Because the phase oscillates somewhat even within the CPZ, actually realized CPEs are occasionally referred to as pseudo-CPEs. One of the key factors influencing interest in fractional calculus in applications is the nonlocality trait. Several intriguing physical phenomena have what are known as memory effects, which means that their current state depends not only on time and position but also on past states. For instance, in 1971, Professor Chua envisioned one such passive device. The circuit elements signify the relationship between pairs of the 4 electromagnetic entities of voltage, flux, charge, and current as shown in Fig. 1. The resistor relates voltage (v) with current (i) whereas the capacitor signifies the relationship between voltage (v) and charge (q). The inductor on the other hand relates the electromagnetic quantities of flux (ϕ) and current (i). However, the relationship between flux (ϕ) and charge (q) was not represented by any device. Therefore, in 1971, Professor Chua envisioned one such passive device. He postulated the existence of the memristor [13], a fourth essential circuit component that links flux and charge and whose resistance is determined by the total amount of charge that has travelled through it over a specific time period. He discussed the generalized concept of the memristor in 1976 [14]. But it was only after 2008, when, in HP-lab, Mr. Williams with his team realized the first memristor in physical form using TiO_2, which drew the attention of many researchers towards this novel element [15]. It can be extremely difficult to describe and analyze systems with memory effects, such as the memristor, using conventional differential equations. Yet, nonlocality provides fractional derivatives with an inherent ability to include memory effects. Thus, fractional calculus may be a highly helpful technique for analysing this family of systems [16].

Following the successful implementation of the memristor, quick development occurred, and the concept was expanded to include inductors and capacitors having memories inside them, which resulted in two other components namely the meminductor and memcapacitor [17].

However, due to the unavailability of commercially available memelements, scholars began to realize various emulators in order to combat this issue. By extensive literature review, it was realized that there are two ways in which meminductance has been realized. Firstly, various emulators were designed to convert memristors into meminductors and

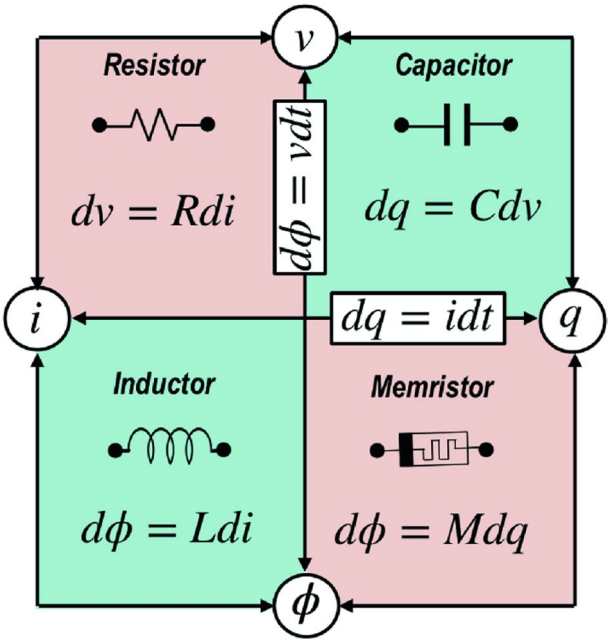


Fig. 1 Relation between circuit elements [8]

memcapacitors using mutator circuits [17, 18]. In [19–22] memristors have been converted to memcapacitor and meminductors using operational amplifiers, current conveyors, resistors, and capacitors. Meminductors have also been made using memristors, trans-impedance op amps, multipliers, and a few resistors and capacitors [23–25]. The SPICE model to convert memristor into meminductor has been given in [26]. The disadvantage of this strategy is that the characteristics of the developed meminductor emulator are heavily reliant on the memristor emulator's features. The alternative method is to make meminductor emulators without using memristors. The meminductors using this method do not use memristors but various active and passive building blocks are employed instead. VDTAs, CDBAs, and capacitors have been used to create high-frequency memristor-less meminductor emulators [27, 28]. Multipliers, current conveyors, op-amps, and OTAs along with resistors and capacitors have been used to realize memristor-less meminductors [21, 29–33]. These meminductor emulators use a lot of active and passive components, which makes the circuit very complex and error prone.

The above-discussed meminductor and memcapacitor emulators realize integer-order emulators and provide less flexibility in terms of regulating various parameters when used in a variety of applications. As depicted in Fig. 2, the pinched hysteresis loops develop between current (i) and flux (ϕ) for the meminductor and between voltage (v) as well as charge (q) for the memcapacitor. To create varied applications and to better handle the numerous circuit parameters, fine control over the pinched hysteresis curves is required.

The researchers faced this dilemma and therefore they turned to the field of fractional order devices in order to find a solution. A lot of research has been carried out over fractional-order memristors, which yielded some promising results in finely controlling the various parameters of the circuit [34–41] but since the concept of meminductors and memcapacitors is relatively new, therefore equal emphasis has not been given to fractional-order meminductor (FOMI) and memcapacitor (FOMC). Abdelouahab *et* al. in [42] presents the

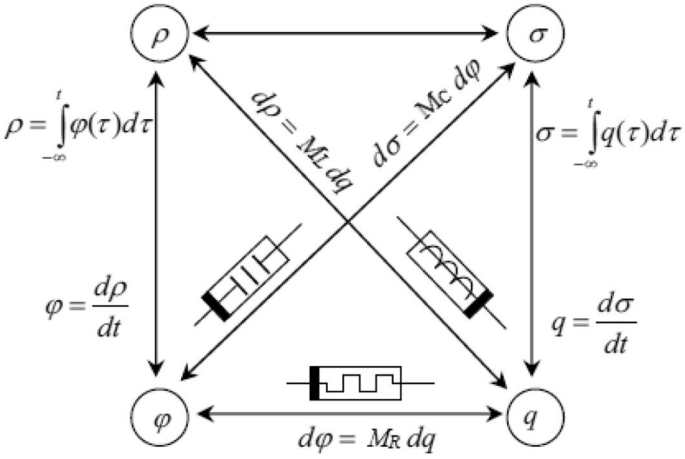


Fig. 2 The relation between mem elements [17]

mathematical model of fractional-order mem elements. Few papers have been reported on the fractional-order meminductor and memcapacitor emulators. Four new fractional-order circuits have been proposed in [43] that contain fractional-order memristor, memcapacitor and meminductor. These fractional-order memristive, memcapacitive, and meminductive systems (FOMMMSs) exhibit a wide range of behaviours. In [44], the fractal-fractional-order domain of Caputo-Fabrizio is used to examine the dynamical properties of memcapacitor and meminductor. Fractional order memelements have been designed in [45] and their application in an analogue controller has been discussed. A general emulator circuit for fractional-order memelements has been realized in [46] using a multiplier, current conveyors, capacitors and resistors, and multiple pinched points have been obtained. Four universal fractional-order memelements emulators have been proposed in [47] using CCII, DVCC and analogue multiplier, DOTA+, BOCC. These emulators have been used to create a chaotic oscillator that demonstrates their capabilities. In [48], a fractional-order current-controlled meminductor model with a nonlinear window function is investigated, and the amplitude-frequency response properties of the meminductor under various excitation signals are analysed in depth. In [49], various arrangements of memristor, fractional-order capacitor, and resistor were employed to achieve fractional-order meminductor and memcapacitor. It has been demonstrated how the pinched point and the hysteresis loop area fluctuate with changes in α and frequency. The effect of change in α has been observed in [50] on floating fractional-order memelements realized using memristor and current conveyors. Different implementations of the emulator have been proposed using different active blocks and impedances. A current/voltage controlled universal emulator realized using two switches, a CCII block, a multiplier and a fractional order capacitor has been featured in [51]. In order to realize a fractional-order meminductor emulator circuit, a fractional-order capacitor that was constructed using the CFE method and Foster-I method is used. With the aid of two OTAs and a CDBA, the meminductor emulator has been realized. It is shown that the fractional-order meminductor emulator performs better than an integral-order meminductor emulator in terms of frequency responsiveness. In comparison to existing FOMI realisations described in the literature, the suggested fractional-order meminductor emulator has a lot simpler architecture and a much better frequency response.

The introduction is the first of this paper's seven sections. In Sect. 2, the characteristics of OTA and CDBA are described. In Sect. 3, the proposed grounded and floating fractional-order meminductor emulator's mathematical analysis is described. The simulation outcomes for grounded/floating configurations using the suggested fractional-order meminductor emulator are displayed in Sect. 4. In Sect. 5, the suggested fractional meminductor emulator is contrasted with current meminductor emulators. Section 6 discusses the use of the suggested meminductor emulators, and Sect. 7 provides the conclusions.

2 Characteristics of Voltage-Tunable OTA and CDBA

Figure 3 depicts the operational transconductance amplifier (OTA) symbol, which is voltage-tunable. It contains five terminals, including two input terminals (+ and −), two output terminals (+ and −), and a fifth terminal (V_B) for regulating the OTA's transconductance gain (g_m). Due to their extremely high input impedance, the two input terminals drain essentially no current as indicated by Eq. (1). When applied to the two high impedance input terminals of the OTA, "+" and "-," a differential voltage (V_{in+}—V_{in-}) results. This voltage is then converted to current (I_{x+} and I_{x-}) at the output terminals "X", where the transconductance gain "g_m" of the OTA depends on the bias voltage V_B as given in Eq. 5. Figure 4 illustrates the CMOS implementation of an OTA [53].

$$I_P = I_N = 0 \tag{1}$$

$$I_{X\pm} = \pm G_m\left(V_{in+} - V_{in-}\right) \tag{2}$$

$$G_m = \frac{K}{\sqrt{2}}\left(V_B - V_{ss} - 2V_{th}\right) \tag{3}$$

where,

$$K = \mu_n C_{ox}\left(\frac{w}{L}\right) \tag{4}$$

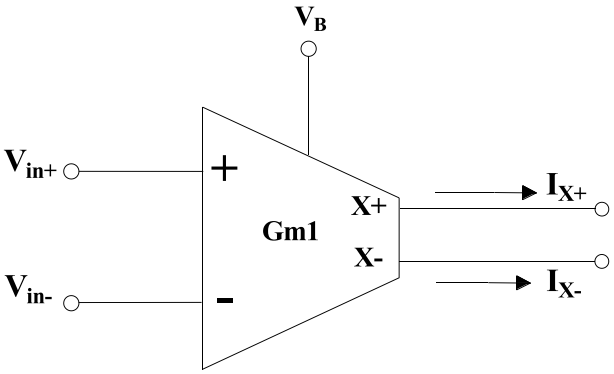


Fig. 3 Symbol of OTA

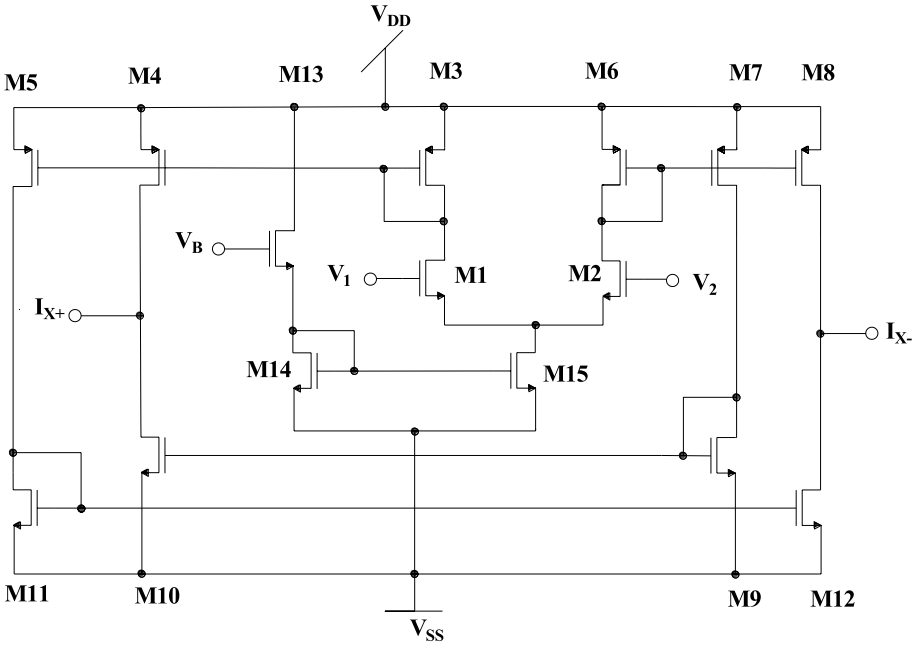
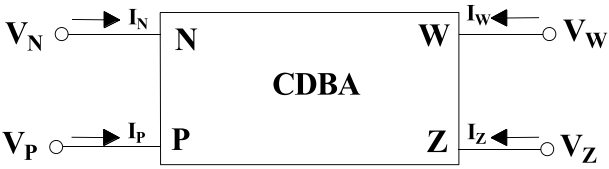


Fig. 4 CMOS based Circuit diagram of OTA [53]

A current differencing buffered amplifier (CDBA), first described in [54], is represented by its symbol in Fig. 5. It is a 4-terminal analog building block having two output terminals (Z and W) and two input terminals (P and N). To apply the two currents I_P and I_N, two input terminals with low input impedance are used. It is possible to measure the difference between these currents at the 'Z' terminal. The 'Z' terminal is given an impedance to change I_Z to V_Z. To terminal W, an internal buffer replicates the voltage V_Z. Equation 7 represents the terminal characteristics of a perfect CDBA. Figure 6 depicts CDBA's CMOS structure [55].

$$V_N = V_P = 0, I_Z = \left(I_P - I_N\right), V_W = V_Z \tag{5}$$

Fig. 5 Symbol of CDBA



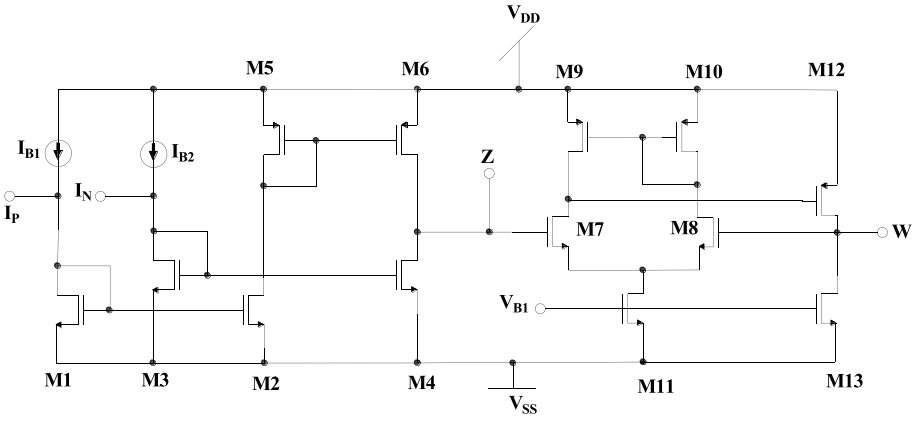


Fig. 6 Circuit diagram of CDBA [55]

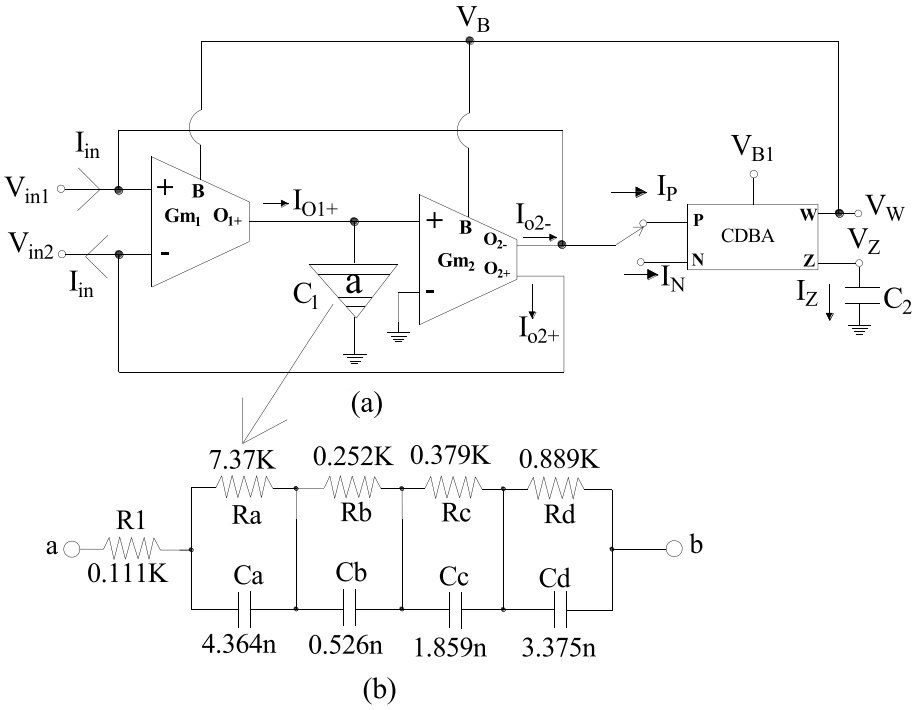


Fig. 7 **a** Proposed fractional meminductor emulator **b** RC realization of the fractional capacitor C1

3 Design of the Proposed Fractional-Order Meminductor Emulator

In this section, the working principle of proposed fractional-order meminductor emulator along with realization of fractional-capacitor used in the design have been covered.

3.1 The Proposed circuit

Two OTAs and a CDBA are used in the proposed design of the incremental and decremental fractional-order meminductor emulator presented in Fig. 7. The "+" and "-" terminals of OTA_1 accept the input voltage. The floating fractional-order meminductor emulator can be changed to a grounded fractional-order meminductor emulator by grounding the "-" terminal. The output of OTA_1, "O_1+", is connected to the fractional capacitor C_1. In the suggested design of the fractional meminductor emulator shown in Fig. 7a, the output terminals "O_{2-}" and "O_{2+}" of the second OTA (OTA_2) are connected to the input terminals "+" and "-" of the first OTA (OTA_1), respectively. The terminal "O_{2-}" of OTA_2 can be connected to terminal "P" or "N" of the CDBA in order to realize incremental or decremental meminductor emulators. By transferring the input current ($I_P = I_{02-} + I_{in}$ or $I_N = I_{O2-} + I_{in}$) to the "Z" terminal, the capacitor C_2 gets charged by CDBA. The transconductance (g_m) of the OTAs is controlled to control the value of meminductance by transferring the voltage (V_Z) to the CDBA's "W" terminal, which is connected to the OTA's V_B terminal. A meminductor emulator is thus realized by adjusting the value of meminductance in accordance with the circuit's historical data (charge stored in C_2).

The mathematical analysis of proposed fractional-order incremental meminductor emulator is presented below.:

$$I_{01+} = G_{m1}\left(V_{in1} - V_{in2}\right) \tag{6}$$

$$V_{01} = \frac{1}{s^{\alpha}C_1} \times I_1 \tag{7}$$

where, $\phi_{in}^{\alpha} = \frac{V_{in}}{s^{\alpha}} = \int V_{in} d^{\alpha}t$.

This is a fractional-order integral equation, which can be calculated by using the methods of [56] and [57]. Therefore, Eq. (7) can be written as:

$$V_{01} = \frac{1}{s^{\alpha}C_1} \times G_{m1}V_{in} = \frac{G_{m1}}{C_1} \times \phi_{in}^{\alpha}(t) \tag{8}$$

$$I_{02-} = -G_{m2}V_{01} \tag{9}$$

As seen in Fig. 7, the terminal "O_{2-}" is shorted to the CDBA's "P" terminal. The current I_z can therefore be expressed as,

$$I_Z = I_P = I_{in} + I_{O2-} \tag{10}$$

The CDBA's "Z" terminal will then have a voltage V_Z,

$$\mathrm{Vz} = \frac{1}{\mathrm{C}_2}\int \mathrm{Izdt} = \frac{1}{\mathrm{C}_2}\int \left(\mathrm{I}_{O2-} + I_{in}\right)\mathrm{dt} \tag{11}$$

Replacing the values of the current 'V_{01-}' and 'I_{O2}' from Eq. (8) and (9), respectively,

$$V_z = \frac{1}{C_2}\int \left(-G_{m2}V_{01} + I_{in}\right)\mathrm{d}t = \frac{1}{C_2}\int \left(\frac{-G_{m2}G_{m1}}{C_1}\phi_{in}^{\alpha} + I_{in}\right)\mathrm{d}t \tag{12}$$

Taking $\int \phi_{in}^{\alpha} dt = \frac{\phi_{in}^{\alpha}}{s^{\alpha+1}} = \rho^{\alpha}$ and $\int I_{in} dt = q(t)$

$$V_z = V_w = V_B = \frac{-G_{m1}G_{m2}}{C_1C_2}\rho^{\alpha} + \frac{q(t)}{C_2} \tag{13}$$

The voltage V_Z is transferred to CDBA's 'W' terminal, which is coupled to the OTAs' 'V_B' terminal.

Since, $G_{m1} = \frac{K_1}{\sqrt{2}}\left(V_B - V_{ss} - 2V_{th}\right)$, Therefore, replacing the value of 'V_B' from Eq. 15 in G_{m1}

$$G_{m1} = \frac{K}{\sqrt{2}}\left(\frac{-G_{m1}G_{m2}}{C_1C_2}\rho^{\alpha} + \frac{q(t)}{C_2} - V_{ss} - 2V_{th}\right) \tag{14}$$

With the help of Eq. (8) and (9), we get,

$$I_{02-} = -G_{m2}V_{01} = \frac{-G_{m2}G_{m1}}{C_1}\phi_{in}^{\alpha} \tag{15}$$

Using the value of G_{m1} from Eq. (14) in Eq. (15), we have,

$$I_{02-} = \frac{-G_{m2}}{C_1}\frac{K_1}{\sqrt{2}}\left(\frac{-G_{m1}G_{m2}}{C_1C_2}\rho^{\alpha} + \frac{q(t)}{C_2} - V_{ss} - 2V_{th}\right)\phi_{in}^{\alpha} \tag{16}$$

The relation among flux ϕ_{in}^{α}, current I(t) and meminductance (M_L) is given by.

$$\phi_{in}^{\alpha} = M_L I(t) \tag{17}$$

Equation 17 can be rearranged as,

$$I(t) = M_L^{-1}\phi_{in}^{\alpha} \tag{18}$$

Comparing Eq. (16) and (18), we get,

$$M_L^{-1} = \frac{-G_{m2}}{C_1}\frac{K_1}{\sqrt{2}}\left(\frac{-G_{m1}G_{m2}}{C_1C_2}\rho^{\alpha} + \frac{q(t)}{C_2} - V_{ss} - 2V_{th}\right) \tag{19}$$

$$M_L^{-1} = \frac{G_{m2}K_1}{\sqrt{2}C_1}\left(V_{ss} + 2V_{th}\right) + \frac{G_{m2}K_1}{\sqrt{2}C_1}\left(\frac{G_{m1}G_{m2}}{C_1C_2}\rho^{\alpha} - \frac{q(t)}{C_2}\right) \tag{20}$$

Connecting the terminal 'O_{2-}' with the 'N' terminal of the CDBA in Fig. 6, we obtain,

$$M_L^{-1} = \frac{-G_{m2}K_1}{\sqrt{2}C_1}\left(V_{ss} + 2V_{th}\right) - \frac{G_{m2}K_1}{\sqrt{2}C_1}\left(\frac{G_{m1}G_{m2}}{C_1C_2}\rho^{\alpha} - \frac{q(t)}{C_2}\right) \tag{21}$$

Therefore, the values of meminductance for decremental and incremental meminductance is obtained as,

$$M_L = \pm\frac{1}{\frac{-G_{m2}K_1}{\sqrt{2}C_1}\left(V_{ss} + 2V_{th}\right)} \pm \frac{1}{\frac{G_{m2}K_1}{\sqrt{2}C_1}\left(\frac{G_{m1}G_{m2}}{C_1C_2}\rho^{\alpha} - \frac{q(t)}{C_2}\right)} \tag{22}$$

According to Eq. (22), meminductance for incremental meminductor emulators tends to increase whereas meminductance for decremental meminductor emulators decreases.

By connecting the '-' terminal of 'OTA_1' to the ground or any other node, respectively, it can be demonstrated that the proposed fractional meminductor emulator may be used in both grounded and floating configurations without affecting its functionality.

3.2 The Fractional Capacitor

Although it is well known that there is no such thing as an ideal fractional capacitor, there have been several attempts to approximate them in order to use them in fractional order systems. In 1964, Carlson used the regular Newton process to derive the rational approximation of $s^{1/n}$ and applied it using the RC ladder network [52]. Similar to this, Matsuda sought to approximate the irrational function to a rational one in [58] fitting the original function in a group of points that were logarithmically separated from one another. In order to obtain a function and an approximation of the fractional order capacitor, additional approximation approaches and identification procedures are also provided in [58].

One of the most well-known and often employed methods for approximating a fractional order impedance is called continuous fraction expansion (CFE). According to [59], it is:

$$(1+x)^{\delta} = \cfrac{1}{1-\cfrac{\delta x}{1+\cfrac{(1+\delta)x}{2+\cfrac{(1-\delta)x}{3+\cfrac{(2+\delta)x}{2+\cfrac{(2-\delta)x}{5+\ldots}}}}}} \tag{23}$$

in order to get a fractional capacitor's impedance function of the order of 0.5. We approximate till the fourth order in Eq. (23) by changing x and δ to (s-1) and -0.5, respectively, and to obtain the impedance function of the capacitor as

$$s^{-0.5} = \frac{s^4 + 36s^3 + 126s^2 + 84s + 9}{9s^4 + 84s^3 + 126s^2 + 36s + 1} \tag{24}$$

This gives us the impedance function for a fractional capacitor with 1F capacitance working best at an angular frequency (ω) of 1 rad/s.

By replacing 's' by $\frac{s}{10^6}$, and dividing Eq. (24) by the desired capacitance i.e., 10^{-6}, we obtain the expression for a fractional capacitor (Eq. 25) with centre frequency as 10^6 and capacitance 1μF which has been used in the design of proposed fractional order meminductor.

$$\frac{1}{10^{-6}\left(\frac{s}{10^6}\right)^{0.5}} = \frac{1}{10^{-6}} \cdot \frac{\left(\frac{s}{10^6}\right)^4 + 36\left(\frac{s}{10^6}\right)^3 + 126\left(\frac{s}{10^6}\right)^2 + 84\left(\frac{s}{10^6}\right) + 9}{9\left(\frac{s}{10^6}\right)^4 + 84\left(\frac{s}{10^6}\right)^3 + 126\left(\frac{s}{10^6}\right)^2 + 36\left(\frac{s}{10^6}\right) + 1} \tag{25}$$

Finding the roots and converting into partial fraction expansion form, we obtain:

$$\begin{aligned} &10^6 . \frac{\left(\frac{s}{10^6}\right)^4 + 36\left(\frac{s}{10^6}\right)^3 + 126\left(\frac{s}{10^6}\right)^2 + 84\left(\frac{s}{10^6}\right) + 9}{9\left(\frac{s}{10^6}\right)^4 + 84\left(\frac{s}{10^6}\right)^3 + 126\left(\frac{s}{10^6}\right)^2 + 36\left(\frac{s}{10^6}\right) + 1} \\ &= \frac{10^3}{9}\left(1 + \frac{A_1}{x+7.55} + \frac{A_2}{x+1.42} + \frac{A_3}{x+0.33} + \frac{A_4}{x+0.31}\right) \end{aligned} \tag{26}$$

Table 1 Aspect ratios of OTA and CDBA

CDBA		OTA	
MOS transistors	W/L (μm)	MOS Transistors	W/L (μm)
M1, M2, M3, M4	32/2	M1, M2	16/1
M5, M6	42.5/0.36	M3, M4, M5, M6, M7, M8	9/1
M7, M8	0.8/0.5	M9, M10, M11, M12	4/1
M9, M12, M13	10/0.5	M13	15/0.36
M10, M11	4/0.5	M14, M15	14/0.36

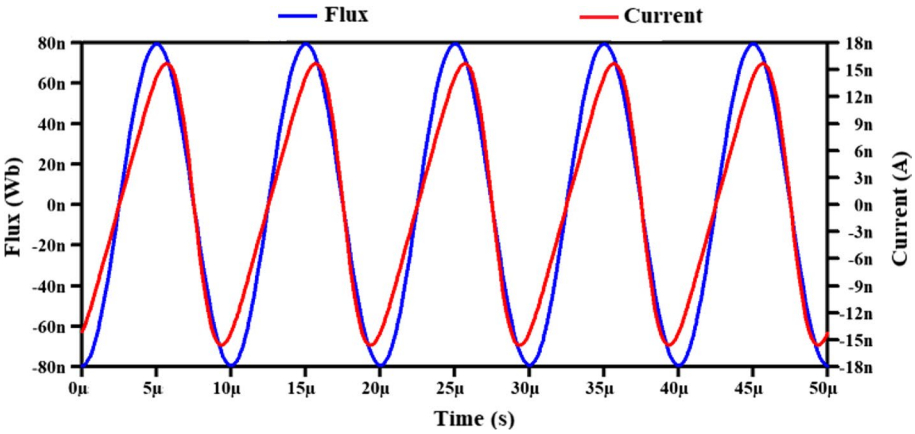


Fig. 8 Transient analysis of the proposed fractional meminductor

Now, by solving this partial fraction and using the foster analysis, we know that we need 5 resistors and 4 capacitors with values as given in Fig. 7b.

4 Simulation Results

Using 180 nm CMOS technology characteristics, the suggested meminductor emulator was simulated using the LTSpice simulator. A 0.9 V supply is used to power the suggested circuit. The bias voltage (V_B) of the CDBA is set to -0.1 V, and the bias currents are $I_{B1} = I_{B2} = 20\mu A$. Capacitor C_2 is calibrated to 40pF. In Table 1 below, the aspect ratios utilised to create the OTAs and CDBA are listed.

4.1 Transient Analysis

An input sinusoidal signal with 100 mV amplitude and 100 kHz frequency was used to perform the transient analysis of the proposed decremental fractional-order meminductor emulator. Figure 8 depicts the transient waveforms for flux and current.

To produce the pinched hysteresis loop (PHL) for the proposed fractional-order meminductor emulator, a sinusoidal signal with amplitude 100 mV in a frequency range of

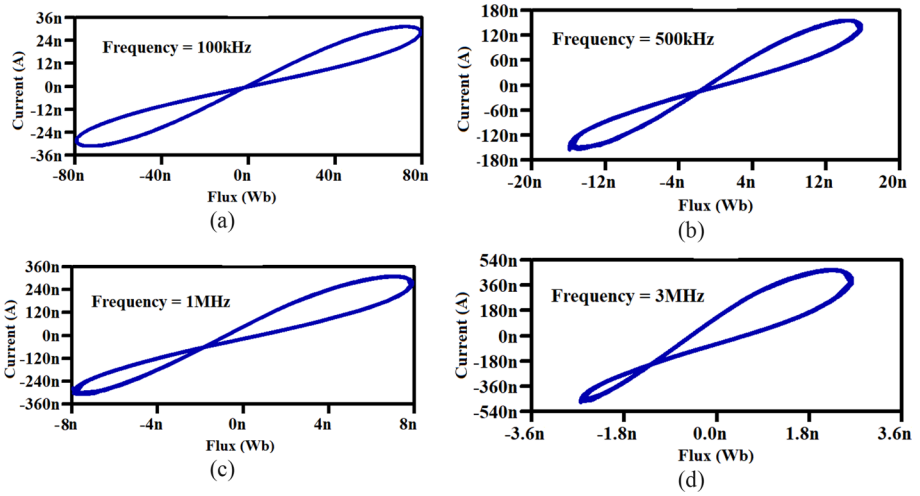


Fig. 9 PHLs of proposed decremental Fractional order meminductor at different frequencies **a** 100 kHz **b** 500 kHz **c** 1 MHz **d** 3 MHz

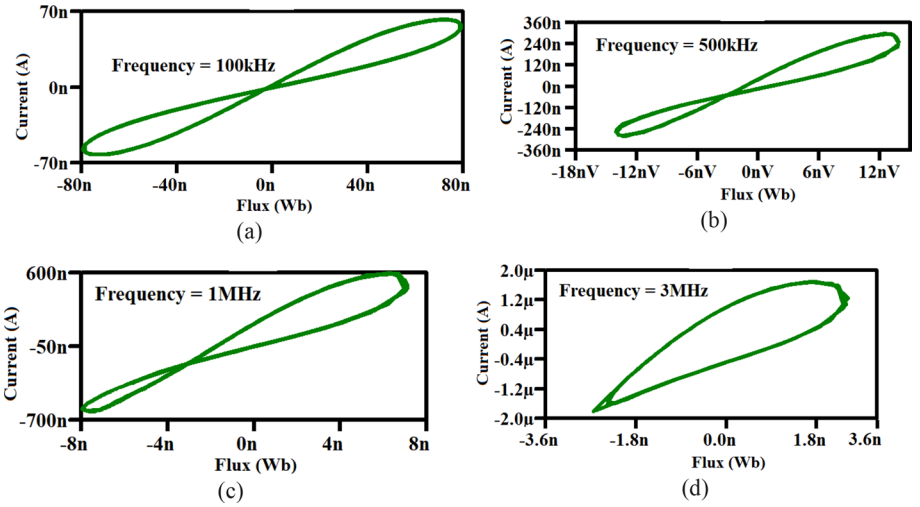


Fig. 10 PHLs of decremental integral order meminductor at different frequencies **a** 100 kHz **b** 500 kHz **c** 1 MHz **d** 3 MHz

100 kHz to 3 MHz was used. The resultant PHL's area diminishes on increasing frequency, as illustrated in Fig. 9. Observing the values of flux (ϕ) on the x-axis of Fig. 9 can confirm this decrease in the hysteresis loop area. The hysteresis loop can last up to 3 MHz, but the pinched point shifts from the origin. As a result, for frequencies greater than 3 MHz, the loop deforms. The pinched hysteresis curves for integer-order decremental meminductor emulator have also been obtained in Fig. 10 but the pinched hysteresis loop deform much earlier as compared to fractional-order meminductor emulator.

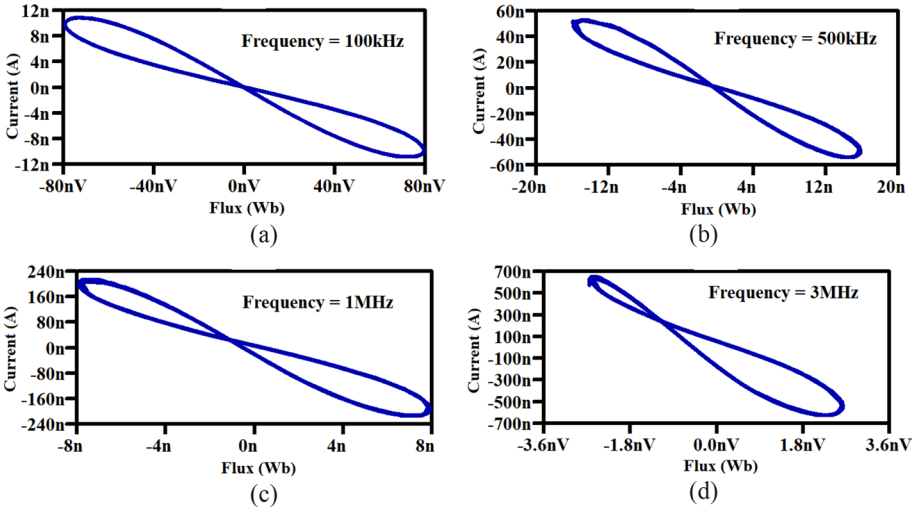


Fig. 11 PHLs of incremental fractional order meminductor emulator at different frequencies **a** 100 kHz **b** 500 kHz **c** 1 MHz **d** 3 MHz

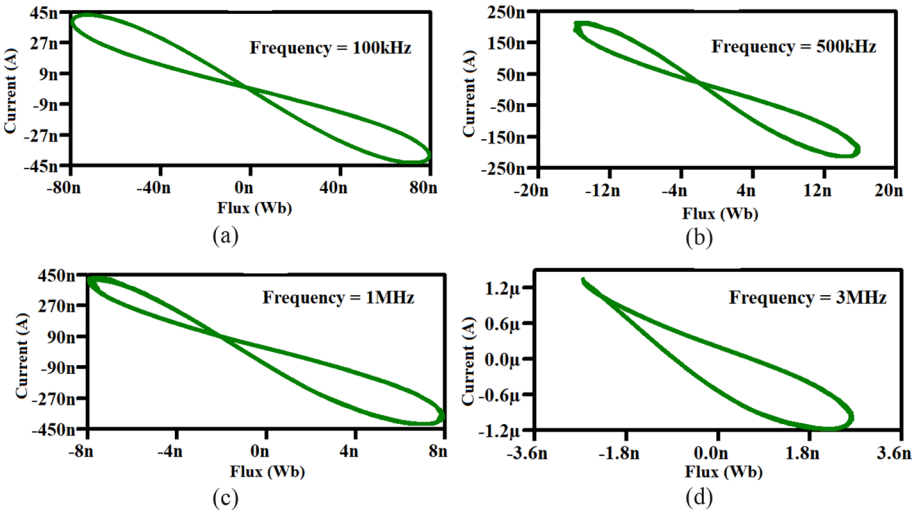


Fig. 12 PHLs of incremental Integer-order meminductor emulator at different frequencies **a** 100 kHz **b** 500 kHz **c** 1 MHz **d** 3 MHz

In Fig. 11, the PHLs of the proposed incremental fractional meminductor emulator are exhibited for frequencies between 100 kHz and 3 MHz. The pinched hysteresis loops for integer-order incremental meminductor emulator have also been obtained in Fig. 12 but the pinched hysteresis loop also deform much earlier as compared to fractional-order meminductor emulator.

The temperature analysis was carried on a sinusoidal signal with 100 mV amplitude and frequency of 100 kHz, to assess the functioning of the proposed decremental/

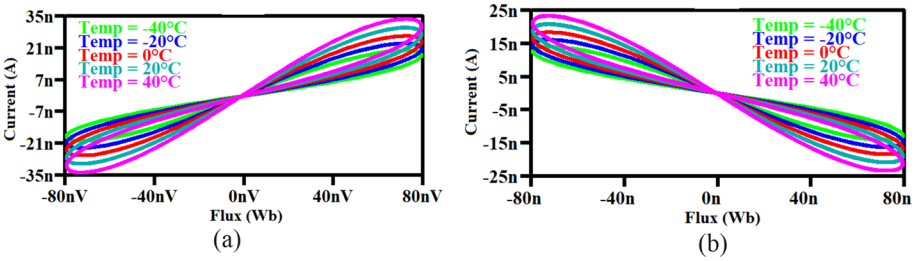


Fig. 13 Temperature analysis of **a** decremental Fractional order meminductor and **b** incremental Fractional order meminductor

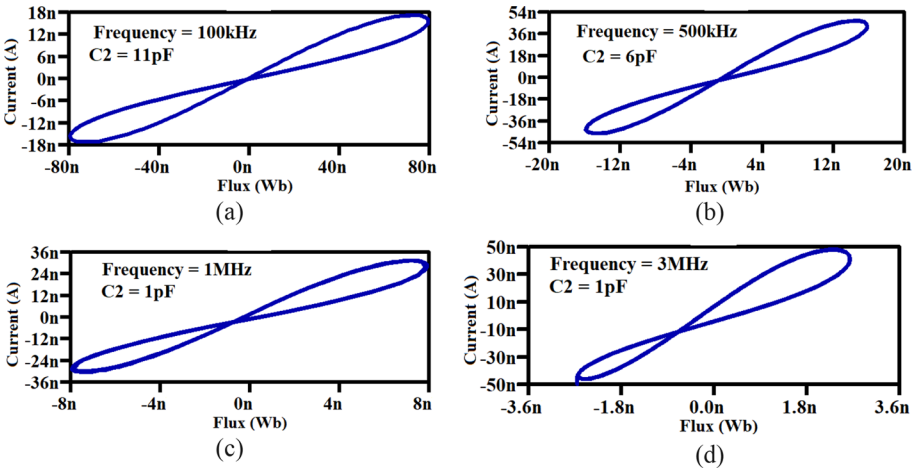


Fig. 14 Pinched Hysteresis Loops for different values of capacitances **a** $C_2 = 11$ pF **b** $C_2 = 6$pF **c** $C_2 = 1$pF **d** $C_2 = 1$pF

incremental fractional meminductor emulator. The temperature was adjusted between − 40 °C and + 40 °C. Figure 13 depicts the acquired results. The temperature study in Fig. 13 shows that the pinched hysteresis curves remain undistorted even when the temperature changes. As a result, the suggested decremental/incremental fractional meminductor emulator's temperature analysis is found to be satisfactory.

4.2 Pinched Hysteresis Loops at High Frequency

The pinched point (V = I = 0) is found to move further from the origin at higher frequencies. By appropriately scaling the value of the capacitor (C_2) utilised in the construction of the fractional meminductor emulator, this shifting can be avoided. The pinched hysteresis loops are displayed in Fig. 14, at various frequencies, when the capacitor value is adjusted correctly to keep the pinched point near the origin.

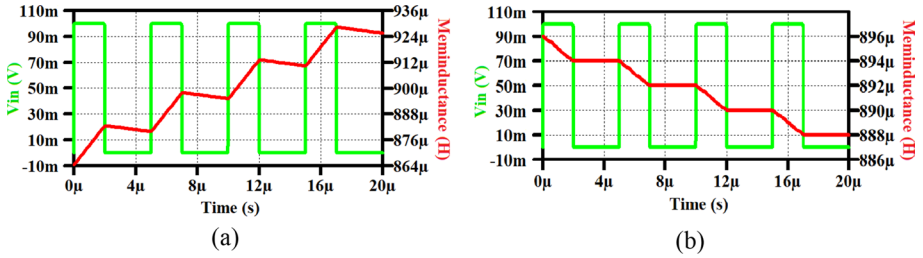


Fig. 15 Non-volatility test for proposed fractional order meminductor **a** Incremental **b** Decremental

4.3 Non-Volatility Test

Using a square pulse with a 100 mV amplitude, a pulse width of 2 µs, and a time period of 5 µs as the input signal, the non-volatility test for the suggested fractional-order meminductor emulator was carried out. The incremental order non volatility test is depicted in Fig. 15a, and it can be seen that when the pulse is high, the meminductance increases while in the non-pulse period the meminductor retains its value. Similarly, in Fig. 15b, the non-volatility test for decremental fractional-order meminductor is shown, and clearly there is negligible change in the meminductance during the non-pulse period while it decreases when the pulse is high.

5 Comparison of Proposed Fractional Order Meminductor Emulator with Other Meminductors in the Literature

The proposed fractional meminductor is contrasted with other meminductors in Table 2. The observations of Table 2 are given below,

1. Many of the reported meminductor emulators employ memristors alongside various passive and active components [19–25, 27], while the proposed circuit is memristor-less.
2. Many multipliers, current conveyors, operational amplifiers, as well as a significant amount of passive elements, are utilised by several meminductor;emulators; however, the proposed meminductor emulator is very simple in its design and makes use of minimal amount of components. [19, 22–25, 29–33, 46, 47, 49–51]
3. For the fractional-order inverse meminductor in [46] and the FOMI in [47–51], the highest frequency for which PHLs are valid is only in the order of kHz, but the maximum frequency for the suggested fractional meminductor emulator is 3 MHz.
4. The highest frequency for PHLs is limited to Hz and kHz for integral meminductor emulators reported in the literature [19, 20, 22–25, 29–32].
5. The proposed fractional meminductor can be used both as a floating and grounded fractional meminductor emulator while many of the emulators in the literature are of either only grounded type. [19, 20, 23, 30, 31, 46, 47, 51]

Table 2 Comparison of proposed circuit with other meminductor circuits in literature

Reference	Active components	Passive components	Memristor-less	Operating frequency
[19]	8 CCII+s, 1 AD633, 5 op amps, 1 memristor	11R, 3C	No	8 Hz
[20]	1 memristor, 1 op-amp	1R, 1C	No	–
[21]	4 CCII, 1 memristor	1R, 1C	No	20 Hz
[22]	2 AD844, 1 memristor	1R, 1C	No	1 kHz
[23]	1 memristor, 2 CCII+, 4 op amps, × 1 multiplierx	7R, 2C	No	800 Hz
[24]	3 CCII+, 3 op-amps, 1 multiplier, 1 memristor	3R, 1C	No	21.1 Hz
[25]	3 op-amps,l3 AD844, 1 AD633, × 1 memristor	10R, 2C	No	16 Hz
[27]	1 VDTA, 1 CDBA	2C	Yes	2 MHz
[28]	2lVDTA	1R, 2C	Yes	1 MHz
[21]	2 CCII, 1 memristor	1R, 1C	No	-
[29]	4 CCII+s, 3 oplamps, 1 multiplier	8R, 1C	Yes	36.9 Hz
[30]	3 oplamps, 1lmultiplier, 10lMOS	2R, 2C, 1L	Yes	300 Hz
[31]	3lCCII+, 1lmultiplier, 1ladder	3R, 2C	Yes	10 Hz
[32]	3lop-amps, 1lintegrator	3R, 2C	Yes	10 Hz
[33]	1lOTA, 1lCFOA, 2lCCIIs, 1lmultiplier	7R, 2C	Yes	5 kHz
[46]	2 CCII, 1 multiplier	3R, 1C, 1FOC	Yes	10 Hz
[47]	5 CCII, 1 multiplier	4R, 1FOC	Yes	10 kHz
[49]	2 CCII, 1 TA, 1 BOCCII, 1 memristor	1FOC	No	2 kHz
[50]	1 DVCC, 1 BOCCII, 1 memristor	1R, 1FOC	No	2 kHz
[51]	3 CCII, 1lmultiplier,l1 divider	3R, 1C, 1FOC	Yes	10 Hz
Proposed work	2 OTA, 1 CDBA	1C, 1FOC	Yes	3 MHz

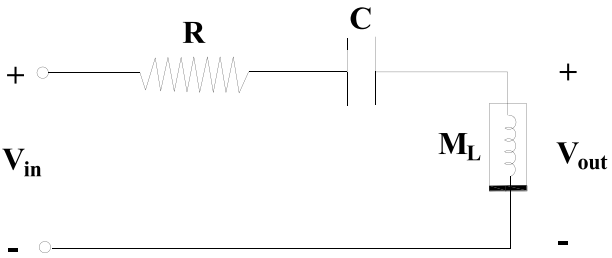


Fig. 16 Meminductor basedlAdaptive Learning Circuit

6 Application of the Proposed Fractional Meminductor Emulator

To test the proposed fractional meminductor emulator's functionality, we designed an adaptive learning circuit [60–62] that simulates an amoeba's behavioural reaction. The amoeba mechanism is based on the current and previous states of the system, and it describes the associative learning process. The following statements reflect an amoeba's associative learning process:

1. Remembering past events,
2. Predicting the future based on the past, and
3. To be able to recognise periodic event's timing patterns.

This circuit, consisting of a capacitor, a resistor, and the fractional meminductor emulator (Fig. 16), represents the behaviour of the amoeba learning process.

The inductance of a meminductor fluctuates depending on the current that has flowed through it in the past, hence the meminductor adapts to the frequency of the temperature swings corresponding to the input voltage (V_{in}). It regulates the amoeba's movement, where the output voltage V_{out}, over the meminductor, indicates the amoeba's movement speed according to the temperature changes. The values of the components used in the adaptive learning circuit are R = 500Ω, C = 50nF and the fractional meminductor emulator.

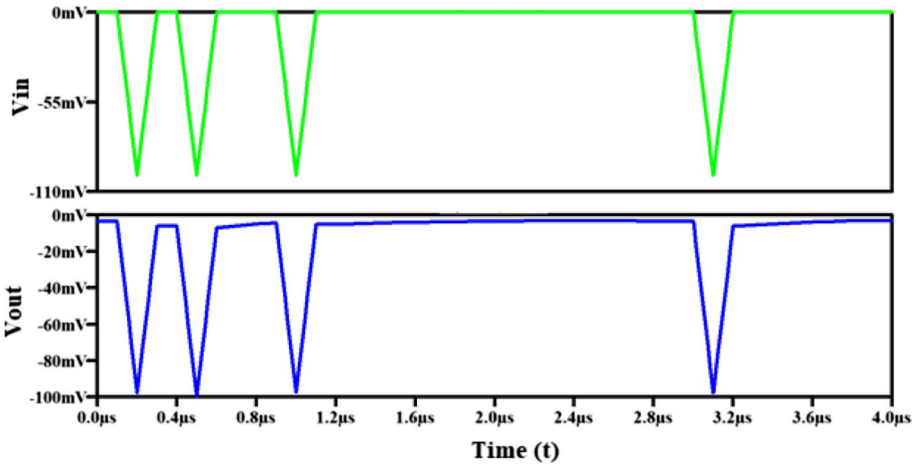


Fig. 17 Response of the adaptive learning circuit

From Fig. 17, we can clearly see that the output learns from the periodic behaviour of the input. After the low-temperature spike, it stays at low movement for some time in order to adapt quickly to the any other cold temperature spike. Only after sufficient time has passed, that it starts returning to the normal amount of activity, as can be seen after the first spike and between the 2nd and 3rd spike. This has shown that the designed adaptive learning circuit perfectly copies the behaviour of the amoeba learning.

7 Conclusion

A new design for an implementation of a grounded and floating incremental/decremental fractional meminductor emulator has been developed using two OTAs, a CDBA, a grounded capacitor, and a fractional capacitor. This emulator operates across a wide frequency range because the pinched hysteresis loops are not distorted up to 3-MHz frequency. The emulator's performance has also been confirmed to be satisfactory throughout a broad temperature range. There are several benefits to the proposed fractional meminductor emulator, including the absence of memristors, straightforward circuit design, and strong frequency response. By putting the suggested fractional meminductor emulator to use in an adaptive learning circuit, its performance was also verified.

Funding Not Applicable.

Data Availability Not applicable.

Code Availability Not Applicable.

Declarations

Conflict of interest All authors declare that there is no conflict of interest.

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