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New Grounded and Floating Decremental/Incremental Memristor Emulators Based on CDTA and Its Application

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Abstract
This paper presents grounded and floating memristor emulators based on current differencing transconductance amplifier. These emulators are realized using current differencing transconductance amplifier, operational transconductance amplifier and a grounded capacitor. Incremental to decremental memristor emulators and vice versa are easily obtained by modifying the circuit slightly. These memristor emulators are very simple in design over other complex realizations reported in the literature. The pinched hysteresis curves have been obtained without using analog multiplier for a wide range of frequency that varies from 600 kHz to 2 MHz. The property of retention has been verified for proposed design of memristor emulators after applying voltage pulse of amplitude 100 mV and frequency 1 MHz. Non-ideal analysis including the effects of parasitic impedances on the behaviour of proposed memristor emulators has also been presented. The proposed designs of memristor emulators have been simulated by Mentor Graphics Eldo simulation tool with TSMC 0.18 µm, level 53, CMOS technology parameters. The performance of proposed memristor emulator is verified by embedding it in the realization of current- mode analog filter.

Keywords CDTA · OTA · Memristor emulators · Filters · Oscillators · Current-mode circuits

1 Introduction

The three well-known circuit elements are resistor, capacitor and inductor. Memristor—the contraction of memory and resistor is the fourth fundamental circuit element which was postulated by Chua [1]. Initially, researchers had not shown much interest to work upon memristors due to limited resources available and lack of understanding. In May 2008, researchers of HP lab found a material namely TiO_2 which exhibits the behaviour of memristor at nano-scale regime [2]. But, memristor is still unavailable in the market as

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off-the-shelf component due to difficulties in fabrication and cost issues that restricts its use in real time applications. Therefore, memristor emulators are being designed to mimic its properties using analog active building blocks such as current conveyers (CC), current feedback operational amplifier (CFOA), current conveyer transconductance amplifier (CCTA), current backward transconductance amplifier (CBTA), current differencing buffered amplifier (CDBA), differential difference current conveyor (DDCC), voltage differencing current conveyor (VDCC), differential voltage current conveyor transconductance amplifier (DVCCTA), operational transconductance amplifier (OTA), voltage differencing transconductance amplifier (VDTA) and etc. A floating memristor emulator employing four current conveyors of second-generation (CCII), one multiplier, five resistors and one capacitor was reported in [3]. Another circuit of floating memristor was reported in [4] using four CCIIs, single operational amplifier, single multiplier, eight resistors and a capacitor. Thereafter, incremental/decremental memristor emulators were reported using DDCC, multiplier, two resistors and a grounded capacitor [5]. Afterward, a floating memristor emulator has been reported by using three electronically tunable CCIIs, one multiplier, four resistors and a grounded capacitor [6]. Next, a current controlled memristor emulator circuit using two CCII+, two bipolar junction transistors, one resistor and a capacitor was reported in which both simulations as well as experimental results are shown to verify the realization [7]. A continuous level memristor emulator using two CFOAs, single OTA, three resistors and two grounded capacitors has been reported and is also utilized to design the multivibrator [8]. A memristor emulator was reported by using double output CCII, multiplier, two resistors and a grounded capacitor that works in the frequency range of 16 Hz–16 kHz [9]. Another memristor emulator was reported using electronically tunable DDCC (formed by 6 OTAs), one multiplier, two resistors and a grounded capacitor [10]. A simple memristor emulator design was presented by using a CCII, exponential amplifier and three resistors [11]. The non-linear behaviour of memristor was obtained using CCII and exponential amplifier. A floating memristor emulator was reported using four CFOAs, two diodes, four resistors and four capacitors which were also utilized in the design of frequency to voltage conversion [12]. Thereafter, electronically tunable memristor emulator has been reported using four current conveyors of second generation, three OTAs, six resistors and a grounded capacitor [13]. Next, a floating memristor emulator has been reported using one OTA, two PMOS and one capacitor in which MOSFETs have been used in the sub-threshold region of operation [14]. A current controlled fractional order memristor was reported using two current conveyors of second generation, multiplier, three resistors and one fractional capacitor [15]. Floating and grounded memristor emulators using CCTA, three resistors and a capacitor has been reported in [16]. Thereafter, decremental/incremental memristor emulators that work at higher frequency were designed by using DVCCTA, three resistors and one capacitor [17]. A grounded configuration of memristor emulator using CBTA, multiplier, two resistors and a grounded capacitor was reported in [18]. A tunable memristor emulator was reported in [19] by employing an OTA having multiple outputs, one multiplier and a single capacitor. The arrangement of incremental and decremental memristor emulators has also been suggested by making a slight change in the configuration of reported memristor emulator. A second generation current conveyor based floating incremental/decremental memristor emulators have been presented using four current conveyors of second generation, multiplier, three resistors and one grounded capacitor [20]. A floating memristor was realized by employing a VDTA, one multiplier, two resistors and a capacitor. Both incremental and decremental configurations can be formed with a slight change suggested in the paper [21]. A floating memristor emulator using an OTA and a grounded capacitor has been reported in which both pre-layout and post-layout

simulation results have been included [22]. A memristor emulator was designed using seven MOSFETs and a grounded capacitor [23]. Next, a memristor emulator by using four OTAs, three resistors and one capacitor has been reported in [24] which were utilized in the design of high pass filter. A resistor-less grounded/floating memristor emulators using two OTAs and a capacitor has been reported in which both incremental and decremental configurations have been suggested [25]. A floating memristor emulator using VDCC, two PMOS transistors and one grounded capacitor has been reported [26]. A floating memristor emulator realized by employing VDTA and MOS-capacitor has been reported in [27]. A memristor emulator using three floating MOSFETs and a grounded capacitor has been reported in which both simulation and experimental results have been included [28]. A memristor emulator reported in [29] uses three current conveyors of second generation, one multiplier, three resistors and one grounded capacitor. Memristor emulator reported in [30] uses four CFOAs, two multipliers and nine resistors that operates only up to 10 Hz frequency. Recently, a memristor emulator is reported using OTA, CDBA and capacitor that operates up to 1 MHz frequency [31].

It has been observed that most of the reported structures of memristor emulators use multipliers to achieve the non-linear characteristics of memristor and also use passive resistors that lead to complex circuitry. Few memristor emulators that do not employ analog multiplier and passive resistors provide hysteresis loop which limited up to only few kHz frequencies. In some research papers, only grounded decremental configurations of memristor emulators have been reported. Therefore, the paper aims to design new resistor-less, high-frequency, floating and grounded decremental/incremental memristor emulators using one CDTA, one OTA and a capacitor. The proposed designs of memristor emulators are simpler as compared to other designs available in the literature because analog multiplier has not been used. CDTA and OTA both perform well at higher frequencies and therefore, in the proposed memristor emulators, pinched hysteresis curves have been formed for higher frequencies. The incremental to decremental memristor emulators and vice versa can be obtained by slight modification in the circuit. The performance of these memristor emulators has been shown by embedding it in the realization of analog filter.

The formation of paper is as follows. The paper has total eight sections comprising introduction. In Sect. 2, characteristics of both voltage tunable CDTA and voltage tunable OTA with their circuit diagrams are presented. Section 3 covers the realization of proposed floating and grounded decremental/incremental memristor emulators. Simulation results have been presented and discussed in Sect. 4. Section 5 covers the non-ideal analysis of proposed memristor emulators including parasitic impedances. In Sect. 6, performance of proposed memristor emulators has been compared with other reported memristor emulators. One application of analog filter has been included to prove the worthiness of proposed memristor emulators in Sect. 7. Concluding remarks are given in Sect. 8.

2 Characteristics of Voltage Tunable CDTA and OTA

Current differencing transconductance amplifier consists of two stages namely current differencing unit (CDU) that is followed by the transconductance amplifier (TA) as shown in Fig. 1. The input impedance of CDTA is very low whereas its output impedance is high. It accepts two currents Ip and In as inputs and provides the difference of these currents at z terminal as given in Eq. (1). Voltage Vz is obtained by connecting impedance Zz at z terminal and is given by Eq. (2). Transconductor converts the voltage Vz in two currents

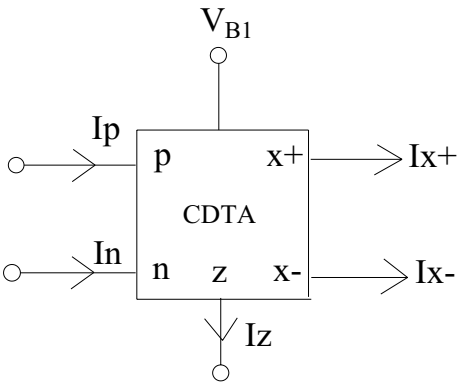

Fig. 1 Symbol of voltage tunable CDTA

which are equal in amplitude and opposite in phase and is given by Eq. (3). The structure of CDTA is slightly modified in which the bias current I_B is obtained using a current mirror structure constituted by MOSFETs M19, M20 and M21. The transconductance of voltage tunable CDTA depends on both bias voltage (V_{B1}) and technology parameters (μ_n and C_{ox}) as given in Eq. (4). The circuit diagram of voltage tunable CDTA is given in Fig. 2.

$$V_p = V_n = 0, \quad I_z = I_p - I_n, \tag{1}$$

$$V_z = I_z.Z_z, \tag{2}$$

$$I_{x+} = g_m V_z, \quad I_{x-} = -g_m V_z. \tag{3}$$

$$G_m = \frac{k}{\sqrt{2}}\left(V_{B1} - V_{SS} - 2V_{th}\right) \tag{4}$$

where $k = \mu_n C_{ox.} \frac{W}{L}$.

The symbol and circuit diagram of voltage tunable operational transconductance amplifier (OTA) are shown in Figs. 3 and 4, respectively. Two voltages V_{in1} and V_{in2} are applied to input

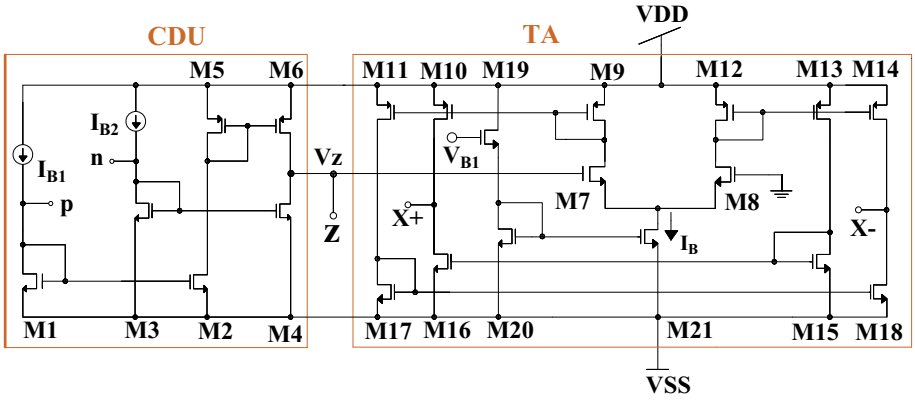

Fig. 2 Circuit diagram of voltage tunable CDTA

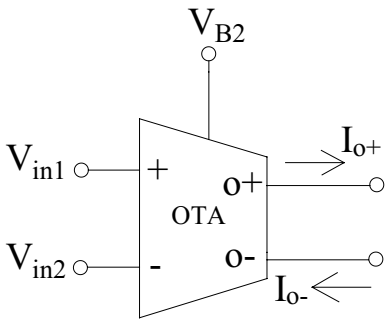

Fig. 3 Symbol of voltage tunable OTA

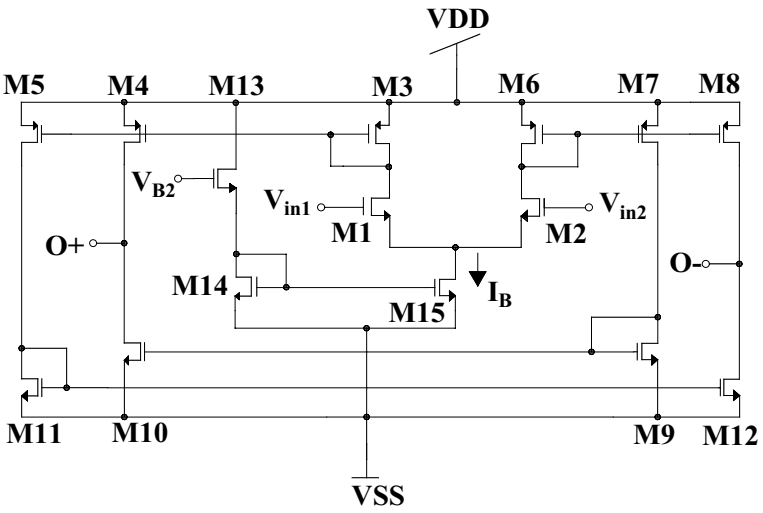

Fig. 4 Circuit diagram of voltage tunable OTA

terminals of OTA that gives two output currents Io+and Io- by its transconductance (g_m) as given in Eq. (5). The structure of OTA is slightly modified in which the bias current I_B is provided by structure of current mirror constituted by MOSFETs M13, M14 and M15. The variation in I_B is achieved by varying the bias voltage V_{B2} applied at gate terminal of MOSFET M13. The transconductance of voltage tunable OTA is obtained as given in Eq. (6) where k is $\mu_n C_{ox} \frac{W}{L}$.

$$I_{0+} = G_m(V_{in1} - V_{in2}), \quad I_{0-} = -G_m(V_{in1} - V_{in2}). \tag{5}$$

$$G_m = \frac{k}{\sqrt{2}}\left(V_{B2} - V_{SS} - 2V_{th}\right) \tag{6}$$

3 Proposed Configurations of Grounded and Floating Memristor Emulators

The proposed design of grounded and floating decremental/incremental memristor emulators are shown in Fig. 5a–d. In grounded decremental memristor emulator of Fig. 5a, one terminal of OTA is grounded whereas in floating decremental memristor emulator of Fig. 5b, both terminals are kept at different voltages. These grounded and floating decremental memristor emulators of Fig. 5a, b can be converted easily into grounded and floating incremental memristor emulators of Fig. 5c, d by interchanging the '+' and '−' terminals of OTA. The simple analysis of the circuit of Fig. 5a lead to following equations

$$I_{in} = I_{o-} = G_m V_{in} \tag{7}$$

$$I_c(t) = I_{x+} = G_m V_{in} \tag{8}$$

The voltage across capacitor is given as

$$V_c(t) = V_{B2} = \frac{1}{C}\int I_c(t)dt \tag{9}$$

After substituting the value of I_c (t) from Eq. (8) into Eq. (9), we get

$$V_c(t) = V_{B2} = \frac{1}{C}\int G_m V_{in}(t)dt = \frac{G_m \phi_{in}}{C} \tag{10}$$

where $\phi_{in} = \int V_{in}(t)dt$ is flux generated in memristor emulator.

Substituting the value of V_{B2} from Eq. (10) into Eq. (6), the value of transconductance is obtained as given in Eq. (11)

$$G_m = \frac{\frac{k}{\sqrt{2}}(-V_{ss} - 2V_{th})}{1 - \frac{k}{\sqrt{2}}\frac{\phi_{in}}{C}} \tag{11}$$

Substituting the value of G_m from Eq. (11) into Eq. (7), the value of memristance is obtained as given in Eq. (12)

$$M(\phi) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = -\underbrace{\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})}}_{\leftarrow\text{Fixed part}\rightarrow} + \underbrace{\frac{\phi_{in}}{C(V_{ss} + 2V_{th})}}_{\leftarrow\text{Variable part}\rightarrow} \tag{12}$$

It is clearly seen from Eq. (12) that the first part of the equation is fixed whereas the second part is variable. Therefore, it can be concluded from Eq. (12) that memresistance M (Φ) of decremental memristor emulator is varied with change in flux (Φ_{in}) generated in the circuit. The decremental memristor emulators can be changed into incremental memristor emulators after modifying the Eq. (12) as results in Eq. (13). The same is obtained in the circuit after interchanging the '+' and '−' terminals of OTA as shown in Fig. 5a, b.

$$M(\phi) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = -\underbrace{\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})}}_{\leftarrow\text{Fixed part}\rightarrow} - \underbrace{\frac{\phi_{in}}{C(V_{ss} + 2V_{th})}}_{\leftarrow\text{Variable part}\rightarrow} \tag{13}$$

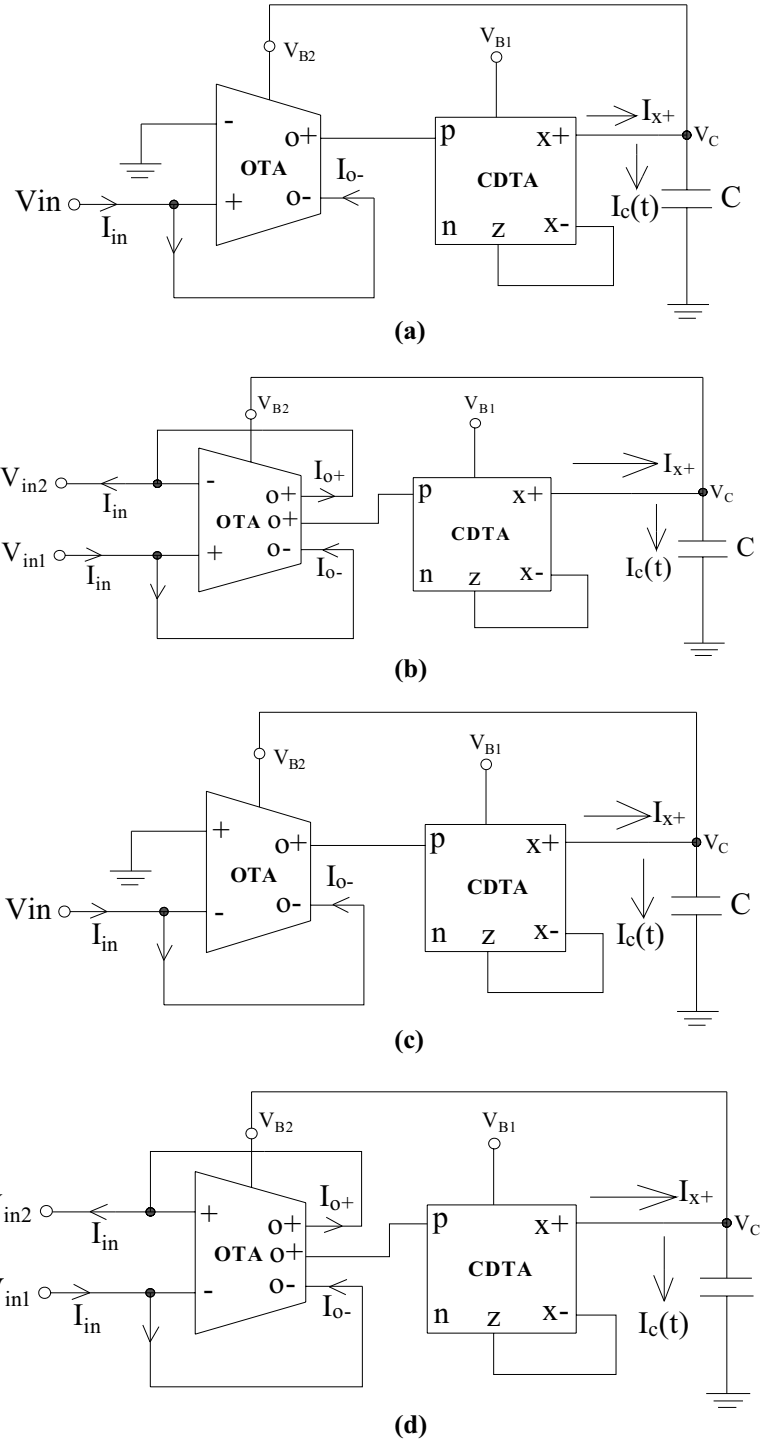

Fig. 5 Proposed memristor emulators. **a** Grounded decremental, **b** floating decremental, **c** grounded incremental and **d** floating incremental

After applying sinusoidal voltage $V_m \sin \omega t$ to grounded memristor emulator, the flux Φ_{in} results in

$$\phi_{in} = \frac{V_m}{\omega} \cos\left(\omega t - \frac{\pi}{2}\right) \tag{14}$$

where V_m is the maximum amplitude of the applied sinusoidal signal and ω is the frequency in radian/sec.

After substituting the value of Φ_{in} from Eq. (14) into Eqs. (12) and (13), we get

$$M(\phi) = -\underbrace{\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})}}_{\leftarrow \text{Fixed part} \rightarrow} \pm \underbrace{\frac{V_m \cos\left(\omega t - \frac{\pi}{2}\right)}{\omega C(V_{ss} + 2V_{th})}}_{\leftarrow \text{Variable part} \rightarrow} \tag{15}$$

From Eq. (15), it can be concluded that the memristance M (ϕ) of proposed grounded memristor emulators depend on the amplitude and operating frequency of the sinusoidal signal. It can be easily derived that the memristances M (Φ) of floating decremental and incremental memristors are

$$M(\phi) = \frac{V_{in2} - V_{in1}}{I_{in}} = \frac{1}{G_m} = -\underbrace{\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})}}_{\leftarrow \text{Fixed part} \rightarrow} \pm \underbrace{\frac{V_m \cos\left(\omega t - \frac{\pi}{2}\right)}{\omega C(V_{ss} + 2V_{th})}}_{\leftarrow \text{Variable part} \rightarrow} \tag{16}$$

The memristances M (Φ) of floating memristor emulators are also dependent on both amplitude and frequency of the input sinusoidal signal.

4 Simulation Results

The proposed designs of memristor emulators are simulated by Mentor Graphics Eldo simulation tool with TSMC 0.18 µm, level 53, CMOS technology parameters. The supply voltages for both CDTA and OTA are chosen as ± 0.9 V. Biasing currents of CDTA are selected as $I_{B1} = I_{B2} = 30$ µA. The value of bias voltage V_{B1} is 550 mV for CDTA. The value of capacitor is 40 pF. The amplitude of sinusoidal input signal is 100 mV. The aspect ratios of MOSFETs for voltage tunable CDTA and OTA are listed in Table 1.

Table 1 Aspect ratios of MOSFETs used in the design of CDTA and OTA

CDTA			OTA		
MOSFETs	W(µm)	L(µm)	MOSFETs	W(µm)	L(µm)
M1–M4	32	2	M1–M2	16	1
M5–M6	42.5	0.36	M3–M8	9	1
M7–M8	16	1	M9–M12	4	1
M9–M14	9	1	M13	15	0.18
M15–M18	4	1	M14–M15	14	0.18
M19	15	0.18			
M20–M21	14	0.18			

4.1 Simulation Results of Proposed Grounded Decremental/Incremental Memristor Emulators

To obtain the transient response, a sinusoidal input signal ($V_m = 100$ mV, f = 1 MHz) is applied at input terminals of proposed grounded incremental memristor emulator. It is evident from transient response of Fig. 6 that the voltage and current are opposite in phase for proposed grounded incremental configuration of memristor emulator. The voltage–current pinched hysteresis curves attained by proposed grounded decremental memristor emulators are illustrated in Fig. 7a–d for different frequencies of 600 kHz, 800 kHz, 1 MHz and 2 MHz. It is concluded from the figures that the decremental grounded memristor emulator works well for a wide range of frequency. It can be observed that the size of hysteresis curve decreases with increase in frequency. Figure 8 shows the effect of different temperatures on grounded decremental memristor emulator. It is observed that hysteresis loop shrinks with increase in temperature. The voltage-current pinched hysteresis curves of grounded incremental memristor emulators are illustrated in Fig. 9a–d. It is evident that the pinched hysteresis curves are not deformed for a wide range of frequency that varies from 600 kHz to 2 MHz. It gives satisfactory outputs for variations in temperatures from −40 to +40 °C as shown in Fig. 10.

4.2 Simulation Results of Proposed Floating Decremental/Incremental Memristor Emulators

A sinusoidal input signal ($V_m = 100$ mV, f = 1 MHz) is applied to obtain the transient response of proposed floating decremental memristor emulator. The transient response of decremental memristor emulator is shown in Fig. 11. The voltage–current pinched hysteresis curves of proposed floating decremental memristor emulator for frequencies of 600 kHz, 800 kHz, 1 MHz and 2 MHz are shown in Fig. 12a–d, respectively. The hysteresis curves of memristor emulators decrease with increase in frequency. Figure 13 shows the effect of temperature varying from −40 to +40 °C on the voltage–current pinched hysteresis loop of floating decremental memristor emulator. The hysteresis loop of proposed floating decremental memristor emulator is not deformed for temperature variations as can be seen from Fig. 13. The voltage–current hysteresis curves of proposed floating incremental memristor emulators are depicted in Fig. 14a–d. It can be seen that hysteresis curves shrink when operating frequency is increased. The performance of proposed floating

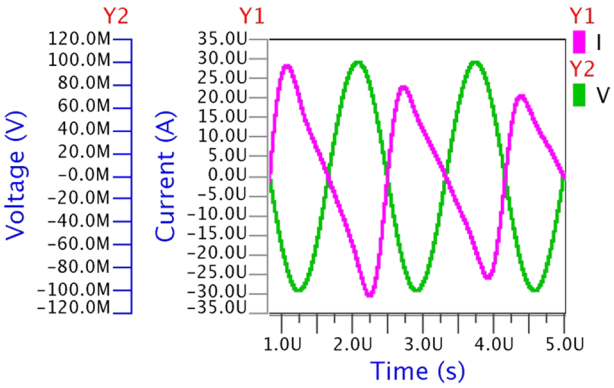

Fig. 6 Transient response of proposed grounded incremental memristor emulator

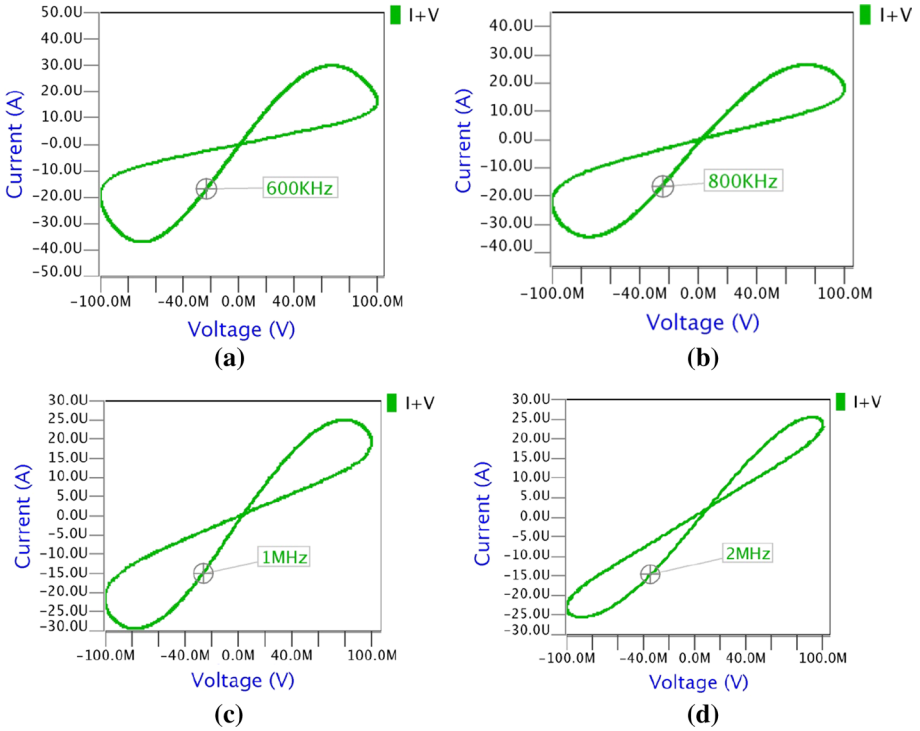

Fig. 7 Voltage–current hysteresis curves of proposed grounded decremental memristor emulator for frequencies of **a** 600 kHz, **b** 800 kHz, **c** 1 MHz, **d** 2 MHz

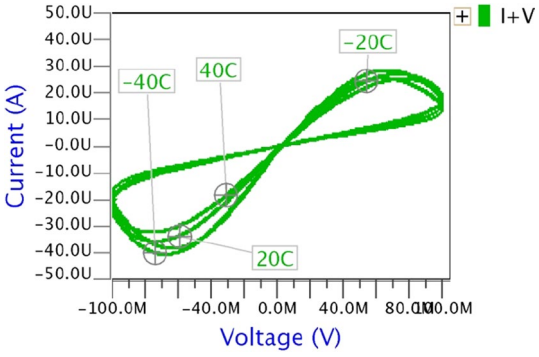

Fig. 8 Voltage–current hysteresis curves of proposed decremental memristor emulator for temperature variations

incremental memristor emulators is satisfactory even after variations in temperature from −40 to +40 °C as hysteresis loop is not deformed as shown in Fig. 15.

4.3 Monte Carlo Simulation Results of Proposed Memristor Emulators

Monte Carlo analysis have been performed for 200 runs to prove the robustness of the proposed design of memristor emulators. The sinusoidal signal having amplitude of 100 mV

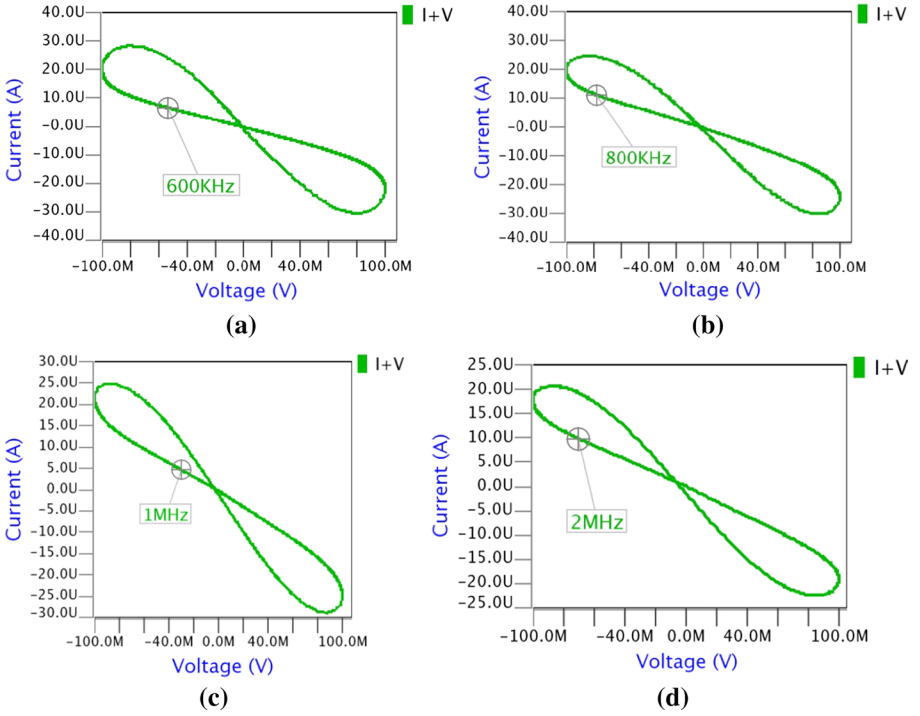

Fig. 9 Voltage–current hysteresis curves of grounded incremental memristor emulator for frequencies of **a** 600 kHz, **b** 800 kHz, **c** 1 MHz, **d** 2 MHz

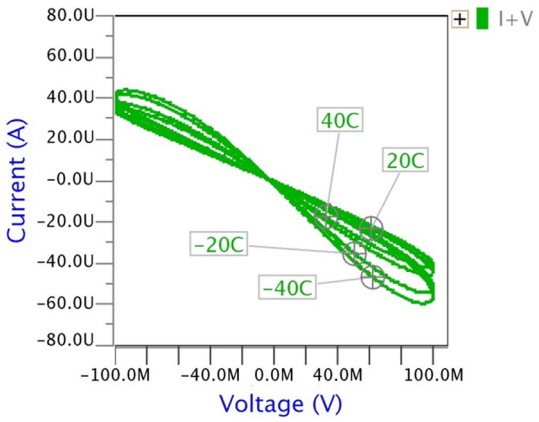

Fig. 10 Voltage–current hysteresis curves of proposed grounded incremental memristor emulator for temperature variations

and frequency of 1 MHz is applied at input terminals of proposed memristor emulators. The deviations in the parameters such as aspect ratios, threshold voltages and capacitances are chosen as gaussian random variations. The pinched hysteris curves obtained for proposed memristor emulators are shown in Fig. 16a–d. It is clearly observed that voltage–current pinched hysteris curves of Monte Carlo analysis are conversed and therefore the performances of proposed memristor emulators are satisfactory.

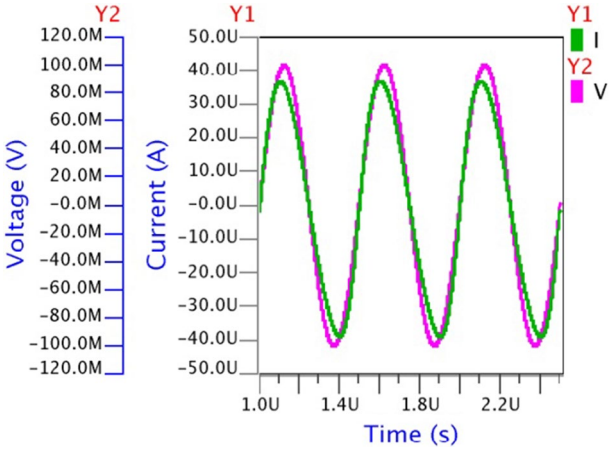

Fig. 11 Transient response of proposed floating decremental memristor emulator

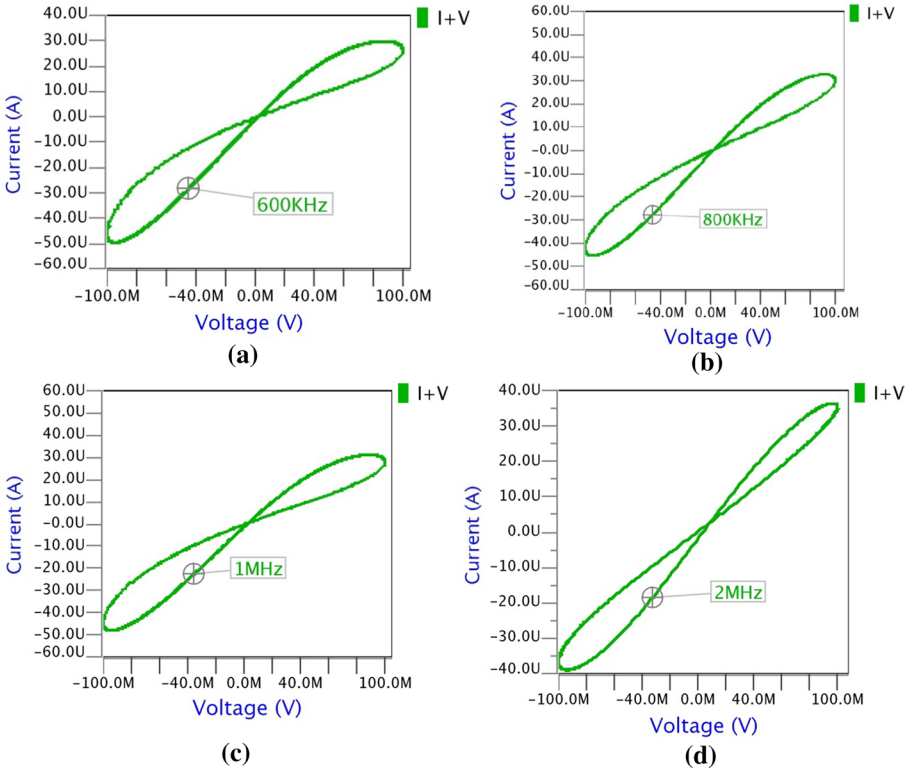

Fig. 12 Voltage–current hysteresis curves of proposed floating decremental memristor emulator for frequencies of **a** 600 kHz, **b** 800 kHz, **c** 1 MHz, **d** 2 MHz

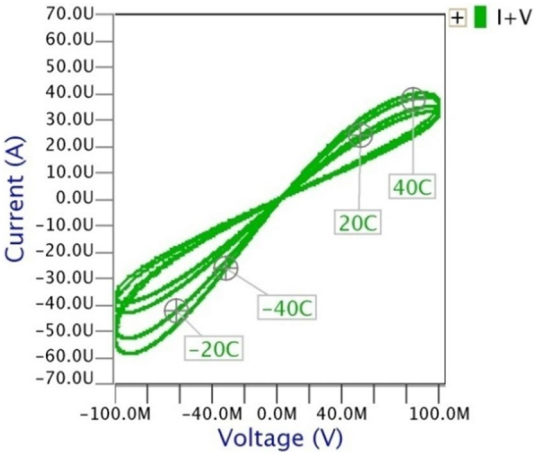

Fig. 13 Voltage–current hysteresis curves of proposed decremental memistor emulator for temperature variations

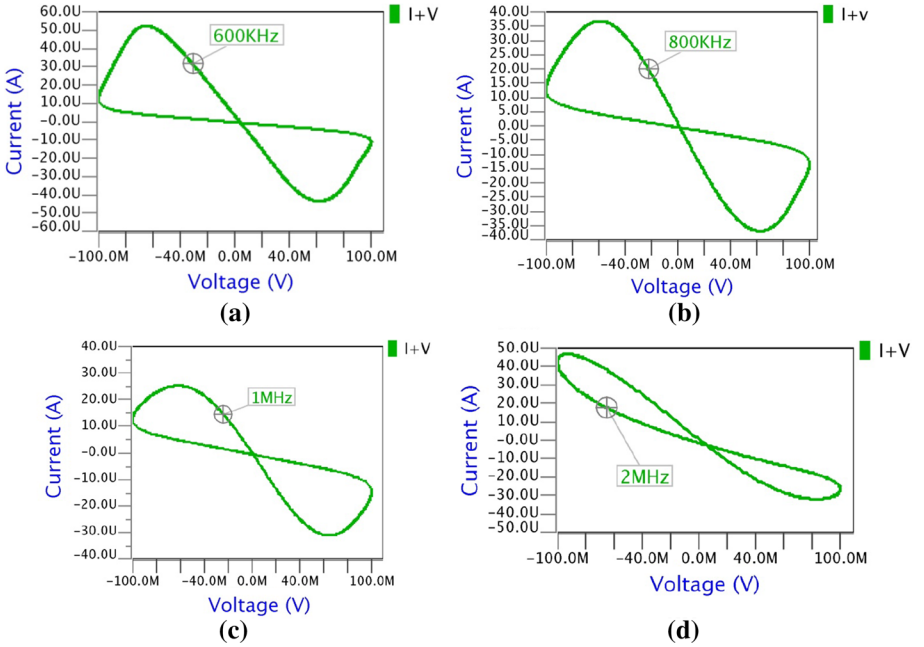

Fig. 14 Voltage–current hysteresis curves of proposed floating incremental memristor emulator for frequencies of **a** 600 kHz, **b** 800 kHz, **c** 1 MHz, **d** 2 MHz

4.4 Current Versus Time Plot for Pulse Input

In order to show the property of retention, the performance of proposed grounded memristor emulators has been analysed after applying a voltage pulse of 1 MHz frequency for a fixed "on" and "off" period. The obtained current versus time plots are given in Fig. 17a, b. It is observed from Fig. 17a that the input current of grounded incremental memristor emulator starts decreasing in the "on" period of input voltage and retained

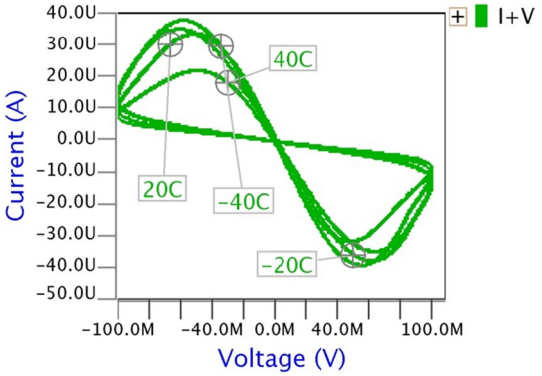

Fig. 15 Voltage–current hysteresis curves of proposed floating incremental memristor emulator for temperature variations

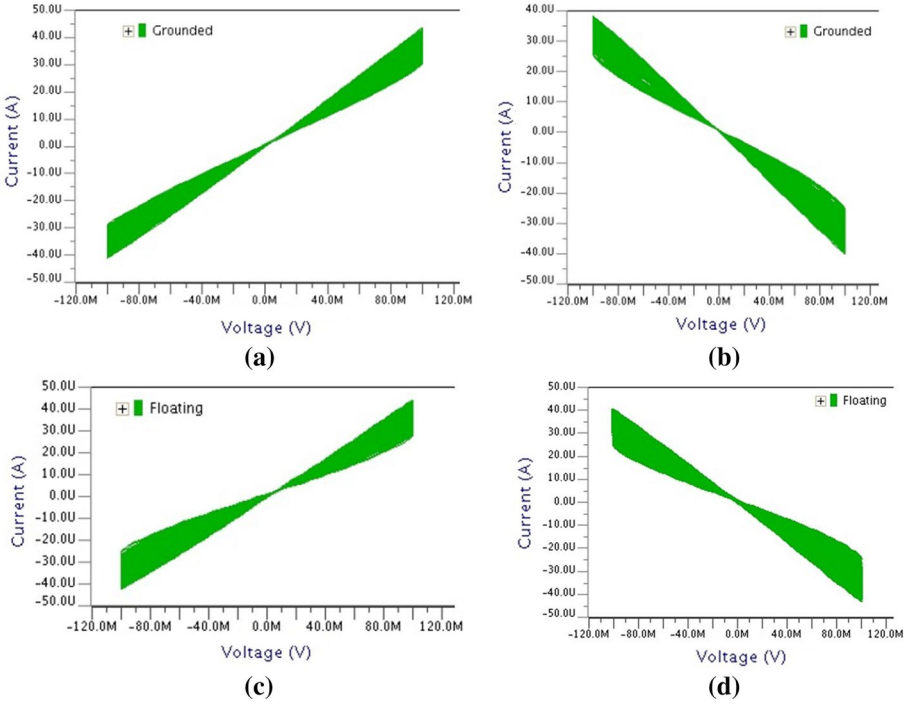

Fig. 16 Monte Carlo analysis of proposed memristor emulators. **a** Grounded decremental, **b** grounded incremental, **c** floating decremental, **d** floating decremental

its value for the "off" period. In the next cycle, the value of input current retained in the previous cycle decreases. Therefore, it is concluded that the memristance (opposite of current) increases for the "on" period and retained its value for the "off" period of input pulse for the grounded incremental memristor emulator. The same has been verified for proposed grounded decremental memristor emulator and is shown in Fig. 17b. Therefore, it is observed that the proposed memristor emulators hold the property of retention.

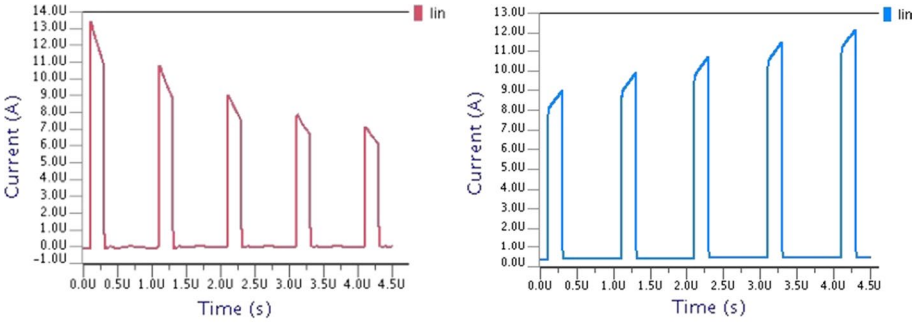

Fig. 17 Current versus time plot for proposed memristor emulators: **a** grounded incremental, **b** grounded decremental

5 Non-ideal Analysis of Proposed Grounded Decremental Memristor Emulator

The performance of proposed grounded decremental memristor emulator is analysed after considering non-ideal effects of CDTA and OTA. Non-ideal model of CDTA and OTA including parasitic effects at different terminals are considered for non-ideal analysis. The non-ideal effects on the performance of grounded decremental memristor emulator are discussed in this section.

5.1 Characteristics of Non-ideal CDTA

The non-ideal CDTA is shown in Fig. 18. The characteristic equations of non-ideal CDTA after considering parasitic resistances and capacitances are given as

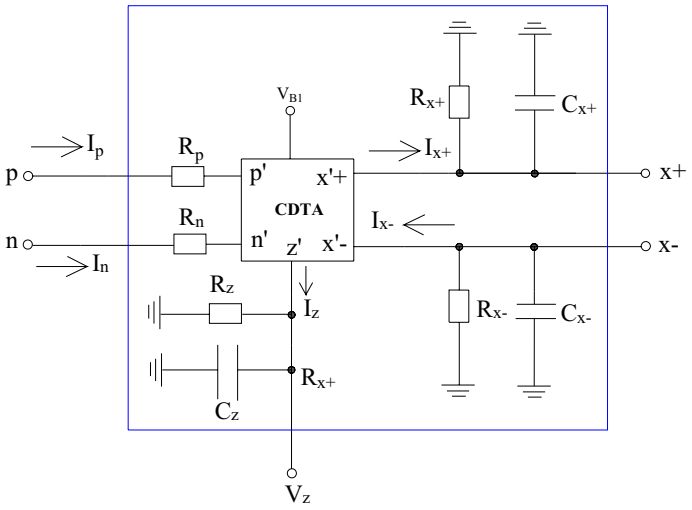

Fig. 18 Non-ideal CDTA

$$V_p = I_p R_p, \quad V_n = I_n R_n, \quad I_z = \alpha_p I_p - \alpha_n I_n, \tag{17}$$

$$I_{x+} = \beta g_m V_z, \quad I_{x-} = -\beta g_m V_z. \tag{18}$$

where R_p and R_n are the parasitic resistances of input terminals (p and n) of CDTA, α_p and α_n are current transfer ratios between p to z terminals and n to z terminals, respectively. Transconductance tracking error from z to x+ and z to x− terminals are given as β. In ideal-CDTA, parasitic resistances R_p and R_n are considered zero whereas current tracking errors (α_p and α_n) and transconductance tracking error (β) are considered one.

5.2 Characteristics of Non-ideal OTA

The non-ideal OTA shown in Fig. 19 includes parasitic resistance R_{in+} that appears in parallel with parasitic capacitance C_{in+} at input "+" terminal. Similarly, parasitic resistance R_{in-} that appears in parallel with parasitic capacitance C_{in-} at input "−" terminal. The parasitic resistance R_{o+} is connected in parallel with parasitic capacitance C_{o+} at output "o+" terminal while parasitic resistance R_{o-} appears in parallel with parasitic capacitance C_{o-} at output "o−" terminal. The transconductance of OTA cannot be maintained at constant value for all operating frequencies. Therefore, it is a function of frequency and is represented by $G_m(s)$. Therefore, the output current I_{o+} is given by

$$I_{o+} = G_m(s) V_{in} \tag{19}$$

where V_{in} is the difference of V_{in+} and V_{in-}.

The transconductance $G_m(s)$ can be represented by

$$G_m(s) = \frac{G_{m0}}{1 + \frac{s}{\omega_{gm}}} \tag{20}$$

where G_{m0} is transconductance at dc that get reduced as pole frequency ω is increased.

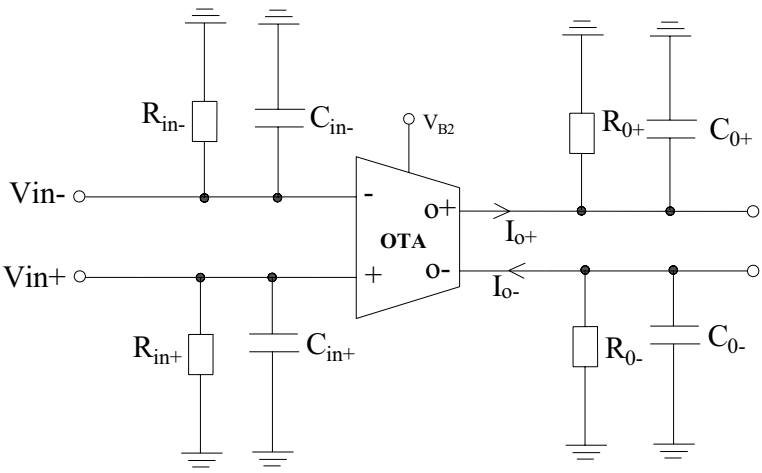

Fig. 19 Non-ideal OTA

5.3 Performance of Proposed Memristor Emulator Considering Non-ideal Effects

The non-ideal equivalent circuit of proposed memristor emulator is shown in Fig. 20. The various parasitic impedances (Z_{p1}, Z_{p2}, Z_{p3}, Z_{p4} and Z_{p5}) connected at different terminals of OTA and CDTA can be given as

$$\begin{aligned} Z_{p1} &= R_{in+} || \frac{1}{sC_{in+}}, \quad Z_{p2} = R_{0-} || \frac{1}{sC_{0-}}, \quad Z_{p3} = R_{0+} || \frac{1}{sC_{0+}} \\ Z_{p4} &= (R_z || R_{x+}) || \frac{1}{s(C_z + C_{x+})}, \quad Z_{p5} = R_{x+} || \frac{1}{s(C + C_{x+})} \end{aligned} \tag{21}$$

The output currents $I_{0-}(t)$ and $I_{0+}(t)$ at "o−" and "o+" terminals of OTA are given as

$$I_{o-}(t) = I_{o+}(t) = G_m(s)V'_{in}(t) = G_m(s)V_{in}(t) \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \tag{22}$$

The current at intermediate terminal Z of CDTA can be expressed as

$$I_z = \alpha_P I_p = \alpha_P I_{0+}(t) \times \frac{Z_{p3}}{R_p + Z_{p3}} \tag{23}$$

where α_P represents current tracking error of P to Z terminal and R_P represents parasitic resistance at input terminal "p" of CDTA.

After substituting the value of $I_{0+}(t)$ from Eqs. (22) to (23), we get

$$I_z = \alpha_P G_m(s)V_{in}(t) \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \tag{24}$$

The z′ terminal is directly connected to x′− terminal of CDTA in Fig. 20. Due to parasitic impedance Z_{p4} that appears at z′ terminal of CDTA, a current tracking error α_c will be introduced between z′ and x′− terminal of non-ideal CDTA which results in

$$I_{x-} = I_{x+} = \alpha_c \alpha_P G_m(s)V_{in}(t) \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \tag{25}$$

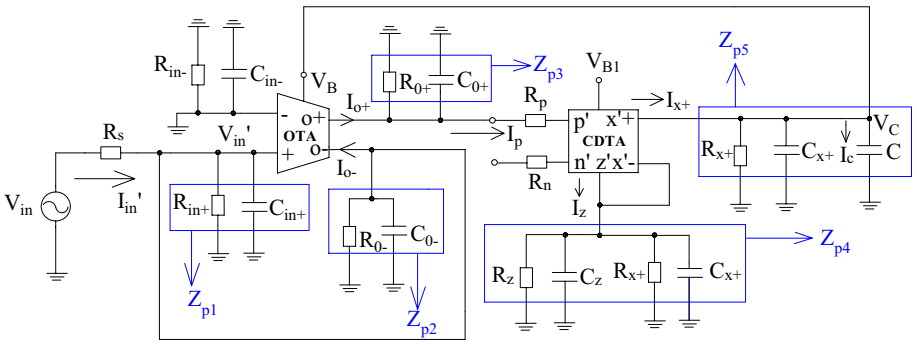

Fig. 20 Non-ideal equivalent circuit of proposed grounded decremental memristor emulator

The value of $V_c(t)$ can be easily calculated from Fig. 20 as

$$V_c(t) = I_{x+} \times Z_{p4} = \alpha_c \alpha_P G_m(s) V_{in}(t) \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \times \frac{1}{s(C + C_{x+}) + \frac{1}{R_{x+}}} \tag{26}$$

As the value of $1/Rx+ \ll s\,(C+C_{x+})$, Eq. (26) is now approximated as

$$V_c(t) = I_{x+} \times Z_{p4} = \alpha_c \alpha_P G_m(s) V_{in}(t) \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \times \frac{1}{s(C + C_{x+})} \tag{27}$$

Equation (27) can be expressed as

$$V_c(t) = I_{x+} \times Z_{p4} = \alpha_c \alpha_P \times \frac{1}{(C + C_{x+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \times \int G_m(s) V_{in}(t) dt. \tag{28}$$

The biasing voltage V_B is equal to V_c (t) and can be expressed as

$$V_B = I_{x+} \times Z_{p4} = \alpha_c \alpha_P \times \frac{1}{(C + C_{x+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \times \int G_m(s) V_{in}(t) dt. \tag{29}$$

The term $\int V_{in}(t)dt$ is the flux generated in memristor emulator and can be substituted by flux ϕ_{in}. Thus the Eq. (29) can be modified as

$$V_B = I_{x+} \times Z_{p4} = \alpha_c \alpha_P \times G_m(s) \times \frac{1}{(C + C_{x+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \times \frac{Z_{p3}}{R_p + Z_{p3}} \times \phi_{in}. \tag{30}$$

After substituting the value of V_B in Eq. (6), we get

$$G_m(s) = \frac{\mu_n C_{ox} \frac{W}{L}}{\sqrt{2}} \left[\left(G_m(s) \times \alpha_c \alpha_p \times \frac{1}{(C + C_{x+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \cdot \frac{Z_{p3}}{R_p + Z_{p3}} . \phi_{in} \right) - V_{SS} - 2V_{th} \right] \tag{31}$$

The Eq. (31) can be rearranged as

$$G_m(s) = -\frac{\frac{\mu_n C_{ox} \frac{W}{L}}{\sqrt{2}} (V_{SS} + 2V_{th})}{1 - \frac{\mu_n C_{ox} \frac{W}{L}}{\sqrt{2}} \left[\alpha_c \alpha_p \times \frac{1}{(C + C_{x+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_{p1}||Z_{p2}}} \cdot \frac{Z_{p3}}{R_p + Z_{p3}} . \phi_{in} \right]} \tag{32}$$

The input current I_{in}' (t) is obtained from Fig. 20 as

$$I'_{in}(t) = I_{o-}(t) \times \left[1 + \frac{R_o}{Z_{p1}||Z_{p2}} \right] \tag{33}$$

where R_0 represents the output resistance of OTA.

After substitution of current I_{o-}(t) from Eqs. (22) to (33)

$$I'_{in}(t) = G_m(s)V'_{in}(t)\left[1 + \frac{R_o}{Z_{p1}||Z_{p2}}\right] \tag{34}$$

The value of memristance $M(\phi_m)$ is obtained from Eq. (34) for non-ideal memristor emulator as

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = \frac{1}{G_m(s)} \times \frac{1}{1 + \frac{R_o}{Z_{p1}||Z_{p2}}} \tag{35}$$

The value of memristance is obtained after replacing the value of G_m (s) from Eq. (32) into Eq. (35) as

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1}{\frac{\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})}{1-\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}\left[\alpha_c\alpha_p \times \frac{1}{(C+C_{x+})}\cdot\frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\cdot\frac{Z_{p3}}{R_p+Z_{p3}}.\phi_{in}\right]}} \times \frac{1}{1+\frac{R_o}{Z_{p1}||Z_{p2}}} \tag{36}$$

Rearranging the terms of Eq. (36) results in

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1-\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}\left[\alpha_c\alpha_p \times \frac{1}{(C+C_{x+})}\cdot\frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\cdot\frac{Z_{p3}}{R_p+Z_{p3}}.\phi_{in}\right]}{\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})} \times \frac{1}{1+\frac{R_o}{Z_{p1}||Z_{p2}}} \tag{37}$$

The value of $Z_{p1}||Z_{p2}$ is very high as compared to R_0, therefore Eq. (37) is reduced to

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1-\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}\left[\alpha_c\alpha_P \times \frac{1}{(C+C_{x+})}\cdot\frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\cdot\frac{Z_{p3}}{R_p+Z_{p3}}.\phi_{in}\right]}{\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})} \tag{38}$$

Rearranging the terms of Eq. (38) leads to

$$M(\phi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = -\frac{1}{\frac{\mu_n C_{ox}\frac{W}{L}}{\sqrt{2}}(V_{SS}+2V_{th})} + \frac{\alpha_c\alpha_P\cdot\frac{1}{(C+C_{x+})}\cdot\frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_{p1}||Z_{p2}}}\cdot\frac{Z_{p3}}{R_p+Z_{p3}}.\phi_{in}}{(V_{SS}+2V_{th})} \tag{39}$$

The values of current transfer ratios α_c and α_p are very close to unity. The parasitic capacitance C_{x+} is found to be very low as compared to capacitor C. The source resistance (R_s) value is quite low. The parasitic resistances R_{o+} and R_{o-} are very high and are in the range of several hundred KΩ. The value of R_P is very low. After taking these considerations, the value of memristance $M(\phi_m)$ obtained by Eq. (39) will be in close proximity of memristance derived under ideal assumptions. Therefore, the behaviour of memristor emulator under non-ideal assumption is satisfactory.

6 Performance Comparison of Memristor Emulators

The comparison of proposed memristor emulators has been done in Table 2 on the basis of number of active and passive components used in the design of memristor emulators, range of frequency over which it works satisfactorily, supply voltage used and different types of configurations realized. Memristor emulators reported in [3, 5, 6, 9–11, 18, 19, 21, 29, 30] use analog multipliers and therefore circuits become complex whereas proposed memristor emulators do not employ multiplier that leads to simpler realizations. Memristor emulators reported in [3, 6, 8–14, 18, 19, 29, 30] work satisfactorily in the frequency range of Hz and KHz only. Memristor emulator reported in [5, 17] operate in MHz range but their frequency of operation is limited to 1 MHz frequency. Memristor emulator suggested in [25] give different frequency of operation for grounded and floating type configurations whereas proposed memristor emulators perform well up to 2 MHz frequency for both grounded and floating configurations. Excess active and passive components are used in the realization of memristor emulators reported in [3, 5, 6, 8–14, 17–19, 29, 30] whereas proposed configuration of memristor emulators use two active and one passive component only. The proposed memristor emulators realize both grounded and floating configuration whereas memristor emulator reported in references [8–11, 17–19, 29] realize only grounded configuration. The memristor emulators reported in [3, 5, 6, 8–13, 17–19, 21, 29, 30] use resistors while the proposed memristor emulators do not employ resistors. Memristor emulators reported in [3, 5, 6, 8–14, 17, 19, 25, 29, 30] use higher supply voltage as compared to proposed configurations of memristor emulators. Therefore, proposed memristor emulators are superior in performance as compared to other designs available in the literature.

7 Application of Grounded Memristor Emulator in Current-Mode Tow–Thomas Biquad

Tow–Thomas biquad is a standard filter realized by CDTAs as shown in Fig. 21. The proposed grounded decremental memristor emulator of Fig. 5a has been used as a memristor M_R (replacing R) in the realization of Tow–Thomas biquad. The grounded memristor emulator offers average memristance (M_R) of 1 KΩ for the sinusoidal input signal of amplitude (V_m) 100 mV and frequency of 2 MHz. The value of V_B is adjusted to 0.9 V. The bias current of CDTA is set to 100 μA which offers the transconductance (g_m) to 0.574 mA/V. The center frequency (f_0) of filter is given by

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{40}$$

Figure 22 shows the responses of low pass; band pass and high pass for Tow–Thomas biquad when 1 K resistor (R) is connected at z terminal of CDTA 1. The center frequency is obtained as 1.8 MHz. The frequency responses of low pass, band pass and high pass biquad after connecting memristor (M_R) is shown in Fig. 23 which also offers the same center frequency of 1.8 MHz. Transient responses of Tow–Thomas biquad after connecting memristor (M_R) are shown in Figs. 24, 25 and 26. Figure 24 shows the response of Tow–Thomas biquad when low frequency sinusoidal signal of 50 Hz is applied. It is observed that filter provides gain only for low pass output whereas band pass and high pass outputs get attenuated. Similarly, when an input sinusoidal signal of 1 MHz is applied to filter, it provides gain to low pass, band pass and high pass because it is closer to center frequency as shown in Fig. 25.

Table 2 Comparison of memristor emulators

Ref.	No. of active blocks	No. of resistors (R) and capacitors (C)	Supply voltage	Range of frequency (Hz)	Floating (F) or grounded (G)
[3]	4 CCIIs, 1 Op-Amp and 1 multiplier	10 and 1	±15 V	160	F
[5]	1 DDCC and 1 multiplier	2 and 1	±1.5 V	1 M	F
[6]	3 ECCIIs and 1 multiplier	4 and 1	±10 V	5 K	F
[8]	2 CFOAs and 1OTA	3 and 2	±12 V	2 K	G
[9]	2 CCIIs and 1 multiplier	4 and 3	±10 V	270 K	G
[10]	6 OTAs and 1 multiplier	2 and 1	±10 V	1.5 K	G
[11]	1 CCII, 1 multiplier, 2 transistors and 1 amplifier	5 and 1	±1 V	3 K	G
[12]	4 CFOAs and 2 Diodes	5 and 4	±10 V	2.9 K	F
[13]	4CCIIs and 3 OTAs	5 and 1	±15 V	10 K	F
[14]	1 OTA and 2 PMOS	0 and 1	±1 V	30	F
[17]	1 DVCCTA	3 and 1	±1.25 V	1 M	G
[18]	1 CBTA and 1 multiplier	2 and C	±0.9 V	100 K	G
[19]	1 OTA and 1 Multiplier	1 and 1	±5 V/1.2 V	10 K	G
[21]	1 VDTA and 1 multiplier	2 and 1	±0.9 V	2 M	F
[25]	2 OTAs	0 and 1	±1.2 V	400 K/8 M	F and G
[29]	3 CCIIs and 1 multiplier	3 and 1	±12 V	4 K	G
[30]	4 CFOAs and 2 multipliers	9 and 1	±2 V	10	F
Proposed	1 OTA and 1 CDTA	0 and 1	±0.9 V	2 M	F and G

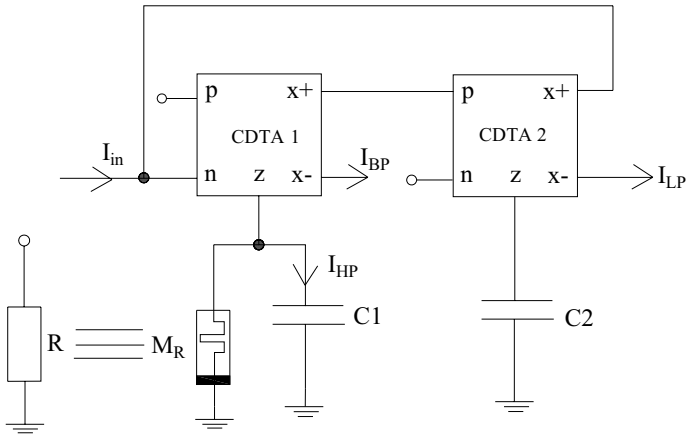

Fig. 21 Current-mode Tow–Thomas biquad realized by CDTAs [32]

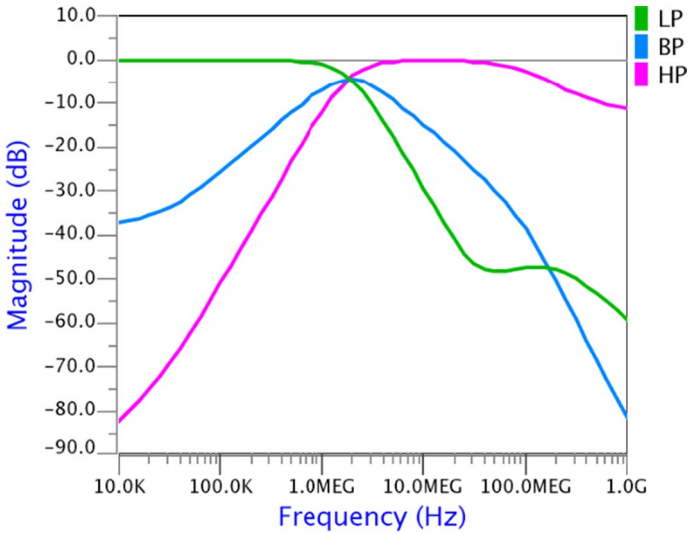

Fig. 22 Response of Tow–Thomas biquad when resistance (R) of 1 kΩ is used

When a high frequency input sinusoidal signal of 20 MHz is applied, it provides gain only to high pass while other two outputs namely low pass and high pass get attenuated as shown in Fig. 26. Therefore, it is concluded from transient responses of Tow–Thomas biquad that the behaviour of grounded memristor emulator as a memristance (M_R) is good enough over a wide frequency range.

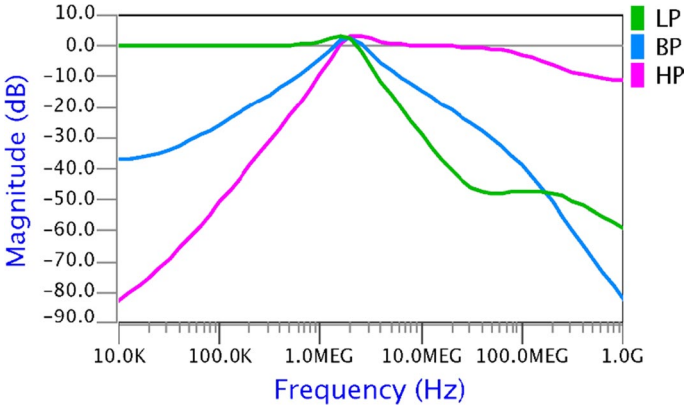

Fig. 23 Response of filter obtained when memristance (M_R) of 1 kΩ is used

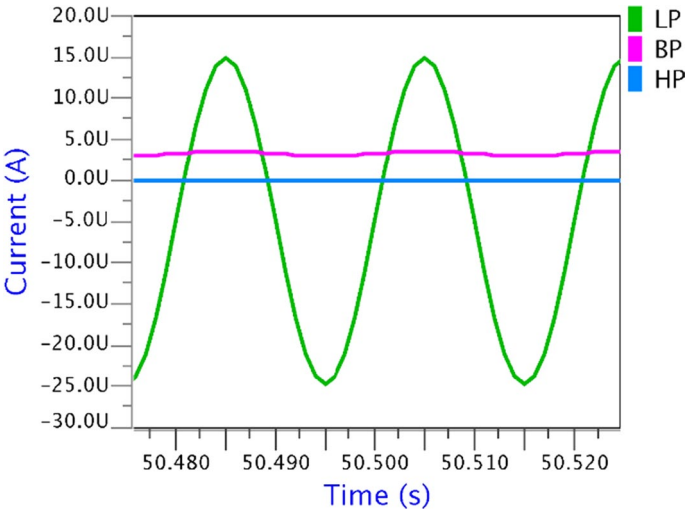

Fig. 24 Transient response of filter obtained by connecting memristance of 1 kΩ for the input signal of 50 Hz frequency

8 Conclusions

New grounded and floating configurations of decremental and incremental memristor emulators have been proposed. The designs of memristor emulators are very simple as compared to other designs available in the literature as analog multiplier has not been used. The voltage–current hysteresis curves obtained by these emulators are not deformed over a wide frequency range and ensure the operation of emulators from low to high frequency range. The performance of grounded memristor emulator has been verified by using it in the design of current-mode Tow- Thomas biquad. It gives almost the same performance and center frequency when resistor (R) is replaced by memristance (M_R) offered by memristor emulators.

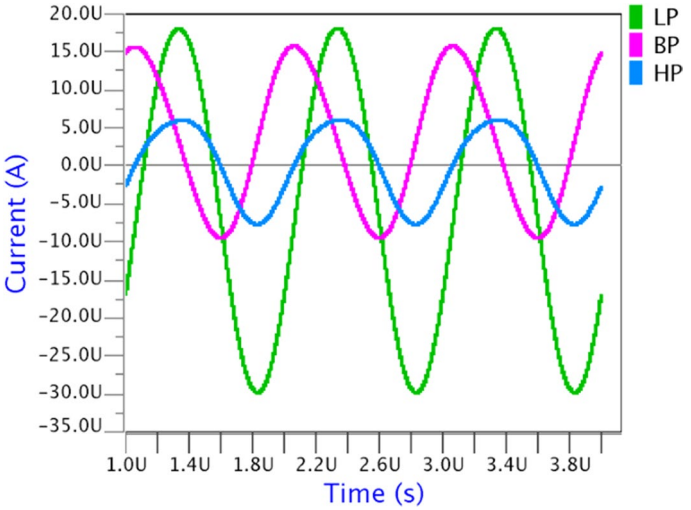

Fig. 25 Transient response of filter obtained by connecting memristance of 1 kΩ for the input signal of 1 MHz frequency

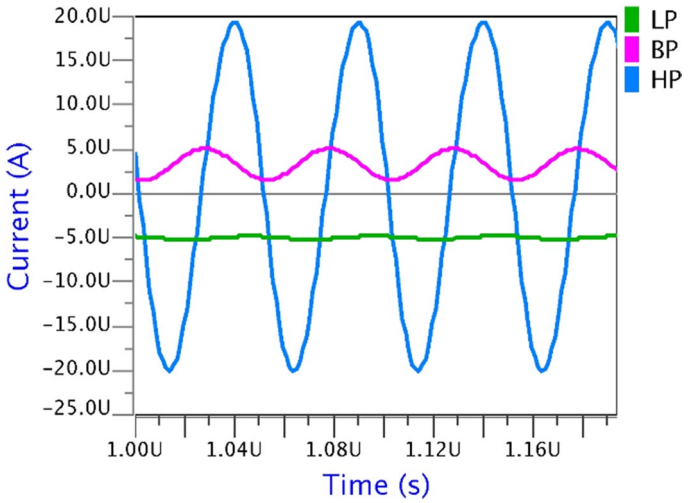

Fig. 26 Transient response of filter obtained by connecting memristance of 1 kΩ for the input signal of 20 MHz frequency

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