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Design and Analysis of Tunable Voltage Differencing Inverting Buffered Amplifier (VDIBA) with Enhanced Performance and Its Application in Filters

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Abstract This paper proposes a high performance tunable Voltage Differencing Inverting Buffered Amplifier (VDIBA) where transconductance of VDIBA is enhanced by using programmable positive feedback technique and bandwidth is enhanced by using resistive compensation technique. The enhanced performance of proposed VDIBA is demonstrated by presenting detailed frequency analysis. Furthermore, it is verified that transconductance of proposed VDIBA can be enhanced up to 10.6 mS at tuning current (Ic) of 100 μA. Moreover, resistive compensation technique enhance bandwidth of propose circuit up to 263 MHz. To illustrate the effectiveness of proposed circuit, voltage mode universal biquad filter is designed as an application example. The pole frequency of proposed filter is tunable in range of 10.5–83.4 MHz. The proposed VDIBA and its filter applications are designed and simulated using TSMC 0.18 μm CMOS technology in Cadence virtuoso schematic composer at ± 0.6 V supply voltage.

Keywords VDIBA · High transconductance · Programmable positive feedback · Voltage mode universal biquad filter

1 Introduction

In scale down CMOS technology and increasing demand of portable electronic circuits have encouraged researchers towards development of high performance low voltage mixed mode signal processing circuits. Compatibility with digital circuits integrated on one chip

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forces analog circuits to operate under low supply voltages. Several novel active elements such as Voltage Differencing Buffered Amplifier (VDBA), Voltage Differencing Transconductance Amplifier (VDTA), Voltage Differencing Current conveyor (VDCC), Current Differencing Buffered Amplifier (CDBA), Current Differencing Transconductance Amplifier (CDTA), Second Generation Current Conveyor (CCII), CFOA (Current Feedback Operational Amplifier) and others have been suggested by Biolek et al. [1] for analog signal processing applications. Apart from architecture of these active elements, there are many applications like filters, oscillators, multipliers and modulators based on these active elements have also been reported in the literature [2–15]. VDIBA is one of the recent active element introduced in [16] for analog signal processing applications. The CMOS implementation of VDIBA has been presented by Herencsar et al. [17]. The most important parameter of VDIBA is transconductance of OTA stage which directly controls various design parameters [such as pole frequency (ω_0), quality factor (Q)] of filters and oscillators. Therefore, VDIBA with high transconductance (G_m) is required for high frequency applications. VDIBA block has inbuilt tunability feature which provides advanced electronic control of parameters, although it does not provide characteristics like low voltage, low power and high transconductance. In this paper programmable positive feedback loop consisting of cross-coupled MOSFETs is used to generate negative transconductance ($-g_m$) which cancels positive output conductance of PMOS load transistors and NMOS differential pair. The proposed VDIBA is based on classical differential structure using PPF technique to enhance G_m of transconductance stage. The resistive compensation technique is used in transconductance stage to enhance bandwidth of proposed VDIBA structure. The combined effect of both techniques produce high transconductance cell, which can be used in more challenging analog signal processing applications. As an application example, the voltage mode universal biquad filter is designed to demonstrate effectiveness of proposed VDIBA circuit. The proposed biquad filter offers various attractive features such as (1) independent tunable filter parameters (ω_0 and Q), (2) no matching constraints for realization of different filter functions, (3) capability to compensate for PVT (Process Voltage and Temperature) variations, (4) low active and passive sensitivities. The paper is organized as follows: After an introduction section, second section describes CMOS implementation of proposed VDIBA with detailed high frequency analysis. The third section describes voltage mode biquad filters based on proposed VDIBA. The simulation results of proposed circuit and its applications are presented in section four. Section five describes conclusion of work performed.

2 Circuit Design

2.1 Proposed VDIBA Circuit

The VDIBA is basically a combination of differential transconductance stage as first stage and the unity gain inverting voltage buffer as second stage which provides voltage output. The circuit symbol and CMOS implementation of existing circuit [17] are shown in Fig. 1a and b respectively.

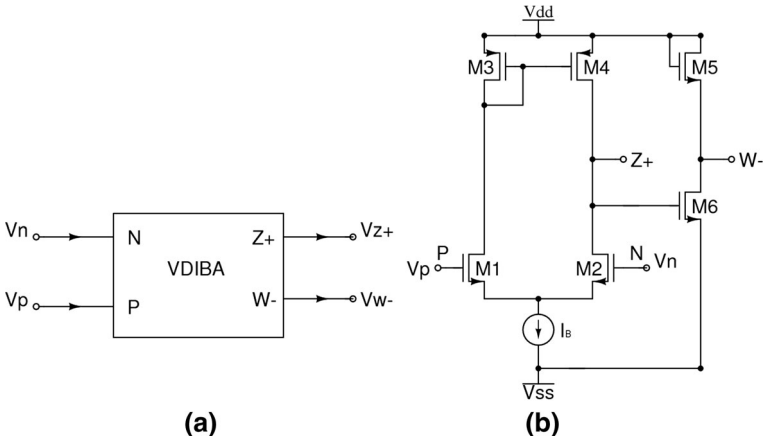

Fig. 1 Voltage differencing inverted buffered amplifier: **a** symbol, **b** existing VDIBA

Using standard notations, characteristics of VDIBA (including non idealities) can be described in following hybrid matrix:

$$\begin{bmatrix} Ip \\ In \\ Iz+ \\ Vw- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ G_m(s) & -G_m(s) & sCz + \dfrac{1}{Rz} & 0 \\ 0 & 0 & -\beta(s) & Rw \end{bmatrix} \begin{bmatrix} Vp \\ Vn \\ Vz+ \\ Iw- \end{bmatrix} \tag{1}$$

where G_m is transconductance of VDIBA and β (ideally unity) represents non ideal voltage gain between ports Z+ and ports W−. The VDIBA has low valued parasitic resistances Rw (ideally zero) at ports W−. It also has large valued parasitic resistances Rz (ideally infinity) in parallel with low valued parasitic capacitances Cz (ideally zero) at ports Z+. The proposed VDIBA is shown in Fig. 2. The first stage consists of transistors M1 and M2 forming input differential pair, transistors M5 and M6 act as active load transistors and transistors M3 and M4 generates negative transconductance (− g_m). It uses cross coupled NMOS transistors between nodes a and b which provide local positive feedback for compensation of positive output conductance of the PMOS load transistors and NMOS differential pair. The advantage of proposed technique is that it does not limits output voltage swing, due to absence of MOSFET diode connected circuit at load side. Furthermore, the resistive compensation technique is used to enhance bandwidth of transconductance stage of proposed circuit [18–20]. An additional advantage of proposed transconductance stage is an inbuilt tuning current (Ic) that can be used for adjusting transconductance (G_m) of proposed VDIBA. The output stage (second stage) of proposed VDIBA is unity gain inverting buffer amplifier with PMOS load (see Fig. 2). Second stage is free from substrate bias effect because of PMOS load.

2.2 High Frequency Analysis of Proposed VDIBA

The small signal high frequency equivalent circuit of the novel transconductance stage (first stage) of the proposed VDIBA is shown in Fig. 3. In high frequency equivalent model g_{mi}, r_{0i}, Gi, Di, Si and C_i denote transconductance, output resistance, gate, drain, source

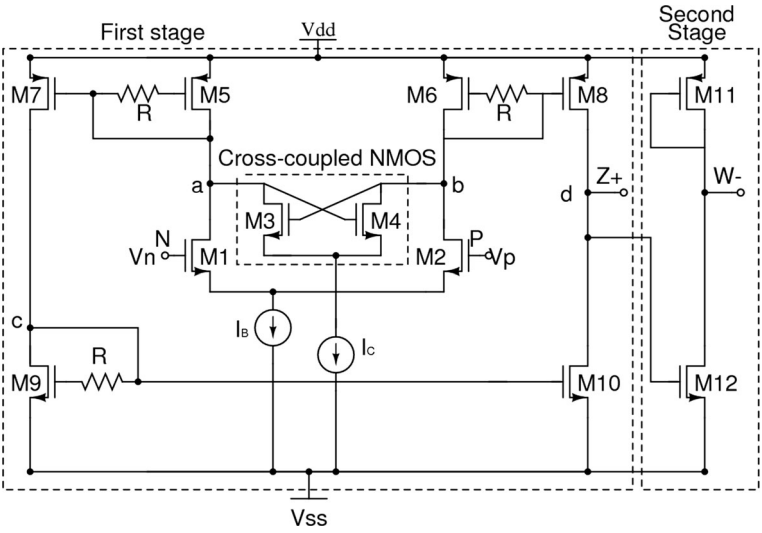

Fig. 2 Circuit diagram of proposed VDIBA

terminals and gate to source capacitance of corresponding MOSFETs Mi respectively (where i = 1–10); Vn and Vp are magnitudes of input voltages applied at gate of transistors M1 and M2.

By using high frequency equivalent model, the short circuit transconductance without compensation resistor R (assume $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$, $g_{m5} = g_{m7}$, $g_{m6} = g_{m8}$, $g_{m7} \approx g_{m9}$, $g_{m9} = g_{m10}$, $C_3 = C_4$, $C_5 = C_6$, $C_7 = C_8$, $C_9 = C_{10}$, $g_{o1} = g_{o2}$, $g_{o3} = g_{o4}$, $g_{o5} = g_{o6}$, $g_{07} = g_{08}$, $g_{09} = g_{010}$) is given by

$$\frac{Iz+}{(Vp - Vn)} = \frac{g_{m1}g_{m5}}{g_{m5} - g_{m3} + g_{01} + g_{03} + g_{05} + sC_4 + sC_5 + sC_7} \tag{2}$$

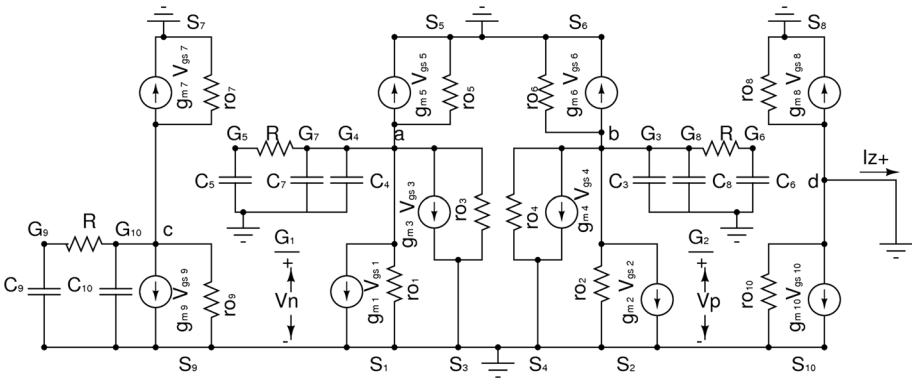

Fig. 3 High frequency equivalent model for transconductance stage of proposed VDIBA

Here $g_o = g_{o1} = g_{o3} = g_{o5}$. Under approximation $g_o << g_m$, Eq. (2) can be simplified as

$$G_m(s) = \frac{Iz+}{(Vp - Vn)} = \frac{g_{m1}g_{m5}}{g_{m5} - g_{m3} + sC_4 + sC_5 + sC_7} \tag{3}$$

It is evident from (3), that differential transconductance gain at low frequency can be expressed as

$$G_m = \frac{g_{m1}g_{m5}}{g_{m5} - g_{m3}} = \frac{g_{m1}}{1 - \frac{g_{m3}}{g_{m5}}} \tag{4}$$

where g_{m3}/g_{m5} is defined as the loop gain factor and its value depends on device sizes of circuit. If loop gain factor g_{m3}/g_{m5} is less than one, amplification is enhanced by gain factor $1/(1 - g_{m3}/g_m)$ which is greater than 1. Note that g_{m3} is fully programmable with tuning current (Ic) which can be useful for compensation of PVT. From (3) it is evident that − 3 dB frequency of transconductance stage of proposed VDIBA (assume $C_{gs} = C_4 = C_5 = C_7$) is given by

$$\omega_{-3\text{ dB}} = \frac{g_{m5} - g_{m3}}{3C_{gs}} = g_{m5}\left(\frac{1 - g_{m3}/g_{m5}}{3C_{gs}}\right) \tag{5}$$

It is clear from (5) that bandwidth of transconductance stage of proposed VDIBA is low. Therefore, for proposed VDIBA, resistive compensation technique of bandwidth extension is used to enhance bandwidth of transconductance stage. Compensation resistors are introduced between gates of MOSFETs M5–M7, M6–M8 and M9–M10 (see Fig. 2). The short circuit transconductance of proposed VDIBA with compensation resistor R is given by

$$G_m = \frac{\frac{g_{m1}g_{m5}}{C_4+C_7}\left(s + \frac{1}{RC_5}\right)}{s^2 + s\left[\frac{C_4+C_5+C_7-g_{m3}RC_5}{RC_5(C_4+C_7)}\right] + \frac{g_{m5}-g_{m3}}{RC_5(C_7+C_4)}} \tag{6}$$

Consider $C_{gs} = C_4 = C_5 = C_7$, Eq. (6) can be written as

$$G_m = \frac{\frac{g_{m1}g_{m5}}{2C_{gs}}\left(s + \frac{1}{RC_{gs}}\right)}{s^2 + s\left[\frac{3-g_{m3}R}{2RC_{gs}}\right] + \frac{g_{m5}(1-g_{m3}/g_{m5})}{2RC_{gs}^2}} \tag{7}$$

However, due to connection of compensation resistor R in proposed circuit, the transfer function G_m becomes second order (see Eq. 7) with one zero and two poles. By choosing $R = 1/g_{m5}$, Eq. (7) can be reduced as

$$G_m = \frac{\frac{g_{m1}g_{m5}}{2C_{gs}}\left(s + \frac{g_{m5}}{C_{gs}}\right)}{\left(s + \frac{g_{m5}}{C_{gs}}\right)\left(s + \frac{g_{m5}(1-g_{m3}/g_{m5})}{2C_{gs}}\right)} \tag{8}$$

The zero in Eq. (8) cancels one of the poles, thereby reducing transfer function to a first order system with bandwidth given by $g_{m5}(1 - g_{m3}/g_{m5})/2C_{gs}$, which is 1.5 times higher than Eq. (5). The input stage consisting of transistors M1–M10 forms the differential transconductance stage which converts differential input voltage into output current (Iz+). The output stage is formed by unity gain inverting buffer amplifier (M11–M12) with PMOS load. The frequency response of output stage (see Fig. 2) is given by [21].

$$\frac{V_{w+}}{V_{z-}} = \frac{g_{m12}}{g_{m11}(1 + s(C_{gs11}/g_{m11}))} \tag{9}$$

From (9) it can be seen that output stage has very high bandwidth. On the other hand bandwidth of transconductance stage (discussed above) is less as compared to output stage which in turn limits bandwidth of VDIBA. Therefore, the bandwidth of proposed VDIBA is mainly decided by bandwidth of transconductance stage only. However, overall bandwidth of proposed VDIBA circuit is increased by using resistor compensation technique.

3 Application Examples

3.1 Proposed Universal Biquad Filter

To describe effectiveness of proposed tunable high performance VDIBA circuit, a voltage mode universal biquad filter has been designed is shown in Fig. 4. The proposed filter can provide five types of standard biquad filter. The routine analysis of circuit (Fig. 4) gives following transfer functions shown in (10)–(14).

$$\text{If } V_1 = \text{Vin},\ V_2 = V_3 = 0,\ \text{then LP: } \frac{Vout}{Vin} = \frac{G_{m1}G_{m2}/C_1C_2}{D(s)} \tag{10}$$

$$\text{If } V_2 = \text{Vin},\ V_1 = V_3 = 0,\ \text{then BP: } \frac{Vout}{Vin} = \frac{-sG_{m2}/C_2}{D(s)} \tag{11}$$

$$\text{If } V_3 = \text{Vin},\ V_1 = V_2 = 0,\ \text{then HP: } \frac{Vout}{Vin} = \frac{-s^2}{D(s)} \tag{12}$$

$$\text{If } V_1 = -V_3 = \text{Vin},\ V_2 = 0,\ \text{then BS: } \frac{Vout}{Vin} = \frac{s^2 + G_{m1}G_{m2}/C_1C_2}{D(s)} \tag{13}$$

$$\text{If } V_1 = V_2 = -V_3 = \text{Vin},\ \text{then AP: } \frac{Vout}{Vin} = \frac{s^2 - sG_{m2}/C_2 + G_{m1}G_{m2}/C_1C_2}{D(s)} \tag{14}$$

where D(s) is characteristic equation and given by

$$D(s) = s^2 + \frac{s}{RC_2} + \frac{G_{m1}G_{m2}}{C_1C_2} \tag{15}$$

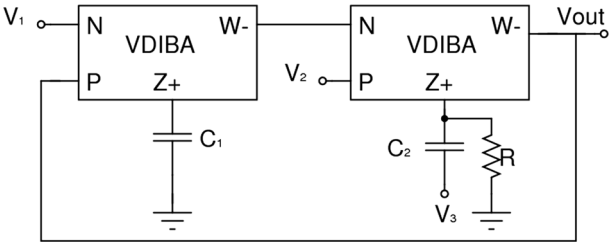

Fig. 4 Circuit diagram of proposed voltage mode universal biquad filter

In Eqs. (10)–(14) G_{m1} and G_{m2} represents transconductance of $VDIBA_1$ and $VDIBA_2$ respectively. The pole frequency ω_0 and quality factor Q can be computed from (15) as follows.

$$\omega_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}}, \quad Q = R\sqrt{\frac{G_{m1}G_{m2}C_2}{C_1}} \tag{16}$$

It can be seen from (16) that Q can be tuned independently by different values resistor R.

Sensitivity analysis of proposed biquad filter with respect to active and passive components may be summarized as

$$S_{G_{m1}}^{\omega_0} = S_{G_{m2}}^{\omega_0} = \frac{1}{2}, \quad S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2}, \quad S_{G_{m1}}^{Q} = S_{G_{m2}}^{Q} = \frac{1}{2}, \quad S_{C_1}^{Q} = -\frac{1}{2}, \quad S_{C_2}^{Q} = \frac{1}{2}, \quad S_R^Q = 1 \tag{17}$$

It is concluded from (17) that the sensitivities of biquad filter are low and it lies within unity magnitude.

3.2 Non Ideal Analysis of Proposed Universal Biquad Filter

Now consider the effect of non ideal parameters of proposed VDIBA from Eq. (1) on biquad filter. As in a non-ideal VDIBA, parasitic capacitance Cz and parasitic resistance Rz appears between high impedance ports Z+ and ground. In proposed biquad filter circuit, parasitic impedances ($Rz_1 \| Cz_1$) and ($Rz_2 \| Cz_2$) appear in parallel with capacitor C_1, C_2 of $VDIBA_1$ and $VDIBA_2$ respectively. Routine analysis of biquad filter (Fig. 5), provides following non ideal transfer function.

$$Vout = \frac{-V_3\beta_2\left[s^2C_2C_1' + sC_2Gz_1\right] - V_2\beta_2G_{m2}\left[sC_1' + Gz_1\right] + V_1\beta_1\beta_2G_{m1}G_{m2}}{s^2C_1'C_2' + s\left[\frac{C_1'}{R} + C_1'Gz_2 + C_2'Gz_1\right] + \beta_1\beta_2G_{m1}G_{m2} + Gz_1Gz_2 + \frac{Gz_1}{R}} \tag{18}$$

In Eq. (18), β_i, G_{mi}, $C_i' = (C_i + Cz_i)$ and $Gz_i = \frac{1}{Rz_i}$ are parameters of ith VDIBA (where i = 1, 2). The parasitic resistances (Rz) are of the order of several KΩs and thus their effect on the performance of biquad filter can be neglected. After neglecting parasitic resistances (Rz), the non ideal ω_0 and Q of the proposed biquad filter can be rewritten as.

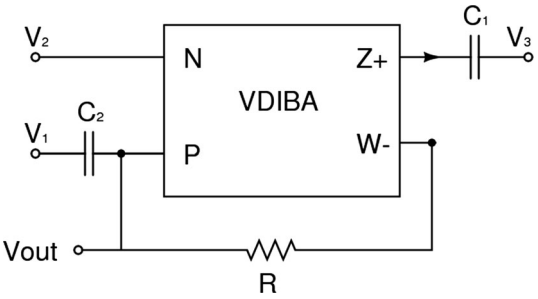

Fig. 5 Circuit diagram of voltage mode universal biquad filter [14]

$$\omega_0 = \sqrt{\frac{\beta_1\beta_2 G_{m1}G_{m2}}{C_1' C_2'}}, \quad Q = R\sqrt{\frac{\beta_1\beta_2 G_{m1}G_{m2}C_2'}{C_1'}} \tag{19}$$

It is clear from characteristic Eq. (19) that the values of ω_0 and Q are slightly modified due to parasitic capacitances. The parasitic capacitances Cz_1 and Cz_2 will be absorbed by external capacitances C_1 and C_2 because their values are very small as compared to external capacitors; hence do not contribute to any unnecessary pole. However, Eq. (19) shows that non ideal voltage gain β also slightly modifies pole frequency ω_0 and quality factor Q of biquad filter. The parasitic resistance Rw is not considered due to its small value. Thus, proposed biquad filter circuit is almost insensitive to non ideal effects. Simulation results of biquad filter based on proposed VDIBA is discussed in the subsequent Sect. 4.

3.3 Voltage-Mode Universal Biquad Filter [14]

The voltage mode universal biquad filter reported in literature [14] has also been designed using proposed VDIBA which is shown in Fig. 5. The simulation result of biquad filter is presented in subsequent Sect. 4.

4 Simulation Results

To verify the theoretical analysis, all circuits are implemented by using TSMC 0.18 μm CMOS process technology and BSIM3 level 49 model devices with DC supply voltage equal to ± 0.6 V. The proposed VDIBA architecture is designed with optimal size to obtain small area, high transconductance, better frequency response and low power dissipation. The biasing of circuit is made in such a manner that all MOSFETs are operating in saturation region. Note that bulk of all NMOS transistors are connected to V_{SS} and all PMOS transistors are connected to V_{DD}. Table 1 shows aspect ratios of MOSFETs used in proposed VDIBA.

The AC response of transconductance stage for proposed VDIBA with compensation resistor R = 4 KΩ for tuning current (Ic) = 100 μA provides bandwidth extension up to 263 MHz at bias current I_B = 150 μA as shown in Fig. 6. Figure 7 shows frequency response of transconductance stage for proposed VDIBA by varying Ic at fixed I_B. The high transconductance (G_m) range of 1.24–10.6 mS can be achieved by varying Ic from 0 to 100 μA at I_B = 150 μA (see Fig. 7a). The low transconductance range of 422 μS–1.24 mS can also be obtained from proposed VDIBA by varying Ic from 0 to 30 μA at

Table 1 Aspect ratios of transistors used in proposed VDIBA

Structures Transistor	Proposed VDIBA W/L (μm)
M1, M2	50/0.36
M3, M4	15/0.36
M5, M6, M7, M8	20/0.36
M9, M10	10/0.36
M11	47/0.18
M12	20/0.18

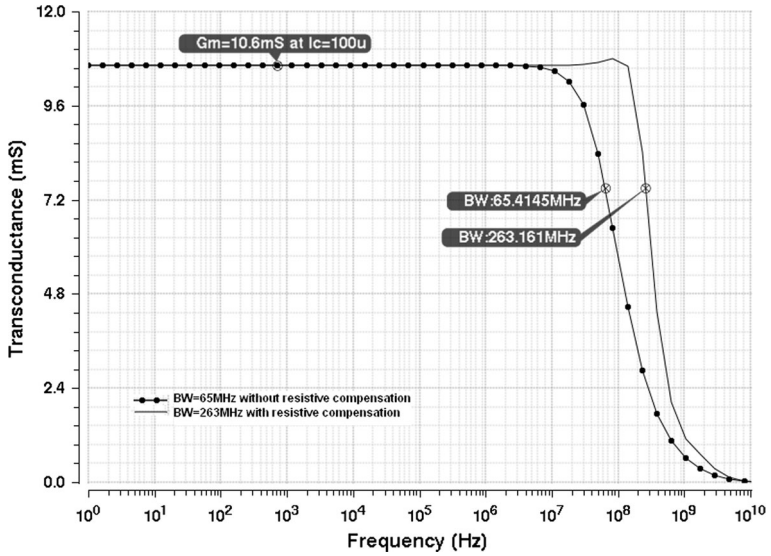

Fig. 6 Transconductance plots of proposed VDIBA

$I_B = 40$ μA (see Fig. 7b). It can be observed from Fig. 7a and b that range of transconductance controllability is wider in proposed VDIBA. Figure 8 shows DC response of transconductance stage for proposed VDIBA circuit. For transconductance stage, maximum range of input voltage without producing significant non-linearity at terminal Z+ is approximately ± 50 mV at Ic = 100 μA. The ac response of second stage for proposed VDIBA is shown in Fig. 9. The non ideal voltage gain (β) of inverting buffer for proposed VDIBA is 1.07 with operating frequency $f_\beta = 3.9$ GHz and transconductance G_m of proposed circuit at Ic = 100 μA is 10.6 mS with operating frequency $f_{Gm} = 263$ MHz. Hence, the operating frequency of proposed VDIBA circuit at Ic = 100 μA is $f_{0\text{-}max} = \{\min (f_{Gm}, f_\beta)\} = 263$ MHz. Figure 10 shows DC response of second stage for proposed VDIBA circuit. The simulation results of proposed VDIBA at bias current $I_B = 150$ μA is summarized in Table 2.

Table 3 shows comparison between performance of proposed VDIBA and other VDIBA/VDBA circuits on basis of transconductance range, power dissipation, bandwidth and supply voltage. It is evident from Table 3, that proposed VDIBA operate at low supply voltage, higher transconductance, and higher bandwidth as compared to other VDIBA/VDBA circuits.

4.1 Simulation Results of Proposed Voltage Mode Universal Biquad Filter

The voltage mode universal biquad filter (Fig. 4) is designed for pole frequency $f_0 = 10.1$ MHz and Q = 1.27 by selecting $G_{m1} = G_{m2} = 1.27$ mS (Ic = 0 μA), external resistances R = 1 KΩ, and external capacitors $C_1 = C_2 = 20$ pF. The simulated magnitude responses of low pass, high pass, band pass, band reject and all pass filter as shown in Figs. 11 and 12 respectively. The tuning of Q for band pass response of proposed biquad filter (Fig. 4) as shown in Fig. 13. It is clear from curves that tuning of Q can be done by varying resistor R. The transient response of biquad filter is measured by applying a sinusoidal input voltage signal with amplitude of 25 mV at 10 MHz frequency. Figure 14

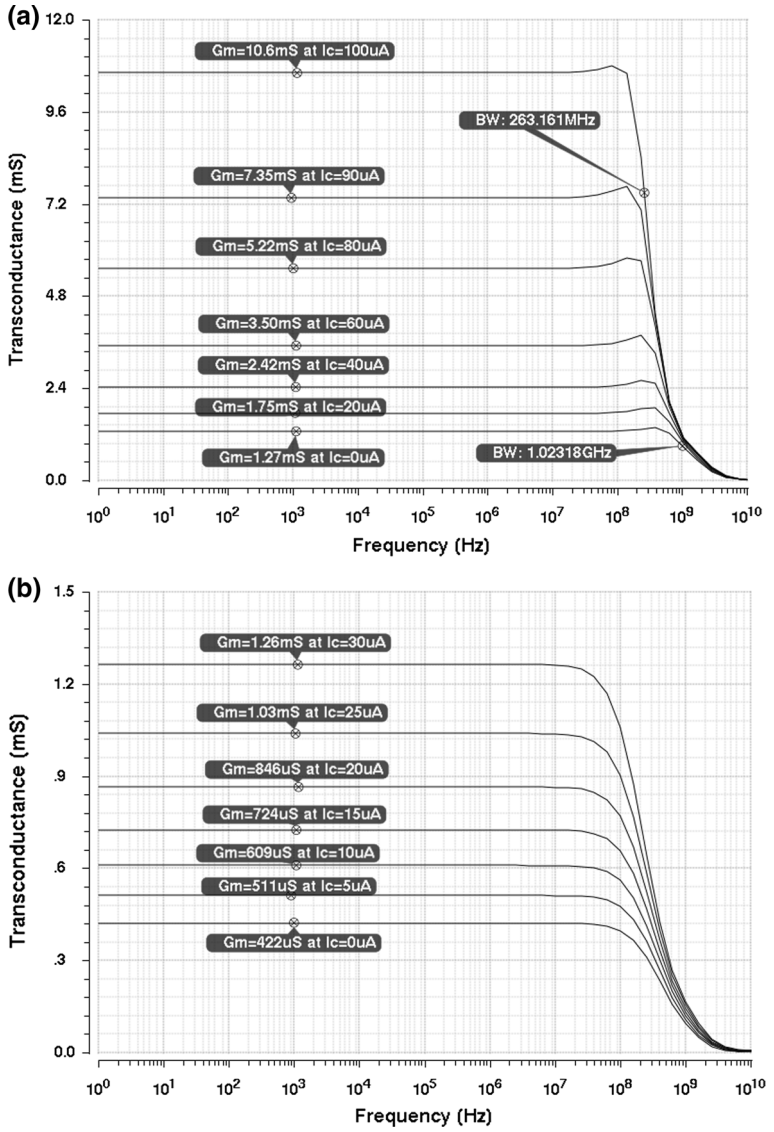

Fig. 7 Frequency response of transconductance stage for different tuning currents (Ic) at **a** bias current (I_B) = 150 μA and **b** bias current (I_B) = 40 μA

shows output signals of band pass response for biquad filter and total harmonic distortion (THD) for output signal is 0.4%. The power dissipation of proposed biquad filter is 1.14 mW. The variation of pole frequency for band pass response is obtained by varying Ic as shown in Fig. 15. The pole frequency is varied for $f_0 \cong$ {10.5; 16.1; 23.8; 38.3; 83.4} MHz via tuning current (Ic) = {0; 25; 50; 75;100} μA respectively.

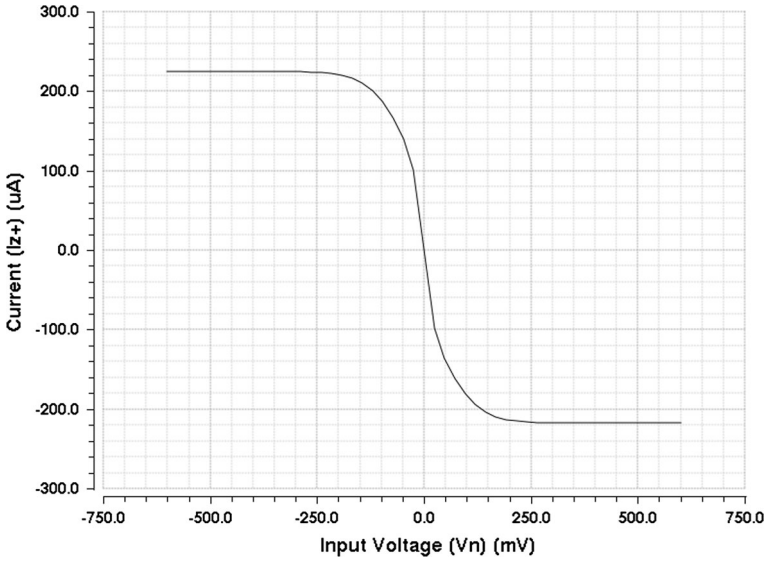

Fig. 8 DC response of transconductance stage for proposed VDIBA

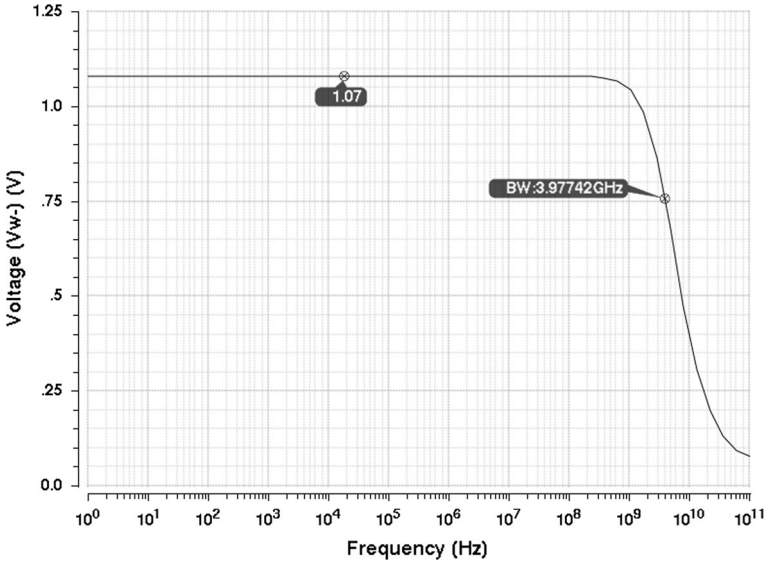

Fig. 9 Frequency response of second stage for proposed VDIBA

4.2 Simulation Results of Existing Universal Biquad Filter [14]

The voltage mode universal biquad filter of Fig. 5 has also been simulated by using both existing VDIBA [17] and proposed VDIBA. The value of passive components are chosen as $C_1 = C_2 = 20$ pF and $R = 1$ KΩ for both cases. The value of transconductance (G_m) for existing VDIBA is 656 μA (at $I_B = 100$ μA) which results in pole frequency of 6 MHz

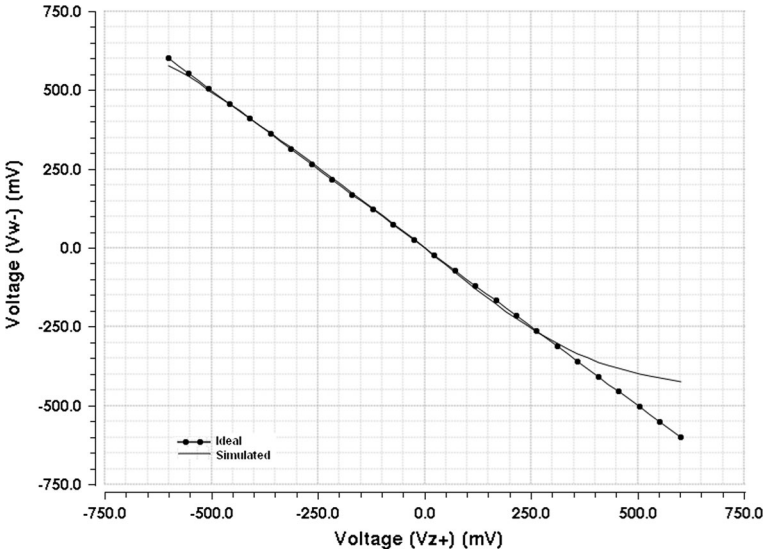

Fig. 10 DC response of second stage for proposed VDIBA

Table 2 The summary of simulation results of proposed VDIBA

Parameters	Proposed VDIBA
Technology	0.18 μm
Supply voltage	± 0.6 V
Tuning current (Ic)	0–100 μA
Transconductance (G_m)	1.27 mS–10.6 mS
Bandwidth of transconductance stage	1 GHz–263 MHz with R = 4 KΩ
Voltage gain of inverter (β)	1.07
DC power dissipation	0.56 mW–0.96 mW

and power dissipation of 8.5 mW. Although, the value of transconductance (G_m) of proposed VDIBA is 4.8 mS (at $I_B = 150$ μA and Ic = 75 μA) which results in pole frequency of 18 MHz and power dissipation of 0.74 mW.

Thus, it can be observed that pole frequency obtained by biquad filter designed with proposed VDIBA is approximately 3 times greater than pole frequency of biquad filter designed using existing VDIBA with power saving of approximately 7.76 mW. Figures 16 and 17 show responses of voltage mode biquad filter designed using proposed VDIBA and existing VDIBA respectively.

Table 3 The comparative results analysis of proposed VDIBA and other VDIBA/VDBA circuits

References	Transconductance (S)	Controlling parameter (μA)	Power dissipation (mW)	Supply voltage (V)	Bandwidth (MHz)	Technology (μm)
Herencsar et al. [17].	656 μ	$I_B = 100$	7.9	± 0.9	226	0.18
Gupta et al. [15].	582 μ	$I_B = 100$	1.5	± 0.75	220	0.18
Sotner et al. [22]	865 μ	$I_B = 100$	–	± 1.2	217	0.18
Proposed work	10.6 m	$I_B = 150$ and Ic = 100	0.96	± 0.6	263	0.18

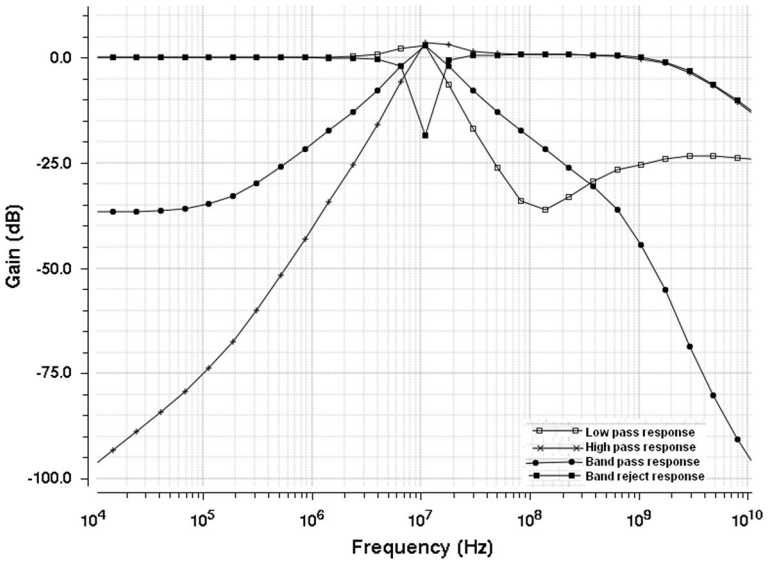

Fig. 11 Frequency response of proposed biquad filter (LP, HP, BP, BR)

5 Conclusions

This paper presents high performance tunable VDIBA based on programmable positive feedback transconductance enhancement and resistive compensation technique. It operates at lower supply voltage and provides high transconductance and consumes low power than other VDIBA/VDBA circuits. The bandwidth of proposed VDIBA is improved by using resistive compensation technique. The transconductance of proposed VDIBA circuit is enhanced up to 10.6 mS with 263 MHz bandwidth. To demonstrate the effectiveness of high performance of proposed circuit, voltage mode universal biquad filters are

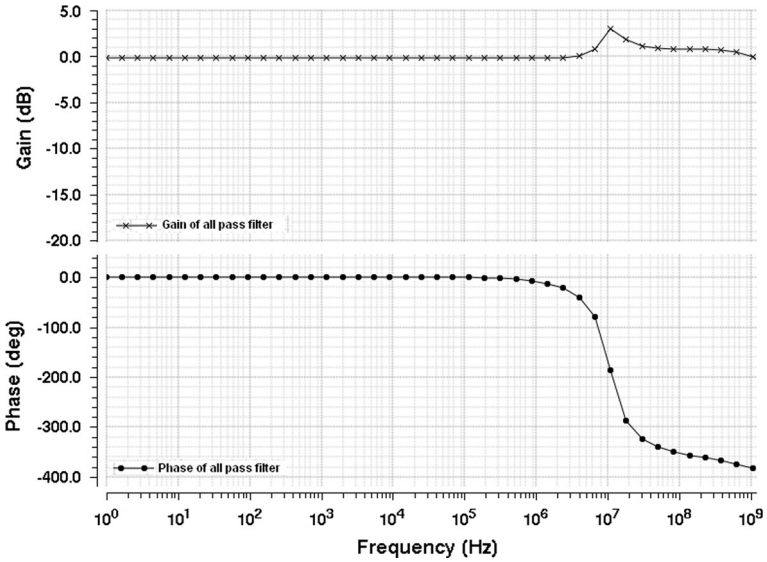

Fig. 12 Frequency response of all pass filter for proposed biquad filter

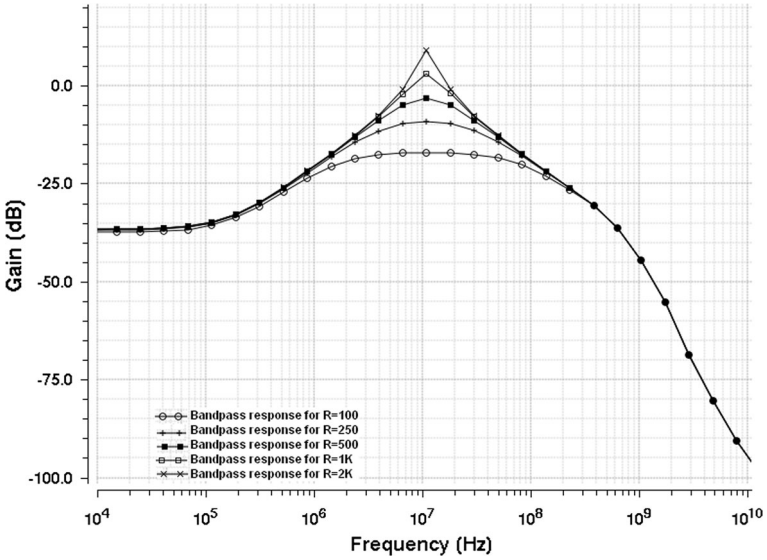

Fig. 13 Frequency response of Band pass filter with different value of resistor R

implemented and simulated. The pole frequency of proposed universal biquad filter is tunable in range of 10.5–83.4 MHz. Therefore, proposed VDIBA circuit may be useful in low voltage low power high performance analog signal processing applications.

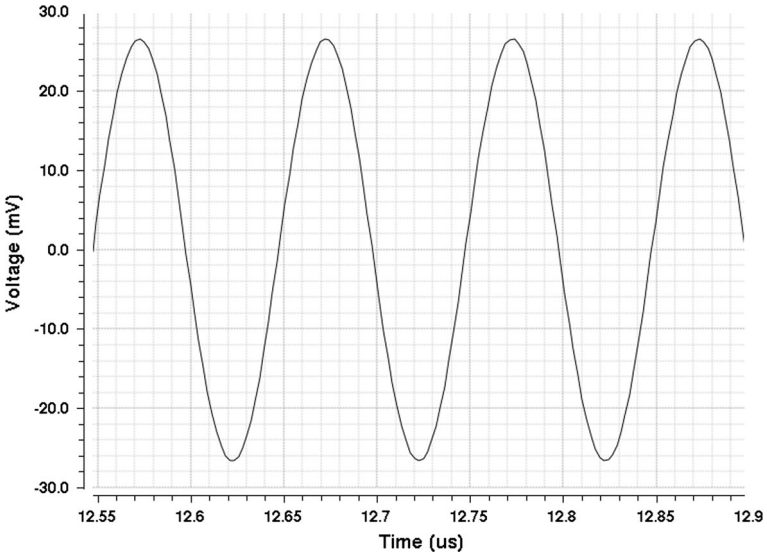

Fig. 14 Transient response of Band pass filter at 10 MHz frequency

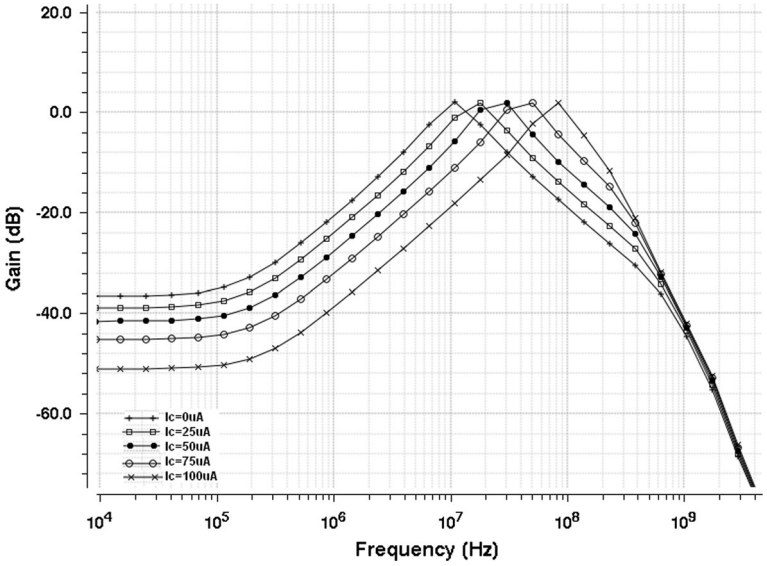

Fig. 15 Pole frequency tuning of Band pass response

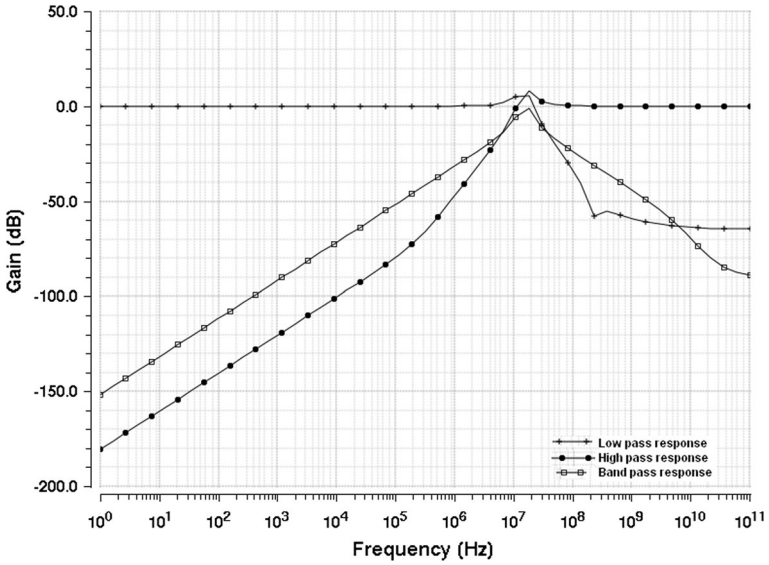

Fig. 16 Response of biquad filter [14] designed using proposed VDIBA

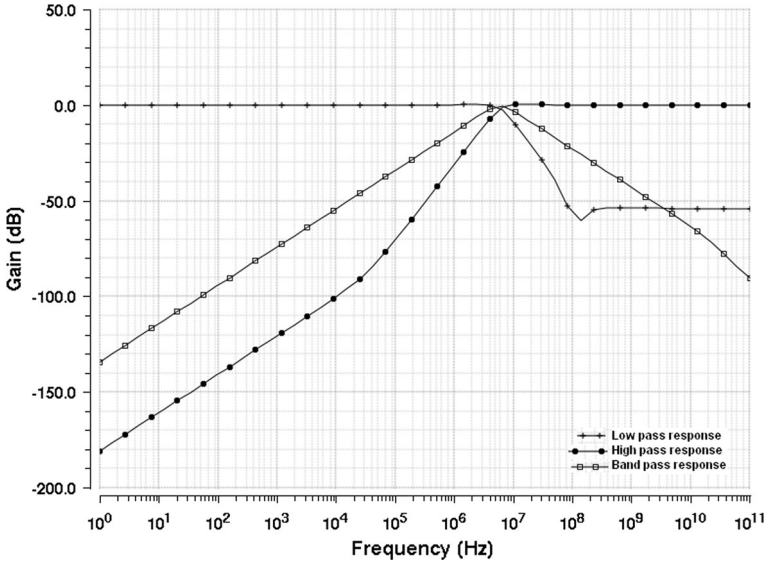

Fig. 17 Response of biquad filter [14] designed using existing VDIBA

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