Wireless Pers Commun (2017) 94:3513–3529
DOI 10.1007/s11277-016-3788-5

A Novel SRAM Cell Design with a Body-Bias Controller Circuit for Low Leakage, High Speed and Improved Stability

Rohit Lorenzo[1] · **Saurabh Chaudhury**[1]

Published online: 29 September 2016

Abstract A dynamic threshold voltage control strategy is presented in this paper to minimize leakage power while enhancing the speed and stability. The threshold voltage of driver and access transistor are tuned dynamically through a novel body-bias controller circuit. The word line signal level controls the action of the proposed body-bias controller. In order to reduce subthreshold leakage current, the threshold voltage of NMOS access and driver transistors are adjusted to a high value by applying a reverse body-bias. On the other hand, forward body-bias lowers the threshold voltage of NMOS access transistor thereby enabling faster read and writes operation. Simulation results shows that the proposed design is much better than conventional and other SRAM cells such as, NC SRAM, PP SRAM, WRE8T. The amount of leakage power reduction is as high as 41.071 % over conventional 6T SRAM cell when tested on (8 × 16) SRAM array. Whereas, the improvement in read and write delay is 30 and 15.81 % respectively.

Keywords SRAM · Leakage power dissipation · Sub threshold leakage current · Word line signal · Body biasing controller · High speed and stability

1 Introduction

Static random access memories (SRAMs) are the integral part of today's electronic systems [1]. It plays a vital role of temporary storage in various digital devices such as, mobile phones, microprocessor, microcontrollers, personal computers and many others. System on chip (SOC) requires both low power consumption and high performance where SRAM

✉ Rohit Lorenzo
rohit.lorenzo@gmail.com

[1] Department of Electrical Engineering, National Institute of Technology Silchar, Silchar, Assam, India

covers a major portion of the total die area as reported in international technology roadmap semiconductor (ITRS) [2].

Supply voltage and device scaling are the most effective ways to achieve low power consumption and high speed in CMOS VLSI circuits [3]. Further, it is possible to attain minimum energy in sub-threshold region as explained in [4]. Again, MOSFET suffers from various short channel effects, which further leads to increase in sensitivity to process variation. Thus, designing in sub-threshold region is a critical design challenge in mobile SOCs [5].

We can expect reduced threshold voltage (V_t), channel length and gate oxide thickness in MOSFET devices today because of continued device scaling [6]. This has consequently led to excessive leakage power consumption. At present leakage power consumption is the dominant contributor of total power consumption in SRAM cells and many other portable digital systems.

However, scaling of supply voltages faces many obstacles such as reduction in read static noise margin (RSNM), write static noise margin (WSNM) and operating speed [7, 8]. Stability in SRAM cell is also caused by the mismatch in V_t of cross-coupled inverter pair [9]. Reduction in supply voltage also reduces SRAM cell current, which consequently decreases the speed of cell. Moreover, power density is a growing concern in today's high performance chip which even demands for thermal-aware design [10].

FD-SOI device has been proposed [11], to solve the static noise margin problem, but its high cost and difficulty in manufacturing limits its use. A variable threshold design of MOSFET is highly desirable in such a situation which can be solved by controlling the bulk potential of a MOSFET device. Bulk voltage in CMOS technology cannot be changed abruptly to a high or a low value because if a reverse body-bias (RBB) is applied across the bulk it may abruptly increase the leakage current in the form of band-to-band tunneling. Again if we forward body-bias (FBB) the bulk of a MOSFET abruptly, then it may cause the latch up current to increase. Consequently it may damage the transistor. So it is important to optimally control the V_t of MOSFET devices for minimum leakage, high speed and good stability. Figure 1 shows the conventional 6T SRAM cell structure which consists of four NMOS transistors and two PMOS transistors. N1, N2 are the two driver

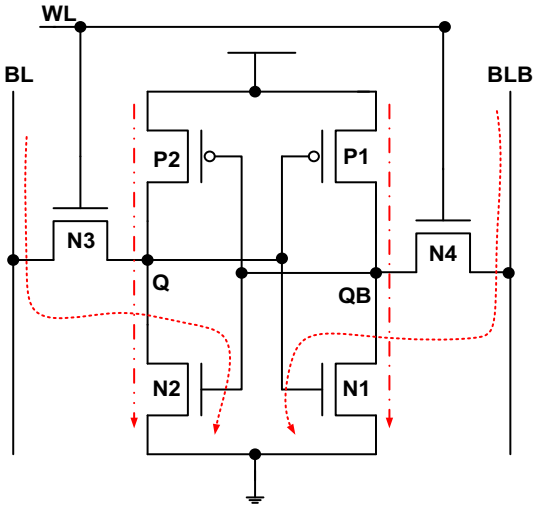


Fig. 1 Leakage path in 6T-SRAM cell

NMOS transistors and N3, N4 are the two access NMOS transistors. Whereas, P1 and P2 are the two PMOS load transistors. As indicated in the Fig. 1, maximum amount of leakage is flowing through the NMOS transistor that is from V_{dd} to ground (dashed line in red) and bitline to ground (dotted line in red). The dominant leakage mechanism in 6T SRAM cell are subthreshold and gate-leakage. Now a days, gate leakage is usually controlled by the use of high K metal gates [12].

As the number of NMOS transistor in SRAM cell is more, so maximum leakage saving is gained by RBB the NMOS transistor during standby mode. The speed of the cell can also be enhanced by FBB the NMOS access transistor (N3 and N4) in active mode. In RBB, V_t of a transistor becomes high and with FBB, V_t of a transistor becomes low. These two performances metric can be achieved by over-driven body-bias [13] which causes the body voltage to move further beyond the supply rail as shown in Fig. 2. High V_t transistors are usually slow and have low subthreshold leakage current. Low V_t transistors on the other hand are fast and have high subthreshold leakage current. The propagation delay (t_{pd}) and sub threshold leakage ($I_{leakage}$) current as given in [14, 15] can be written as,

$$t_{pd} \alpha \frac{C_L V_{dd}}{I_{DS}} = \frac{C_L V_{dd}}{A(V_{dd} - V_t)^2} \tag{1}$$

where C_L is the load capacitance, V_{dd} is the supply voltage, I_{DS} is the drain current in the saturation, V_t is the threshold voltage and A is constant.

$$I_{leakage} = \frac{W}{W_0} I_0 e^{(V_{gs} - V_t)/nV_{th}} = \frac{W}{W_0} I_0 10^{(V_{gs} - V_t)/s} \tag{2}$$

where, $I_0 = \mu C_{ox} \frac{W}{L} V^2 e^{1.8}$, $V_{th} = \frac{KT}{q} = 0.026$ Vμ denotes carrier mobility, C_{ox} is the gate oxide capacitance per unit area, V_{th} is thermal voltage, W is width is the Boltzmann constant, T is the absolute temperature, q is the electrical charge of conduction, n is a constant and $S = nV_{th}$ ln 10 is the sub threshold slope of 100 mV/decade, each 100 mV decrease in V_t will cause an order of magnitude increase in leakage current.

A typical memory organization consists of individual cells arranged in an array of horizontal rows and vertical columns [16]. Based on word line signal, a particular row of the cell is in active mode and others are in standby mode. In this paper, we propose a word-line based controller circuit to operate the SRAM cell in active and standby mode. The word line signal defines the two different body voltages for NMOS transistors in active and standby mode.

The rest of the paper is organized as follows. Section 2 presents the design of the proposed controller. Section 3 analyzes the simulation results of the proposed SRAM cell. Finally, Sect. 4 concludes the paper.

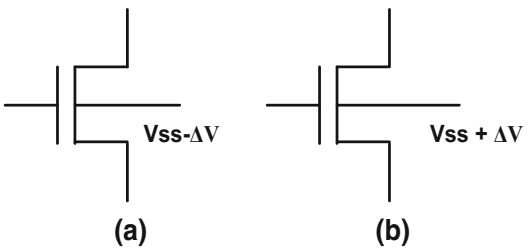


Fig. 2 Body bias voltage of NMOS transistor in **a** standby mode **b** active mode

2 Related Works

In this section, we review some of the previously proposed SRAM cell architectures. Ref. [17] proposes a new architecture termed as NC SRAM cell. The main idea of this cell is the use two pass transistors, NC1 and NC2, which provide different ground levels to the memory cell in the active and idle mode as shown in Fig. 3. In active mode, the source of the driver transistor is connected to the ground. But in the idle mode, the source of the driver transistor is biased positively to raise its voltage above the ground level. This causes the subthreshold leakage current to reduce. This reduction of subthreshold current is because of increase in V_t due to body effect. Again, further reduction of leakage current is due to reduction in the drain-source voltage and consequently due to lower DIBL effect. In this cell, in order to reduce the bit-line leakage, the pass transistors (N3, N4) with higher V_t are used. While, to decrease the leakage currents of NC1 and NC2, their V_t has also been increased. Thus NC-SRAM is able to reduce static power consumption using the virtual ground level technique and increasing the V_t, but it has caused extra dynamic power consumption along with degradation in SNM and performance.

In [18], another cell called PP-SRAM is suggested which uses PMOS access transistors instead of NMOS access transistor in order to reduce gate leakages shown in Fig. 4. Since the mobility of holes is less than the mobility of electrons, so using PMOS transistor it would cause a reduction in timing performance. To compensate this performance reduction, it is necessary to use PMOS transistor whose width is wider than the NMOS transistor. As a result of which it would cause increase in capacity of parasitic capacitors and finally increase in power.

Ref. [19] proposes a write and read enhanced 8T SRAM cell (WRE8T) structure as illustrated in Fig. 5. The beauty of the architecture is that it minimizes the subthreshold leakage current by stacking four transistors (M7-M3-M1-M8). This SRAM cell basically improves the read and writes static power. Further, the read delay in this scheme is also less

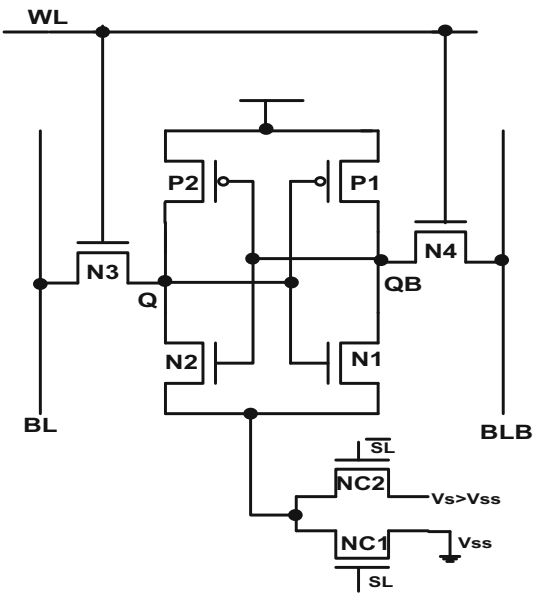


Fig. 3 NC SRAM cell [17]

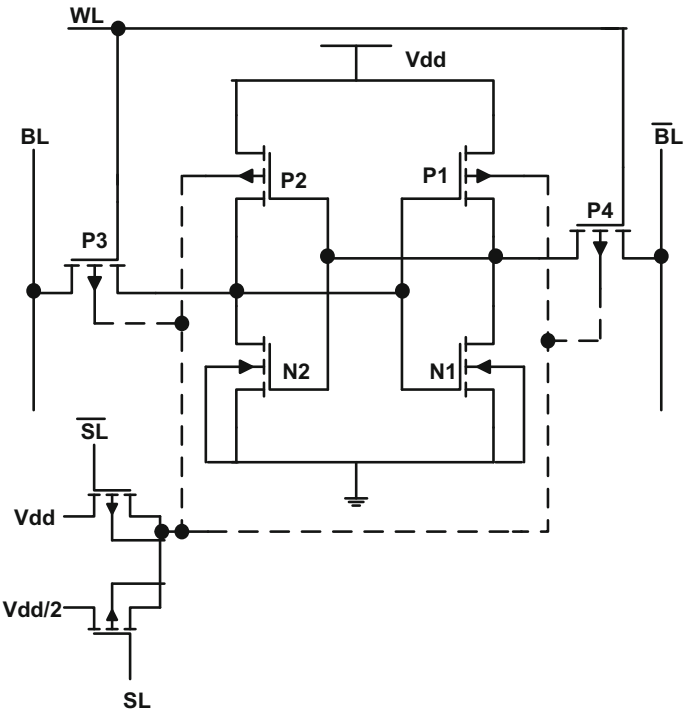
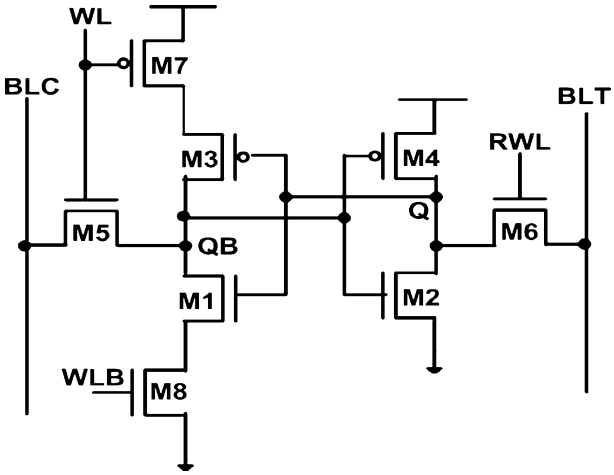


Fig. 4 PP SRAM cell [18]

Fig. 5 WRE8T SRAM [19]



due to single ended read operation. This is because capacitance associated with large drivers are now removed. Write delay however, is higher than the differential SRAM cell due to single ended operation.

3 Proposed Controller Design

This section presents the 6T SRAM cell with the proposed controller circuit. Figure 6a shows the conventional 6T SRAM cell with a provision to accommodate the control signals (marked in red and blue node). The proposed controller circuit is shown in Fig. 6b, c and is designed with a minimum number of transistors which will help in improving the speed during active mode and reduce the leakage power during standby mode.

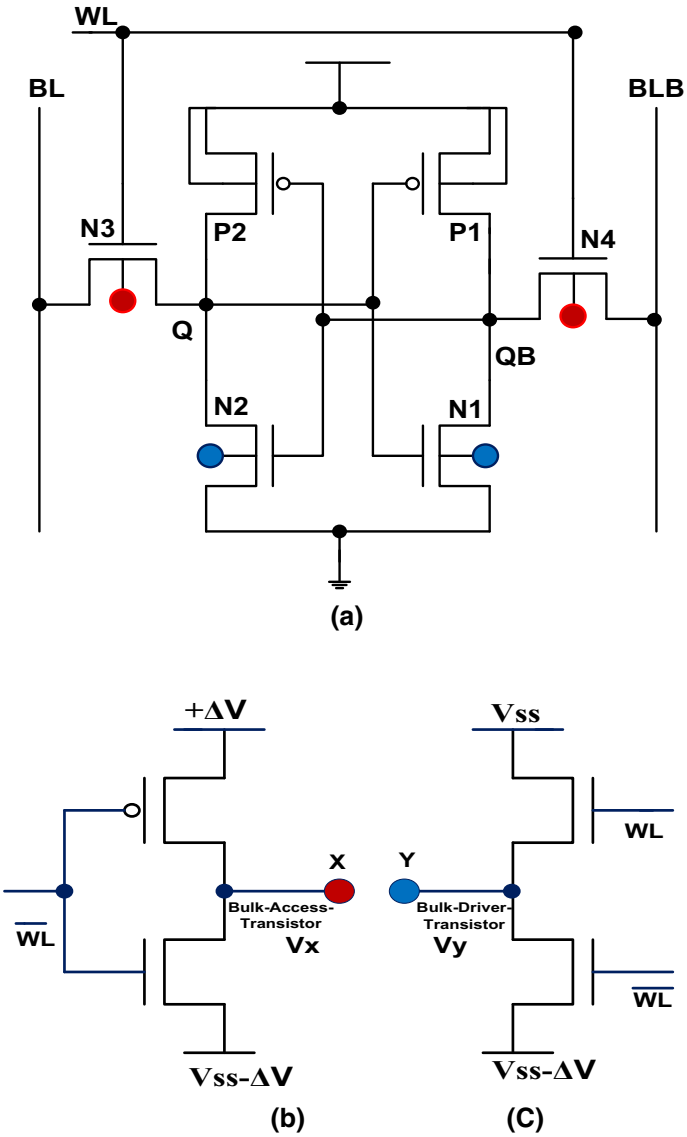


Fig. 6 Proposed body bias controller with SRAM cell

In an array of SRAM cell, the body bias voltage of NMOS access and driver transistor will be controlled by the word line signal levels. To control the leakage power, speed and stability, different voltages levels are required at the body terminal during active and standby mode. In Fig. 6a red node indicates body bias voltage for NMOS-access transistor and blue node indicates body bias voltage for NMOS-driver transistor. In standby mode, word line signal, WL = 0 and as such WL (bar) = 1. The X-node (red node) of body bias controller in Fig. 6b transfers Vss − ΔV to the body of NMOS-access transistor. Similarly, Y node (blue node) in Fig. 6c transfers Vss − ΔVto the body of driver transistor. These body bias voltages will offer a high V_t to both NMOS driver and access transistors, which consequently reduces the leakage current. During active mode, WL = 1 and so WL (Bar) = 0, which enables X-node to transfers small FBB voltage of (+ΔV) to NMOS access transistor and enables Y-node to transfer a voltage Vss = Gnd (i.e. no body-bias) to the body of NMOS driver transistor. The NMOS-access transistor is now FBB which will now offer a low V_t and consequently it will enhance the read/write speed. On the other hand, driver transistor will get no-body bias (because of ground potential to the bulk of NMOS transistor). To avoid the stability problem we are keeping no body bias to the load and driver transistors in active mode becauseV_t variation of driver transistor has the largest impact on the voltage transfer characteristic and as such W/L ratio of driver transistor is large compared to other transistors in a SRAM cell [20]. The combination of SRAM cell and controller circuit provides good operation during active and standby mode. To test the functionality of the circuit we have chosen arbitrarily a FBB of +ΔV = 0.4 V and RBB of Vss − ΔV = −0.23 V, Vss = ground and Vdd = 1 V at 65 nm technology. Depending upon the word line signal level (WL), the controller circuit transfers a voltage to the body of NMOS access transistor, Vx = 0.4 V during active mode (WL = 1) and Vss − ΔV = −0.23 V during standby mode (WL = 0). Similarly, for NMOS driver transistor, the control circuit transfers a voltage to the body terminal.

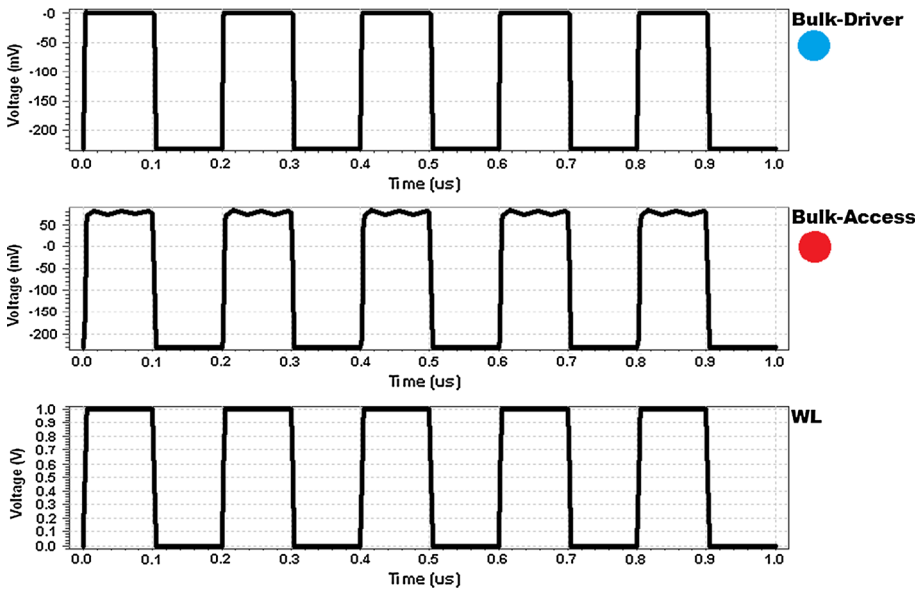


Fig. 7 Control circuit signal to the body of access and driver NMOS transistors

Vss = ground (0 V) during active mode and Vss − ΔV = −0.23 V during standby mode. Based on these values the simulated waveform of the control circuit is shown in Fig. 7. Array structure with the proposed controller is shown in Fig. 8. The control lines from the controller circuit are indicated in blue and red lines, which are shared by the row of cells.

4 Results and Discussion

To verify the proposed design, extensive simulations with Tanner EDA tool using a 65 nm predictive technology model (PTM) [21] were performed. The performance of the proposed SRAM cell then compared with conventional (6T), NC SRAM, PP SRAM and WRE8T SRAM cells taking 1 V as power supply.

4.1 Static Power Dissipation

Static power dissipation of the circuit is measured during standby mode (when WL = 0). In standby mode, bit line pairs are charged and word line signal level is zero which turns-OFF the access transistors. The driver and access transistors are over driven by applying a RBB of Vss − ΔV to the body of NMOS transistor. In this way V_t of the NMOS transistors (driver and access) is raised to a high value, which will reduce the leakage current in SRAM cell. Table 1, shows the simulated values of static power dissipation with a wide variation in RBB voltage which are indicated as Vx and Vy values. Form the table, it is clear that the proposed design substantially reduces the static power dissipation when

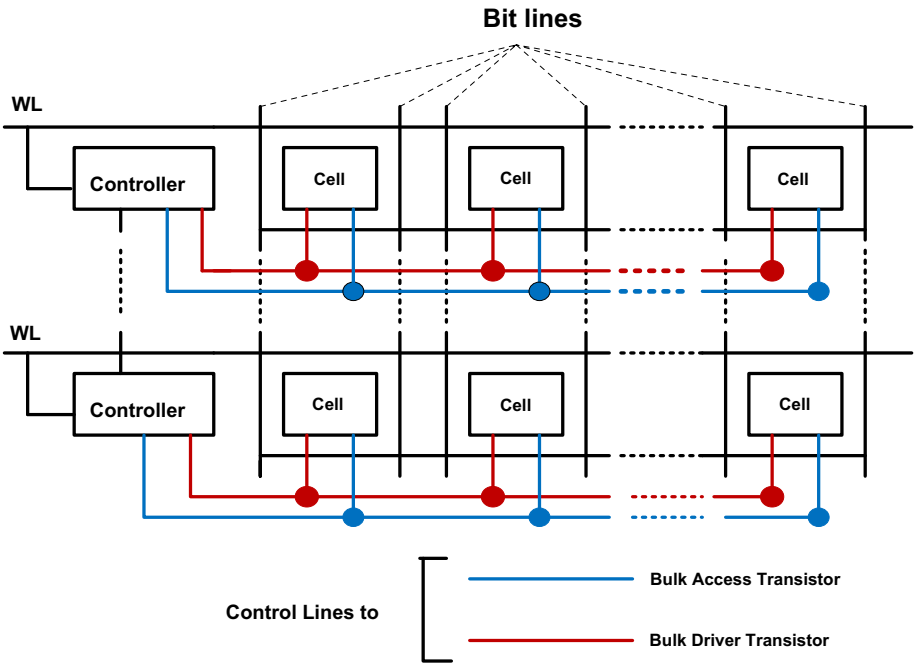


Fig. 8 Array structure of proposed design

Table 1 Static power dissipation

SRAM cells	Static power (W)	% Saving
8 × 16 Array = 128 cells (27 °C)		
Conventional 6T	0.001978	–
Proposed design at body bias		
Vx and Vy =		
−0.1 V	0.0016846	14.833
−0.16 V	0.0015998	19.122
−0.23 V	0.0015055	23.887
−0.28 V	0.0014412	27.133
−0.32 V	0.0013915	29.651
−0.36 V	0.0013433	32.087
−0.41 V	0.0012859	34.989
−0.45 V	0.0011656	41.071

Vx = Vy = Vss − ΔV = −0.45 V, which is about 41.071 % in an 8 × 16 array. The static power dissipation of proposed design is also compared with all other designs referred earlier and is represented as bar-chart in Fig. 9. From the figure, we can observe that proposed design gives better reduction than all other designs at different body bias voltages.

Static power dissipation is also a function of temperature. Comparison of static power for the proposed and conventional SRAM cell at different temperature is shown in Fig. 10. For simulation purposes, we have limited the reverse body-bias voltages up to −0.45 V. Beyond this voltage level the static power values come out to be erratic probably because of excessive tunneling which has been verified experimentally in [22]. Similarly, Fig. 11 shows the comparison of proposed and conventional SRAM cell at different process conditions.

4.2 Read and Write Delay

Read and write delay of SRAM cell is calculated when the word line signal gets activated (i.e. WL = 1). In the architecture of proposed SRAM cell as shown in Figs. 6 and 8, the

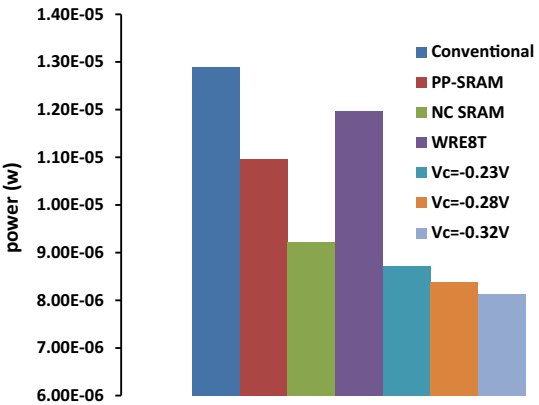


Fig. 9 Comparison of static power dissipation in standby mode

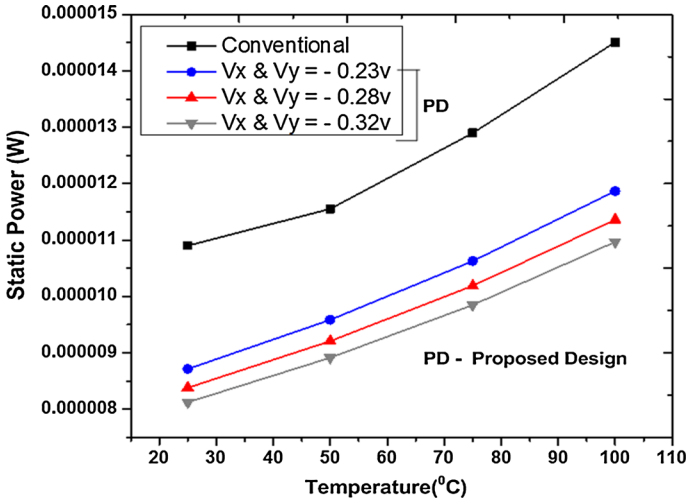


Fig. 10 Static power consumption of proposed and conventional cell at different temperature

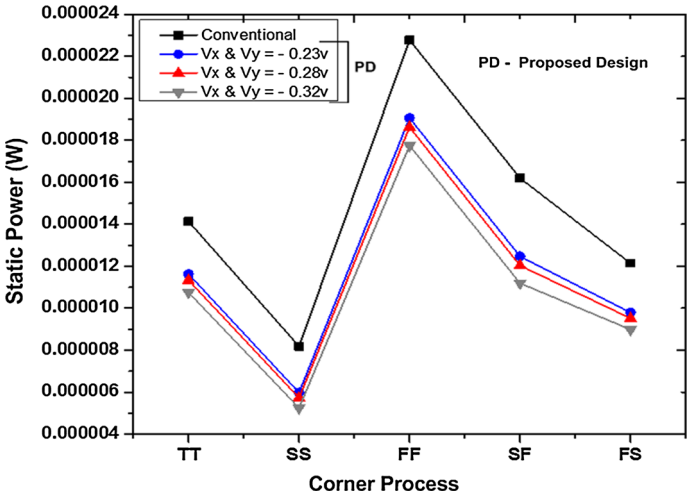


Fig. 11 Static power consumption at different process condition

control circuit transfers a small forward bias of Vx = +ΔV through X node (red node) to the body of NMOS-access transistor.

This Vx will lower the V_t of NMOS access transistor thus enhancing the read and write speed. On the other hand, Y node (blue node) is supplied with Vy = Vss (ground) to the body of NMOS driver transistor keeping the transistor in no-body bias (means body voltage to ground) state.

Read and write delay of the circuit is calculated over some range of FBB from Vx = 0.3 V to 0.5 V. Table 2 shows the result of simulation for read and write delay. It

Table 2 Comparison of read/write performance

SRAM	Read delay (s)	% Reduction	Write delay (s)	% Reduction
6T	2.30E−11	–	3.54E−11	–
Proposed design at body bias				
Vx = 0.3 V	1.98E−11	13.91	3.26E−11	7.909
Vx = 0.4 V	1.75E−11	23.91	3.11E−11	12.14
Vx = 0.5 V	1.61E−11	30	2.98E−11	15.81

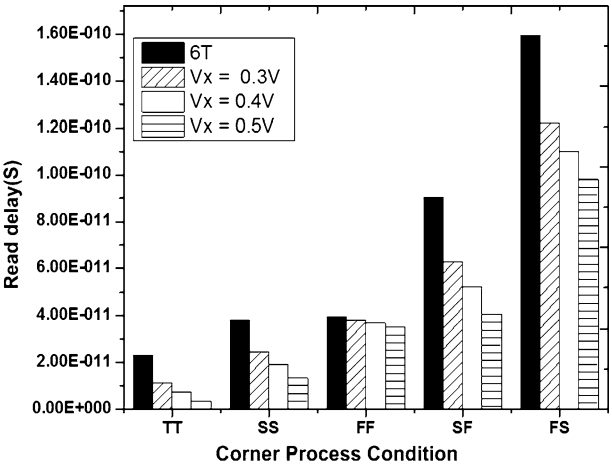


Fig. 12 Read delay at different process condition

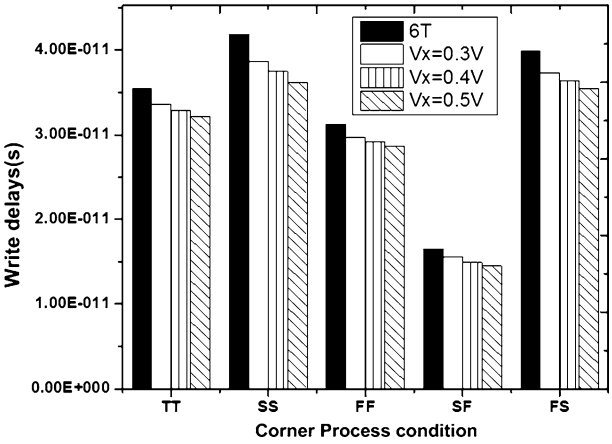


Fig. 13 Write delay at different process condition

can be seen that the proposed design gives a better read and write performance over conventional 6T SRAM cell at different process corners as shown in the bar diagram of Figs. 12 and 13.

In the structure of NC SRAM cell which uses high V_t pass transistor, the voltage level of the ground increases. This causes the read and write performance to degrade. In PP-SRAM, the read and write performance is enhanced by reducing the V_t of PMOS transistor through S and Sbar signals. In case of WRE8T, write operation is single ended, so write delay is more than differential write operation. On the other hand, the single ended read operation leads to decreased in read delay. This is because capacitance related to large write drivers are removed from bit lines during read operation.

Figure 14 and 15 shows the comparison of read and write delay. Simulation shows that a better read and write performance can be obtained as we go on increasing the FBB (Vx). Further, it is seen that the proposed design could achieve a read delay reduction of 30 % and write delay reduction of 15.81 % over conventional 6T SRAM cell through the use of body bias controller.

4.3 Static Noise Margin

Static noise margin is determined by the side length of smaller square as illustrated in Fig. 16. SNM is highly dependent on the β ratio in SRAM cell. The β ratio of conventional 6T and proposed SRAM cell is taken as 1.8. So, W/L ratio of driver transistor is large compared to all other transistors in SRAM cell. The simulated butterfly curve for static noise margin (SNM) during read operation is shown in Fig. 16.

During active mode, the V_t of driver transistor remains unchanged, because V_t variation has the largest impact on voltage transfer characteristic in SRAM cell. Thus the body of driver transistor is tied to Vss (ground), hence there is no body bias.

But to reduce the read and write delay, the V_t of access transistor is decreased by applying a FBB, $Vx = +\Delta V$. This reduction in V_t of access transistor has a negative impact on read SNM. Consequently, stability is little degraded during read operation when Vx is gradually changed. From the plot of read SNM in Fig. 16 we can observe that as we gradually increase the FBB of access transistor, the read stability decreases which can be observed from the Table 3.

Writing in SRAM cell takes place, when the bitline pairs (BL and BL bar) are set with V_{DD} and 0 V respectively. The write operation can be carried out successfully, when access transistor and write driver win the fight with the PMOS pull-up transistor inside the

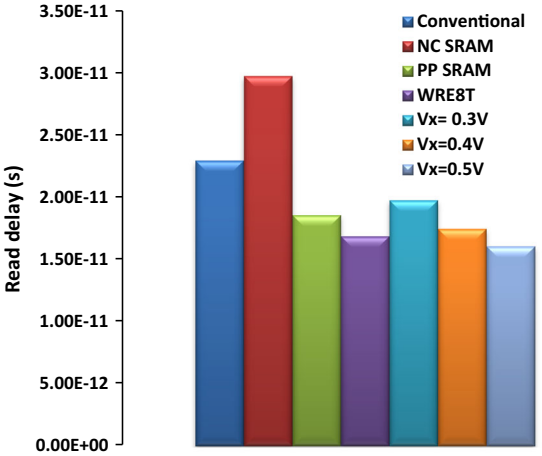


Fig. 14 Comparison of read delay

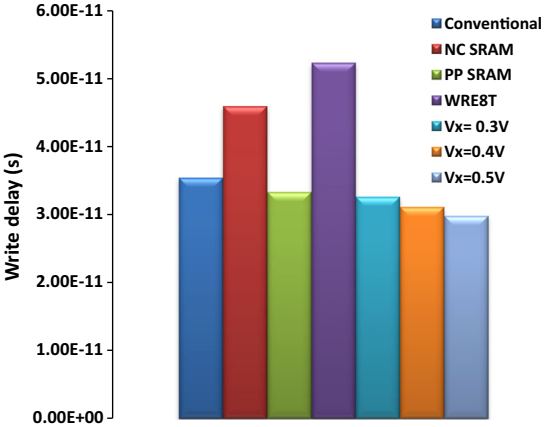


Fig. 15 Comparison of write delay

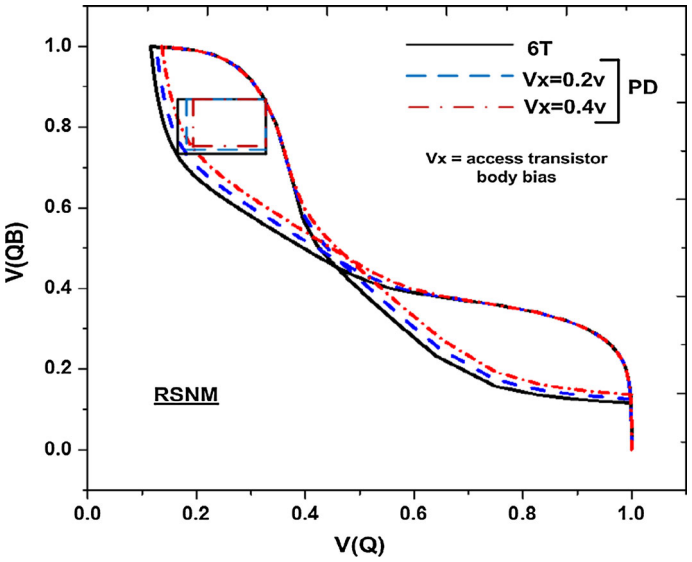


Fig. 16 Static noise margin during read operation

Table 3 Read and write SNM of conventional 6T and proposed design

SRAM cell	RSNM (mV)	% Penalty	WSNM (mV)	% Improvement
6T	162.32	–	240.71	–
Proposed design at				
Vx = 0.2 V	156.26	−3.7	268.18	10.2
Vx = 0.4 V	145.82	−10.1	282.13	14.6
Vx = 0.5 V	142.06	−14.2	296.23	18.7

cell. An improved noise margin is achieved in the proposed SRAM cell because of the reduction in V_t of accessed transistor. From Table 3 we can observe that the improvement in write margin is about 18.70 % at Vx = 0.5 V.

Butterfly curve of hold static noise margin (HSNM) of conventional 6T and proposed SRAM cell during standby mode is shown in Fig. 17. In this mode, V_t of all transistors are high, which causes less leakage current to flow, so the static noise margin is improved. As the body bias voltage Vx and Vy of proposed cell increases, voltage transfer characteristic curve is expanded and the size of the butterfly lobe increases which means a better HSNM. Table 4 shows an improvement of 29.9 % in hold static noise margin at Vx = Vy = −0.32 V as compared to conventional 6T SRAM cell.

4.4 Dynamic Power dissipation

Dynamic power is calculated during active mode, so to calculate the same, access transistors of both the conventional and proposed cell need to be turned ON. Table 5 shows the comparison of dynamic power in case of conventional 6T and proposed SRAM cell. In the

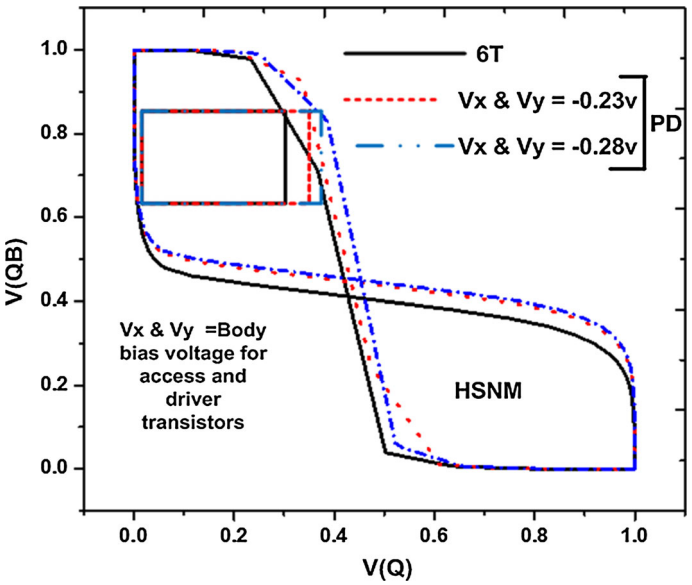


Fig. 17 Static noise margin during standby operation

Table 4 Hold SNM of conventional 6T and Proposed design

SRAM cell	HSNM (mv)	% Improvement
6T	356.5	–
Proposed design		
Vx and Vy = −0.23 V	424.9	16.09
Vx and Vy = −0.28 V	460.6	22.6
Vx and Vy = −0.32 V	508.6	29.9

Table 5 Dynamic power dissipation (active mode at WL = 1)

SRAM cell	Dynamic power (W)	% Penalty
8 × 16 array		
6T	0.003432	–
Proposed design at		
Vx = 0.2 V	0.003521	−2.527
Vx = 0.4 V	0.003669	−6.905
Vx = 0.5 V	0.003721	−7.766

Fig. 18 Layout photo of 8 × 16 SRAM with proposed controller circuit

proposed SRAM cell architecture, each row of SRAM cell is connected to the control circuit. Moreover, the bulk of each transistor of SRAM cell is connected to an appropriate control signal. Charging/discharging of capacitances with respect to control signals activity and variation of V_t with the proposed controller leads to increase in dynamic power dissipation of the proposed cell as compared to conventional 6T SRAM cell. Table 5 shows the dynamic power dissipation of 8 × 16 SRAM array. From the table, we can conclude that increase in dynamic power is negligibly small with the proposed design even for large arrays as compared to conventional SRAM array.

4.5 Layout

The layout of a 8 × 16 SRAM array architecture is shown in Fig. 18. The layout of proposed SRAM cell is generated using L-EDIT environment in Tanner EDA tool. Although it causes some extra area overhead due to controller circuit, but it is least concern in nanometer regime, which can be further reduced by using common controller for multiple bit SRAM cells.

5 Conclusion

Leakage power, speed and stability are the critical issues in SRAM design. In this paper, a novel controller circuit is introduced, whose functioning is based on word line signal level. This control circuit minimizes the leakage power, reducing the delay and improves the stability by controlling the V_t of NMOS driver and access transistors of SRAM cell. In standby mode, static power consumption of 8 × 16 array is reduced by about 41.07 % and the read and write delay is enhanced by 30 and 15.8 % respectively. The cell also exhibits higher HSNM and WSNM of 29.9 and 18.7 % respectively by the variation of V_t.

Furthermore, with proposed design, the amount of dynamic power penalty is about 7.76 % in 8 × 16 array whereas, the penalty in read stability is about 14.2 %. This can be considered to be in acceptable range. We have also verified the effectiveness of the proposed SRAM cell, under various process, voltage and temperature variations using 65 nm technology. The results are found to be very promising.

References

1. Prince, B. (1991). *Semiconductor memories*. New York: Wiley.
2. International Technology Roadmap for Semiconductors. (2012). http://www.itrs.net/Links/2012ITRS/Home2012.htm.
3. Yamaoka, M., & Kawahara, T. (2007). Operating-margin-improved SRAM with column-at-a-time body-bias control technique. In *Proceedings of the european solid-state circuits conference (ESSCIRC)* (pp. 396–399).
4. Yang, Y., Park, J., Song, S. C., Wang, J., Yeap, G., & Jung, S. O. (2015). Single-ended 9T SRAM cell for near-threshold voltage operation with enhanced read performance in 22-nm FinFET technology. *IEEE Transaction on Very Large Scale Integration, 23*(11), 2748–2752.
5. Dreslinski, R. G., Wieckowski, M., Blaauw, D., Sylvester, D., & Mudge, T. (2010). Near-threshold computing: reclaiming Moore's law through energy efficient integrated circuits. *Proceedings IEEE, 98*(2), 253–266.
6. Sinha, S., & Chaudhury, S. (2013). Impact of oxide thickness on gate capacitance—A comprehensive analysis on MOSFET, nanowire FET, and CNTFET devices. *IEEE Transaction on Nanotechnology, 12*(6), 958–965.
7. Seevinck, E., List, F. J., & Lohstroh, J. (1987). Static noise margin analysis of MOS SRAM cells. *IEEE Journal of Solid State Circuits, 22*(5), 748–754.
8. Takeda, K., Ikeda, H., Hagihara, Y., Nomura, M., & Kobatake, H. (2006). Redefinition of write margin for next-generation SRAM and write-margin monitoring circuit. In *Proceedings international solid-state circuits conference* (pp. 630–631).
9. Calhoun, B. H., & Chandrakasan, A. (2005). Analysing static noise margin for sub-threshold SRAM in 65 nm CMOS. In *Proceedings ESSCIRC* (pp. 363–366).
10. Chaudhury, S., Sistla, K. T., & Chattopadhyay, S. (2009). Genetic algorithm based FSM synthesis with area and power trade-offs. *Proceedings Integration the VLSI Journal, Elsevier, 42*(3), 376–384.
11. Yamaoka, M., Maeda, N., Shinozaki, Y., Shimazaki, Y., Nii, K., & Shimada, S., et al. (2005). Low-power embedded SRAM modules with expanded margins for writing. In *Proceedings ISSCC* (pp. 480–611).
12. Nho, H., Kolar, P., Hamzaoglu, F., Wang, Y., Karl, E., & Ng, Y. G., et al. (2010). A 32 nm high-k metal gate SRAM with adaptive dynamic stability enhancement for low-voltage operation. In *Proceedings IEEE international solid-state circuits conference (ISSCC)* (pp. 346–347).
13. Ananthan, H., Kim, C. H., & Roy, K. (2004). Larger than—Vdd forward body bias in sub-0.5v nanoscale CMOS. In *Proceedings ISLPED* (pp. 8–13).
14. Kao, J. T., & Chandrakasen, A. (2000). Dual-threshold voltage techniques for low-power digital circuits. *IEEE Journal of Solid State Circuits, 7*(35), 1009–1018.
15. Kao, J., Chandrakasan, A., & Antoniadis, D. (1997). Transistor sizing issues and tool for multi-threshold CMOS technology. In *Proceedings of design automation conference* (pp. 409–414).
16. Kang, S., & Leblebici, Y. (2003). *CMOS digital integrated circuits*. New York: Mc-Graw hill.
17. Elakkumanan, P., Thondapu, C., & Sridhar, R. (2004). A gate leakage reduction strategy for sub-70 nm memory circuit in implementation of high performance circuits. In *Proceedings of the IEEE dallas/CAS workshop* (pp. 145–148) Texas.
18. Razavipour, G., Afzali-Kusha, A., & Pedram, M. (2009). Design and analysis of two low-power SRAM cell structures. *IEEE Transactions on Very Large Scale Integration Systems, 10*(17), 1551–1555.
19. Pasendiand, G., & Fakhraie, S. M. (2014). An 8T low voltage and low leakage half selection disturb free SRAM using Bulk-CMOS and FinFETs. *IEEE Transactions Electron Devices, 7*(61), 2357–2363.
20. Pavlov, A., Sachdev, M., & Pineda de Gyvez, J. (2004). An SRAM weak cell fault model and a DFT technique with a programmable detection threshold. In *Proceedings* of *ITC international test conference* (pp. 1006–1015).
21. http://ptm.asu.edu/.

22. Srivastava, A., & Zang, C. (2008). An adaptive body bias generator for low voltage CMOS VLSI circuits. *International Journal of Distributed Sensor Networks, 4*, 213–222.

Rohit Lorenzo received the B.Tech degree in electronics and communication engineering from U.P Technical University, Lucknow, India, in 2006 and the M.E degree in VLSI design from Karunya University, Coimbatore, India, in 2008. He is currently working toward the Ph.D degree under the guidance of Dr. S. Chaudhury in the department of Electrical engineering, NIT Silchar, India. During 2008–2010, he was a Assistant professor at Invertis University, Barielly, India and from 2011 to 2012 he work as a Assistant professor on contract at NIT Kurukshetra, India. His research interest include low power VLSI design, synthesis, leakage power minimization, and digital VLSI design. He is reviewer of international journal of electronics (Taylor and Francis). He is a member of IEEE.

Saurabh Chaudhury was born in 1971 silchar, India and graduated in Electrical Engineering Regional Engineering College (Now NIT) Silchar in 1994 and subsequently obtained his M.Tech and Ph.D in the field of microelectronics and VLSI Design from IIT Kharagpur in 2001 and 2009 respectively through QIP Scheme of Government of India. He has joined REC Silchar (Now NIT Silchar) in 1997 as a Lecturer and currently he is holding the post of Associate Professor. He is a member of IEEE and reviewer of many international journals and conferences. His research interests include Low power VLSI design, synthesis, leakage minimization, carbonnanotube based FET devices and circuits, Digital Signal and Image Processing.