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Optimized Threshold Voltage Variation for Tunable Body Biasing CMOS Power Amplifier

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Abstract In this work, variation in threshold voltage is optimized for tunable body biasing CMOS power amplifier (PA). A two stage tunable biasing circuit is designed and integrated with class AB PA which improves variability in threshold voltage. Three most popular materials gallium arsenide, silicon and gallium nitride with two predictive technology model of 65 and 45 nm are employed for the analysis of threshold voltage optimization. A conventional single stage of tunable body biasing class AB PA is compared with a proposed PA of two stages. This concept demonstrates that threshold voltage variation can be lowered further if body biasing circuit is employed on the subsequent higher stages. The adaptive two stage body biasing design with class AB PA is analyzed with derived analytical equations. The calculated results shows gallium arsenide offers minimum variability in threshold voltage as compared to silicon and gallium nitride. Additionally, this class AB PA topology is simulated and fabricated for silicon material

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using 45 nm CMOS technology. The simulation results improve the robustness of the circuit in terms of performance parameters. S-parameter analysis is done that gives good agreement between simulated and measured results.

Keywords Tunable body biasing · Power amplifier (PA) · Variability · Threshold voltage optimization

1 Introduction

In preceding years, a continuous miniaturization of complementary metal oxide semiconductor (CMOS) technologies in nanometer scale is facing many reliability and degradation issues. Designer needs to pay more attention towards circuit design that are reliable and insensitive to the transistor parameter degradation. The resilient biasing technique aims to design reliable circuits that are capable of post process adjustment and insensitive to the transistor parameter degradation over long term stress effect [1, 2]. Random doping fluctuation is one of the most important fluctuation sources for threshold voltage. Due to random doping profile, the fluctuation of threshold voltage is expected to be larger [3]. Threshold voltage variation is inherent to the property of CMOS. The sensitivity of the threshold voltage variations in the critical dimensions is greater due to increasing shorter channel effects as the gate length is reduced using CMOS technology. The resilient or body bias technique dynamically changes the threshold voltage by varying voltage of the body terminal which depends upon the substrate materials as well as technology scaling. In the development of different device technologies or different semiconductor materials, much research has been investigated on threshold voltage variation. It is found that one of the most popular materials that is silicon (Si) for which variation in sensitivity of V_T is more as compared to other materials. Gallium Arsenide (GaAS) based MOS devices has advantages over silicon [4] based devices are of its high electron mobility, larger band gap, high critical field etc. which dominates towards the sensitivity of threshold variations. Additionally, gallium nitride (GaN) material also plays vital role as compared to Si and GaAs. But GaN material based parameters are more sensitive to external bias i.e. body potential which directly affects the threshold parameter of devices. A GaAs FET power switching performance with competing silicon devices (MOSFETs, FCTs, GTOs, and bipolar transistors) indicates that the GaAs FET will have better switching efficiency at all operating frequencies [5].

In [6], authors used adaptive gate biasing scheme to compensate the drain current in MOS circuits that is less sensitive to a threshold voltage and mobility degradation for radio frequency power amplifier design for reliability. In [7], authors from Intel argue that process variation is not an "insurmountable barrier" to Moore's Law, but is simply another challenge to be overcome. Random doping fluctuation, oxide thickness variation and line edge roughness result in significant threshold voltage variation of CMOS transistors at the 45-nm technology node and below in [8–11]. In [12], adaptive substrate biasing scheme is used for low noise amplifier to improve process variability and circuit reliability. In [13], analysis and design of CMOS RF power amplifier using resilient biasing which reduces the impact of variability and reliability when subjected to threshold voltage shift and electron mobility degradation.

In this paper, optimization of the threshold voltage variation for RF CMOS power amplifier with two stages tunable body biasing is proposed. Analytical equations are derived for analysis using three materials with scaling in technology which reduce the threshold voltage shift in preceding stages. GaAs offered prominent threshold voltage variations as compared to Si and GaN. Moreover, this class AB topology achieves power added efficiency of 45 % with output power of 14.96 dBm during simulation. The design also achieves wide bandwidth at resonant frequency of 34 GHz within frequency band of operation. Section 2 describes the analysis of threshold voltage variations. The circuit implementation at design and fabricated level is discussed on Sect. 3. The results and discussion is in Sect. 4 and conclusion is followed in Sect. 5.

2 Analysis of Threshold Voltage Variation

This section describes the analysis of threshold voltage variation using different substrate materials with scale down in CMOS technology which reduces the impact of variability of V_T. The tunable body biasing technique is already studied in [13]. It is observed that the threshold voltage V_T is the major circuit performance parameter for CMOS technology and its variability depends upon the substrate materials as well as technology scaling. The numerical analysis of V_T variation is discussed in next sub-sections *A* and *B* respectively.

2.1 Single Stage Class AB PA with Tunable Body Biasing

Figure 1 shows the conventional design of single stage body biasing class AB PA. In Liu and Yuan [13] have designed a resilient biasing technique for PA using silicon substrate with 65 nm PTM and achieved a more stable design in terms of sensitivity of threshold voltage variation δV_T. During analysis, it is found that the level of reduction in V_T of MOSFET is related to the body effect coefficient γ and MOSFET structure coefficient β.

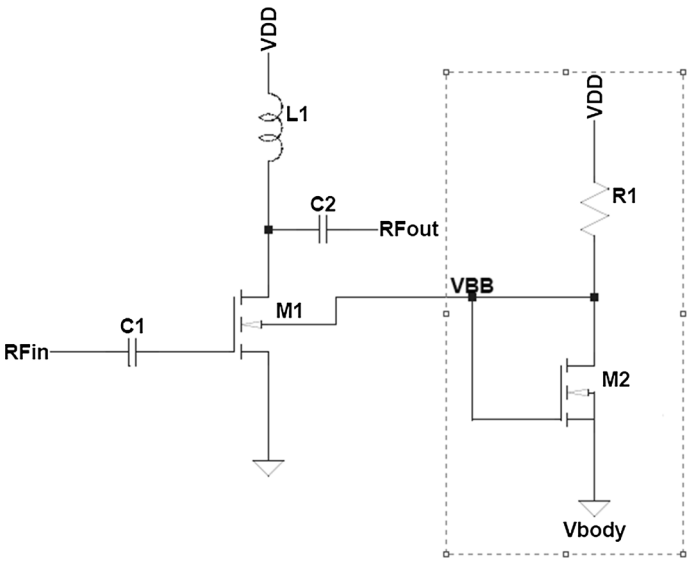

Fig. 1 Conventional design of single stage body biasing class AB PA

The β and γ depends upon the substrate material as well as technology scaling. Using this conception, three different materials Si, GaN and GaAs with two PTM of 65 and 45 nm are employed for the analysis of δV_T. The calculated node voltage V_{BB} is given in Eq. (1) [13].

$$V_{BB} = V_{body} + V_{T2} + \frac{\sqrt{2\beta_2 R_1 (V_{DD} - V_{body} - V_{T2}) + 1} - 1}{\beta_2 R_1} \tag{1}$$

Here, V_{body} is voltage of MOSFET M_2, V_{T2} is threshold voltage of M_2 and β_2 is MOSFET structure coefficient and its expression is $(= \mu_n C_{ox} \frac{W}{L})$. From this relation (1), it is noticed that the potential V_{BB} is a function of body bias V_{body} and threshold voltage V_{T2}. Here, V_{body} is assumed to be constant and is lower than the supply voltage V_{DD}. The parameter V_{T1} of MOSFET M_1 due to body effect is given in Eq. (2).

$$V_{T1} = V_{TO} + \gamma\left(\sqrt{2\emptyset_F - V_{BB}} - \sqrt{2\emptyset_F}\right) \tag{2}$$

Here, V_{TO} is zero bias threshold voltage of M_1, γ is the body coefficient of M_1 whose expression $(\gamma = \frac{\sqrt{2q\in_{substrate} N_{substrate}}}{C_{ox}})$ and $\emptyset_F$ is the Fermi Potential $(= \left(\frac{kT}{q}\right)\ln\left(\frac{N_{substrate}}{n_i}\right))$. Now, parameters of the chosen materials Si, GaN and GaAs are analyzed using γ expression. It is possible to reduce δV_{T1} if designer chooses different substrate materials other than silicon where V_T is a critical parameter to be considered. The overall expression of δV_{T1} for single stage body bias PA is stated as in (3) [13].

$$\delta V_{T1} \approx \frac{\partial V_{T1}}{\partial V_{TO}} \delta V_{TO} + \frac{\partial V_{T1}}{\partial V_{BB}} \delta V_{BB} \tag{3}$$

From (1), (2) and (3), it is concluded that the threshold voltage of M_1 depends on the potential V_{BB} and V_{BB} depends on biasing V_{body}. Therefore, V_{T1} of M_1 can be reduced to a minimum value by choosing γ and varying V_{BB} accordingly. All parameters of γ are constant except for $\in_{substrate}$ and C_{ox}. The V_{BB} potential corresponding to M_1 by tuning body voltages is further divided into V_{BB1} and V_{BB2} and as shown in (4) and (5) respectively.

$$V_{BB1} = V_{body1} + V_{T2} + \frac{\sqrt{2\beta_2 R_1 (V_{DD} - V_{body1} - V_{T2}) + 1} - 1}{\beta_2 R_1} \tag{4}$$

$$V_{BB2} = V_{body2} + V_{T2} + \frac{\sqrt{2\beta_2 R_1 (V_{DD} - V_{body2} - V_{T2}) + 1} - 1}{\beta_2 R_1} \tag{5}$$

where V_{body1} and V_{body2} represent the two different tuning body voltages. According to [13], $\delta V'_{T1}$ corresponding to two different body voltages is given as in (6).

$$V'_{T1} = \gamma\left[\sqrt{2\emptyset_F - V_{BB2}} - \sqrt{2\emptyset_F - V_{BB1}}\right] \tag{6}$$

A comparison of calculated threshold voltages with respect to tune body voltage is as shown in Figs. 2 and 3 respectively. From the graph, it can be seen that V_{T1} of M_1 decreases linearly when V_{body} increases from −0.2 to 0.2 V. The amount of percentage

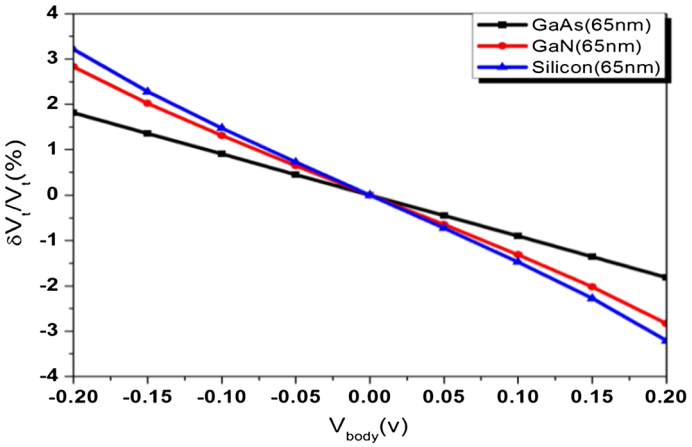

Fig. 2 Sensitivity of threshold voltage versus body voltage

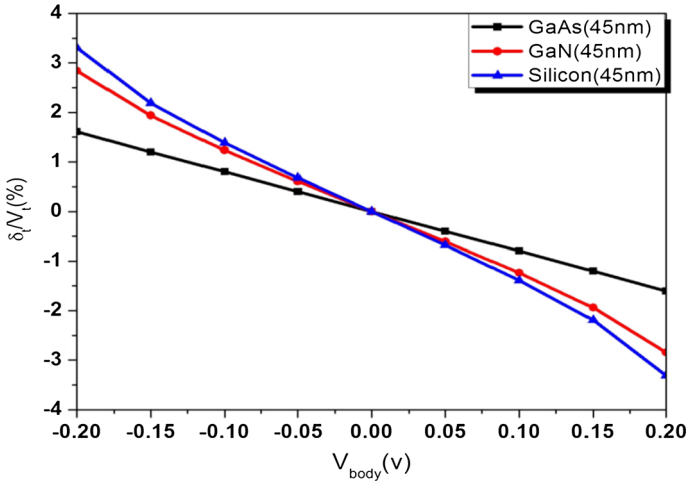

Fig. 3 Sensitivity of threshold voltage versus body voltage

Table 1 Comparison of threshold voltage variation using three materials at 65 and 45 nm

Materials	Silicon (Si) (%)	Gallium nitride (GaN) (%)	Gallium arsenide (GaAS) (%)
$\delta V_t/V_t$ (65 nm)	3.21–3.21	2.75–2.75	1.82–1.82
$\delta V_t/V_t$ (45 nm)	3.29–3.29	2.67–2.67	1.61–1.61

change in $\delta V_T/V_T$ with respect to V_{body} is shown in Table 1. The table highlights the importance of the selection of materials as well as plays vital role by scaling in device length which improves the level of threshold voltage variation reduction. According to graphs, GaAs shows minimum variation of sensitivity in threshold voltage as compared to Silicon and GaN.

2.2 Proposed Two Stage PA with Tunable Biasing

The proposed schematic of two stage body biasing class AB PA is shown in Fig. 4. For optimization of threshold voltage variation, three substrate materials (Si, GaN and GaAs) with scaling in technology are proposed for this analysis. It is found that can be possible to further reduce δV_{T1} of M_1 with the help of one or more stage when incorporated with single body biased PA circuit. The V'_{BB1} and V'_{BB2} potentials are generated by tuning V_{body} and V'_{body} voltages as shown in Eqs. (7) and (8) respectively.

$$V'_{BB1} = V_{body1} + \left[V'_{TO} + \gamma \left(\sqrt{2\emptyset_F - \left(V'_{body1} + V_{T3} + \frac{\sqrt{2\beta_3 R_2 \left(V_{DD} - V'_{body1} - V_{T3} \right) + 1} - 1}{\beta_3 R_2} \right)} - \sqrt{2\emptyset_F} \right) \right] + \frac{\sqrt{2\beta_2 R_1 \left(V_{DD} - V_{body1} - V_{T2} \right) + 1} - 1}{\beta_2 R_1} \tag{7}$$

$$V'_{BB2} = V_{body2} + \left[V'_{TO} + \gamma \left(\sqrt{2\emptyset_F - \left(V'_{body2} + V_{T3} + \frac{\sqrt{2\beta_3 R_2 \left(V_{DD} - V'_{body2} - V_{T3} \right) + 1} - 1}{\beta_3 R_2} \right)} - \sqrt{2\emptyset_F} \right) \right] + \frac{\sqrt{2\beta_2 R_1 \left(V_{DD} - V_{body2} - V_{T2} \right) + 1} - 1}{\beta_2 R_1} \tag{8}$$

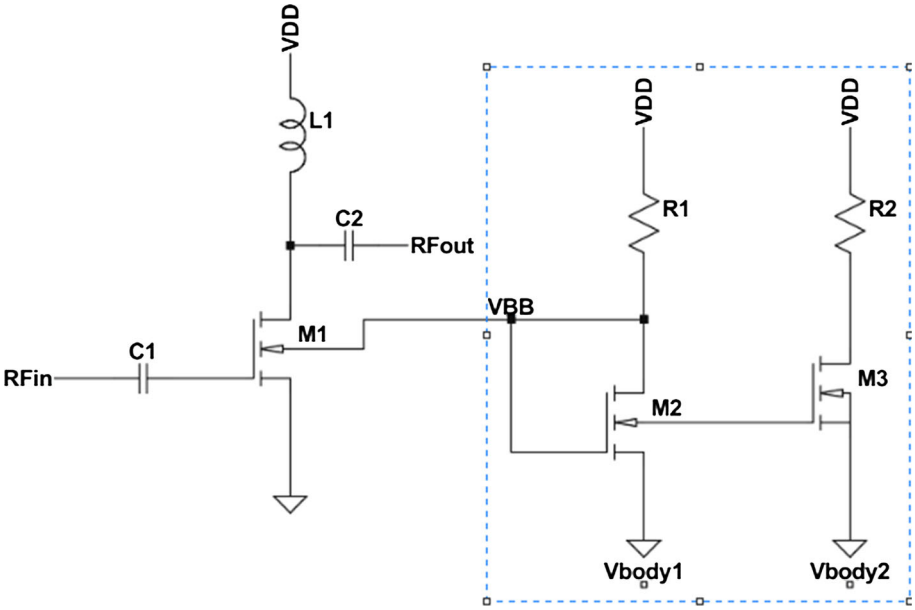

Fig. 4 Proposed schematic of two stages body biasing class AB PA

Here, V'_{body1} and V'_{body2} is obtained by tuning V'_{body} whereas V_{body1} and V_{body2} by tuning V_{body}. V_{T3} is threshold voltage of M_3 which is constant. Now, two values of threshold voltage V_{T2} for M_2 would be generated as V_{T21} and V_{T22} by tuning the body bias of M_3 (V'_{body}) whose expressions are given in (9) and (10).

$$V_{T21} = V_{T2O} + \gamma\left(\sqrt{2\emptyset_F - (V'_{BB1})} - \sqrt{2\emptyset_F}\right) \tag{9}$$

$$V_{T22} = V_{T2O} + \gamma\left(\sqrt{2\emptyset_F - (V'_{BB2})} - \sqrt{2\emptyset_F}\right) \tag{10}$$

Here, V_{T2O} is zero bias threshold voltage of M_2. Now putting the values of V_{T21} and V_{T22} in place of V_{T2} in Eqs. (4) and (5) and evaluate according to Eq. (6), the values for δV_{T1} is obtained. A complete expression is shown below which could be complicated when substituting V'_{BB1} and V'_{BB2} as given in (7) and (8) respectively.

$$\delta V_{T1} = \gamma\left[\sqrt{(2\emptyset_F - V'_{BB2})} - \sqrt{(2\emptyset_F - V'_{BB1})}\right] \tag{11}$$

Plots of the normalized value of V_{T1} with respect to V_{body} are shown in Figs. 5 and 6 respectively. The percentage change in $\delta V_T/V_T$ with respect to V_{body} is shown in Table 2. Here, the tabular data indicates fact that a two stage resilience network provides further reduction in δV_{T1}. Again, GaAs shows calculated variation of δV_{T1} from 1.80 to −1.82 % at 65 nm while 1.59 to −1.61 % at 45 nm. The proposed network can gives better performance of MOSFET because it is well known that threshold voltage is must small as much as possible.

3 Circuit Design

Figure 7 shows a 34 GHz class AB PA topology which includes two stage body biasing circuit, input matching network and output matching network. In class AB PA, matching networks is composed of C_1, C_2, C_3, L_2 and L_3 with bias voltages of V_{GG} and V_{DD}. The

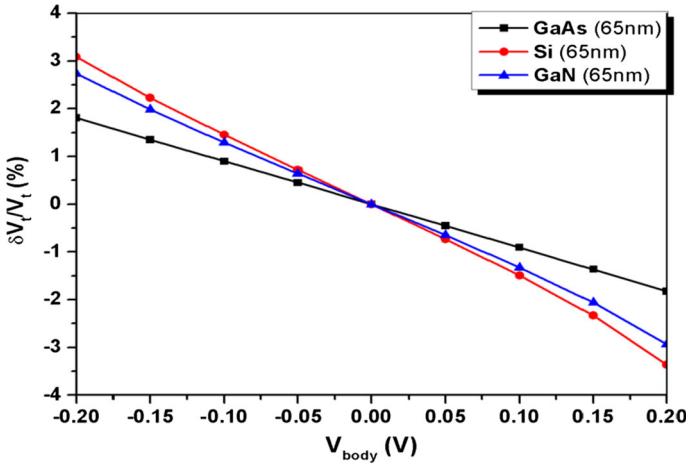

Fig. 5 Variation of threshold voltage versus body biasing

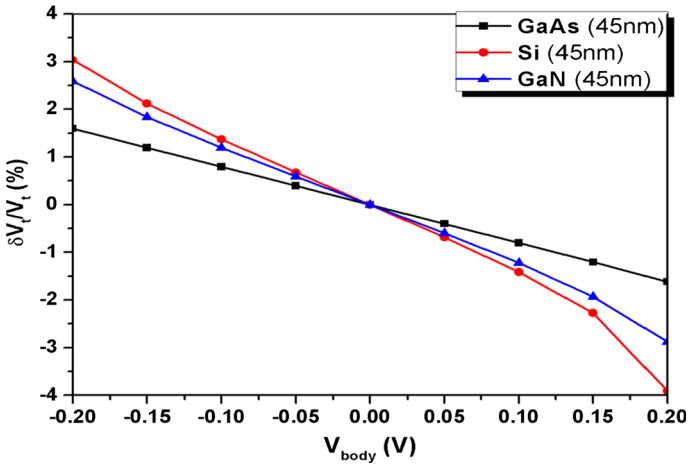

Fig. 6 Variation of threshold voltage versus body biasing

Table 2 Comparison of threshold voltage variation using three materials at 65 and 45 nm

Materials	Silicon (Si) (%)	Gallium nitride (GaN) (%)	Gallium arsenide (GaAS) (%)
$\delta V_t/V_t$ (65 nm)	3.08–3.36	2.73–2.93	1.80–1.82
$\delta V_t/V_t$ (45 nm)	3.03–3.90	2.58–2.87	1.59–1.61

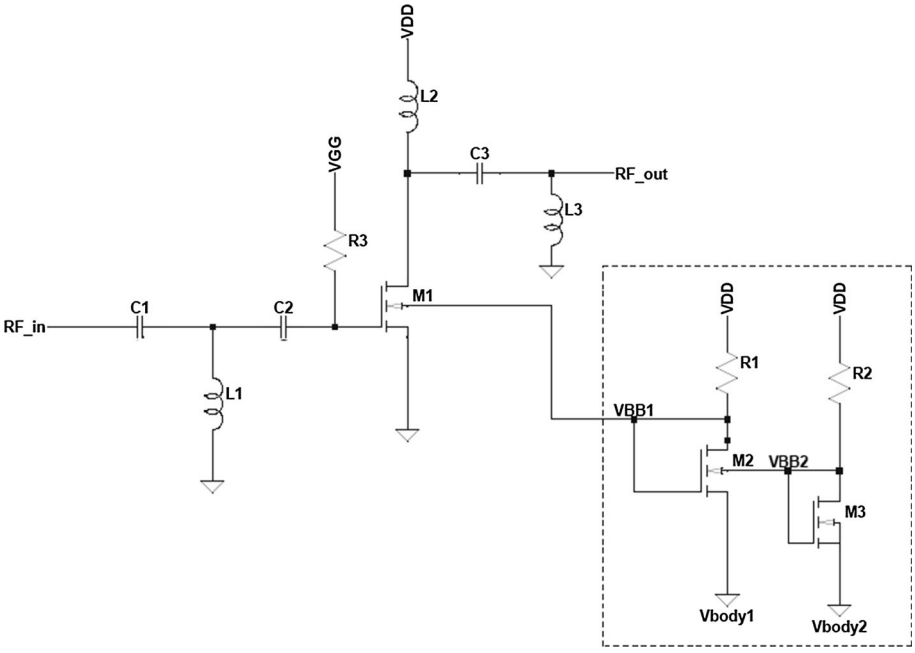

Fig. 7 Proposed architecture of CMOS Class AB PA with matching network

Table 3 Component values with dimensions of proposed power amplifier

C1	C2	C3	L1	L2	L3
64 fF	1.23 pF	1 pF	1 nH	0.5 nH	1.2 nH
R1 (KΩ)	R2 (KΩ)	R3 (KΩ)	M1 (μm)	M2 (μm)	M3 (μm)
1	4	26	80	180	280

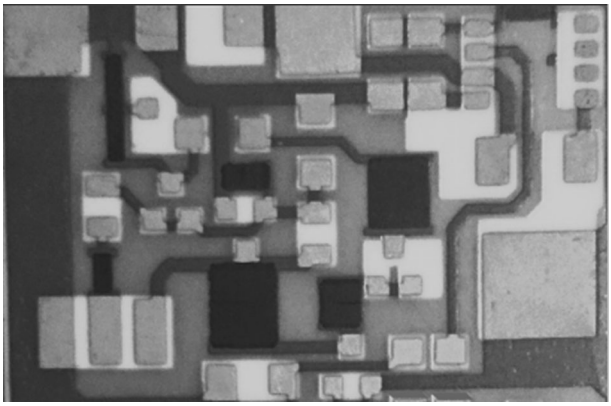

Fig. 8 Chip photograph of 34 GHz Power Amplifier

biasing voltages are chosen according to [13]. The RF source is taken as 50 Ω and gets maximum power transformation when impedance matching network between source and transistor input are employed. It is possible to achieve maximum output power, gain and power added efficiency (PAE) by improving the input matching. The optimal output value is achieved by tuning the output matching network using ADS load pull instrument. The 45-nm NMOS transistors are modeled by the PTM equivalent BSIM4 model card. As discussed in above section, V_T is the most significant parameter and affected by body biasing of the transistors. According to [13], tunable biasing technique controls the body potential of the MOSFET which is to adjust the threshold voltage and to achieve maximum output power and PAE. So, here also two stages of tunable body biasing improve V_T variation of CMOS PA and after simulation achieves more output power, higher gain and best PAE. The proposed schematic design of 34 GHz PA topology is simulated using harmonic balance (HB) simulator in advanced design system (ADS) tool. Table 3. Gives design specifications of proposed power amplifier and its values. Figure 8 presents the chip photograph of the 34 GHz CMOS PA with a chip size of 0.84×0.95 mm^2. For fabrication silicon substrate is utilized. The simulation and measured results of this design are discussed in next section.

4 Results and Discussion

The above discussed 34 GHz class AB PA topology is simulated by ADS using PTM model of 45 nm CMOS process. In the input matching, parallel inductance L_1 is 1 nH and series capacitances C_1 and C_2 are 64 fF and 1.23 pF respectively. At the output,

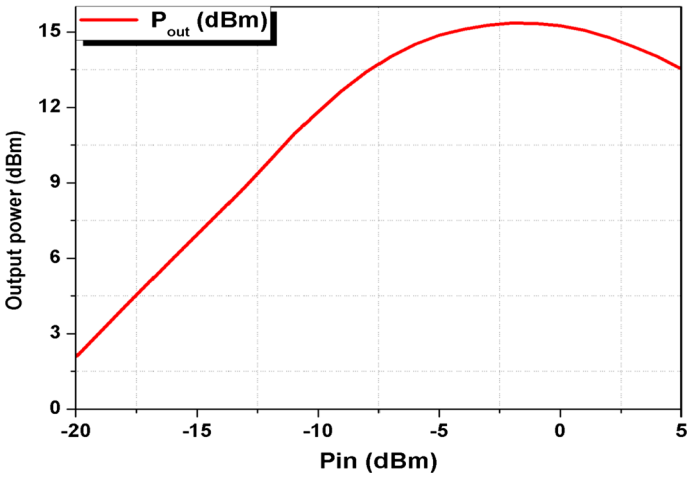

Fig. 9 Output power versus input power

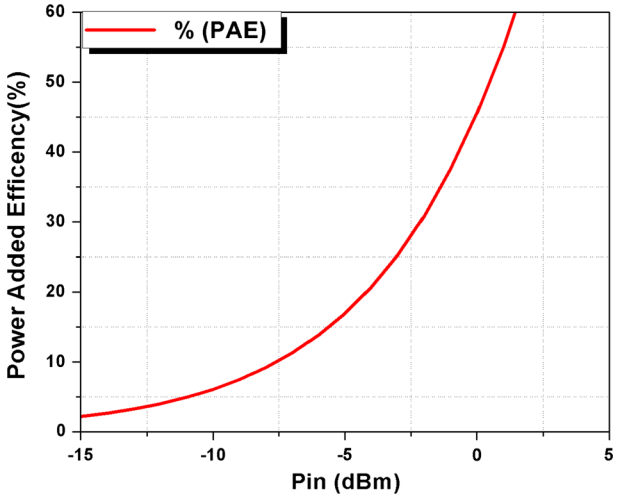

Fig. 10 PAE versus input power

capacitance C_3 is 1 pF where inductance value L_3 is 1.2 nH. As shown in Fig. 9, at 34 GHz, output power is 14.96 dBm while input power signal is 0 dBm. It is observed that if input power is <0 dBm and with the increase of input power, output power increases but output powers stop up to a saturation point, once the input power exceeds the 0 dBm. It is seen that in Fig. 10, the maximum power added efficiency (PAE) of this circuit achieves up to 44.8 %. The PA is measured via On-wafer probing with test capability of 35 nm plate. The measurement of fabricated chip could be possible for s-parameters only. As per the simulation and measurement results, return loss is obtained at the operating frequency of 34 GHz within frequency range of 33–35 GHz which is shown in Fig. 11. It is small

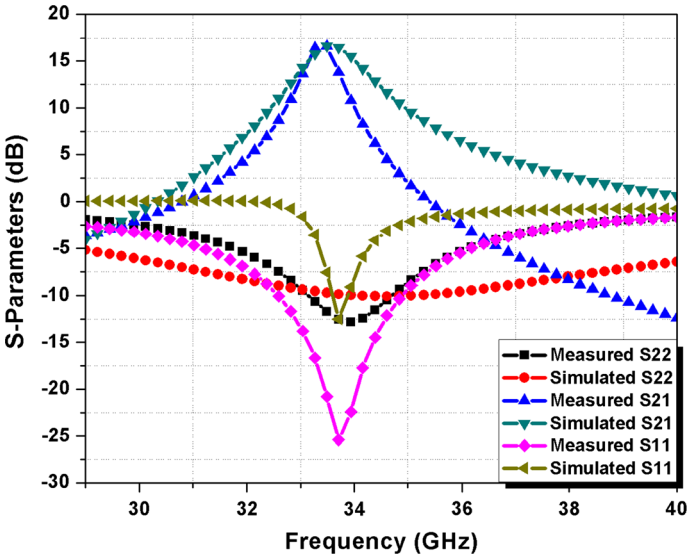

Fig. 11 Variation of return loss and forward gain versus frequency

Table 4 Comparison of circuit design with previous reported paper

Parameters	[13]	Current work
Technology (μm)	0.065	0.045
Freq (GHz)	24	34
Supply voltage (V)	1	1
S_{11} (dB)	NA	−23
S_{21} (dB)	NA	16.9
Pout (dBm)	10.96	14.96
PAE (%)	34.25	44.80

enough to indicate the satisfactory input matching. The best gain of 16.9 dB is achieved with the help of two stages tunable biasing body design can see in Fig. 11. A dc power dissipation of approximately 11.3 mW under 1 V power supply is utilized for this design. Table 4. Show comparison in parameters of circuit design with previous reported paper.

5 Conclusion

In this paper, two stage tunable body biasing class AB PA using three substrate materials with scaling in technology optimizes the threshold voltage variation. A single stage adaptive body biasing class AB PA is compared with two stages and it is analytically proven that the threshold voltage variation in preceding stages can be diminished if body biasing design is tunabled. A two stage tunable body biasing class AB Power amplifier with matching networks is simulated in ADS and shows that at operating frequency of 34 GHz, output power is 14.96 dBm and PAE of 44.8 %. Performance standards are met for the PA circuit. Moreover, state of the art of this work achieves S_{11} of −23 dB with

forward gain of 16.9 dB which relaxed 50 Ω matching constraints throughout in PA circuit.

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