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A Novel CMOS CCCII Based on Cross-Coupled Differential Transistor Pair and Its Application

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Abstract In this paper, a novel CMOS circuit of second-generation current controlled conveyor (CCCII) is proposed, which offers wide input voltage range and large 3 dB bandwidth of voltage–current transfer gain with high linearity under low supply voltage. The core of this CCCII adopts cross-coupled differential transistor pair as input stage instead of conventionally source-coupled and the principle of the circuit is analyzed theoretically in detail. This CCCII is implemented by PSPICE program in TSMC 0.18 μm RF CMOS technology and verified by simulation results. A current-mode universal filter which consists of two proposed CMOS CCCIIs is also simulated to validate the feasibility of the new circuit topology.

Keywords Cross-coupled · Differential pair · Transfer gain · CMOS CCCII · Universal filter

1 Introduction

The current-mode (CM) circuits have received significant attentions in recent years as they have advantages of high slew-rate, wide bandwidth, small nonlinear distortion, large dynamic-range and so on. The Second-Generation Current Conveyor (CCII) is introduced in 1970 [1], and it is a versatile and flexible building block in current-mode analog circuit design [2–8]. However, CCII has two main drawbacks: (1) large voltage tracking error from terminal Y to terminal X because of the parasitic resistor of terminal X, which leads to transfer function error; (2) lack of electronically tunable feature, which means the parameters can not be adjusted by additional bias current.

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In 1996, A. Fabre proposed a CCCII [9]. It possesses electronically tunable function by utilizing the parasitic floating intrinsic transimpedance at port X (R_X), which can be tuned electronically by adjusting the bias current.

In the past, the core of CCCII is simply constructed by the mixed translinear-loop, which is originally realized in BJT [10, 11] and later in MOSFET [12–15]. BJT has advantages of low noise and high operating frequency, but it is not compatible with CMOS VLSI technology, so it is inconvenient for VLSI integration. Minaei proposed a CMOS CCCII circuit based on MOS translinear loop in 2002 and Al-Shahrani proposed a CMOS CCCII based on source-coupled differential pair input stage in 2003 [16]. However, the CCCII based on MOS translinear-loop has unsymmetrical dynamic-range and strict restrictive condition in fabrication technology. Meanwhile, CMOS CCCII based on source-coupled differential pair has poor input voltage range and low linearity. Hence, the objective of this paper is to present a new CMOS CCCII with high linearity to overcome the problems mentioned above, then it can be better applied in more application fields [17–25], such as chaotic system, oscillators, current mode filters, radio frequency oscillators, low noise amplifiers, ASK/FSK modulators and so on [26–28].

This paper is organized as follows: the cross-coupled differential pair input stage and the proposed novel CMOS CCCII are described in Sects. 2 and 3, respectively. The PSPICE simulation results of this proposed CCCII circuit in TSMC 0.18 μm CMOS RF technology and performance comparison with other reported circuits are included in Sect. 4. To further illustrate merits of this proposed CMOS CCCII, A current-mode universal filter is simulated in Sects. 5 and 6.

2 The Cross-Coupled Differential Pair Input Stage

Assuming that all MOSFET are enhancement-mode types and biased in saturation region with substrates connected to their respective sources. Then the body effect is ignored and the transistor drain current can be approximated by the relation [29]:

$$I_D = k(V_{GS} - V_{TH})^2 \tag{1}$$

where V_{GS} is gate-source voltage, V_{TH} is the threshold voltage, $k = (W/L)\mu C_{ox}/2$ is the trans- conductance parameter, W and L are width and length of the transistor channel, μ is the effective surface carrier mobility and C_{ox} is the gate oxide capacitance per unit area. The channel length modulation effect is not included in (1).

The CCCII circuit symbol is illustrated in Fig. 1 and its ideal defining equation can be given as [12]:

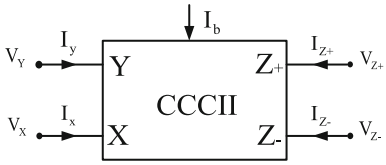

Fig. 1 Circuit symbol of CCCII

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{2}$$

In Fig. 1, terminal X is a current input which possesses low input impedance; terminal Y is a voltage input which possesses high input impedance; Z+ is the non-inverting current output port, and Z− is the inverting current output port. I_b is the biasing current, by which the voltage relation between terminal X and terminal Y is adjustable.

The current output at port $Z(i_z)$, which is conveyed from the input current at port $X(i_x)$, can be expressed as [14]:

$$i_x = \pm i_z = \pm \frac{v_x - v_y}{R_x} \tag{3}$$

As R_x is the parasitic resistance, the CCCII-based application can be realized in resistor-free and tunable architectures by utilizing R_x as the adjustable circuit parameter. To better understand the function of CCCII, the equivalent circuit of it is displayed in Fig. 2.

Considering a matched transistor pair (M_{n1}, M_{n2}) coupled by two voltage sources with equal value of $(V_{TH} + V_x)$, which is shown in Fig. 3. Representing $(V_2 - V_1)$ by v, using (1) gives:

$$I_1 = k(V_x - v)^2 \tag{4a}$$

$$I_2 = k(V_x + v)^2 \tag{4b}$$

The output current $i_x = I_1 - I_2$, obtained by a simple p-channel current mirror, will be

$$i_x = I_1 - I_2 = 4kV_x v \tag{5}$$

Thus this configuration exhibits a perfectly linear transconductance of value $G_m = 4kV_x$.

3 The Proposed CMOS CCCII

Considering a actual implementation of the circuit described in Fig. 3, the sources $(V_{TH} + V_x)$ are substituted by two additional n-channel transistors (M_{n3} and M_{n4}) biased by constant currents. The practical circuit configuration is displayed in Fig. 4. M_{n1} and M_{n4} share a same p-well connected to their common source node, whereas M_{n2} and M_{n3} are in a separate well to avoid back-gate bias effects. For obtaining reasonable voltage sources with low source impedance, these devices must be biased with currents which are larger than the signal currents through them.

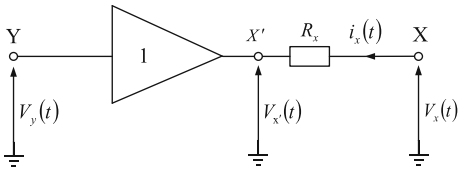

Fig. 2 Equivalent circuit of a CCCII

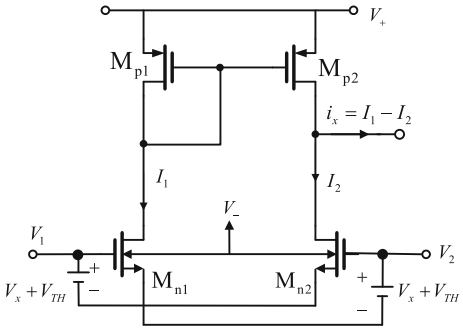

Fig. 3 Schematic diagram of cross-coupled input stage

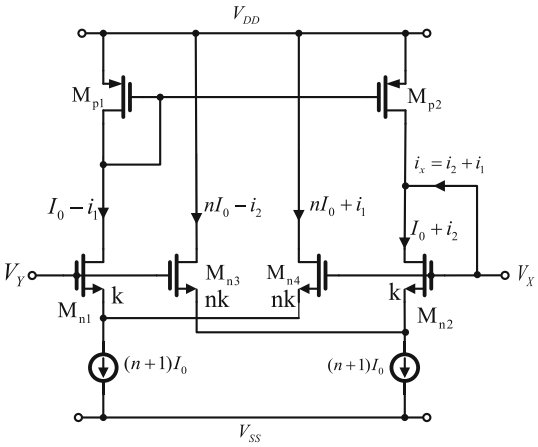

Fig. 4 Practical circuit configuration of cross-coupled input stage

M_{n1}, M_{n2}, M_{n3} and M_{n4} have the same channel length, but the channel widths of M_{n3} and M_{n4} are made n times wider than M_{n1} and M_{n2}. For maintaining the value of $V_b = \sqrt{I_0/k}$, M_{n3} and M_{n4} are biased with nI_0. Defining normalized variables $X = V_{XY}/V_b$ and $Y = i_x/I_0$ with reference to Fig. 4, we write:

$$Y_1 = i_1/I_0 = -\gamma X^2 + \frac{\alpha}{2} X\sqrt{1-\beta X^2} \tag{6a}$$

$$Y_2 = i_2/I_0 = \gamma X^2 + \frac{\alpha}{2} X\sqrt{1-\beta X^2} \tag{6b}$$

where

$$V_{XY} = V_X - V_Y$$

and

$$\alpha = 4n/(n+1), \quad \beta = n/(n+1)^2, \quad \gamma = n(n-1)\Big/(n+1)^2 \tag{6c}$$

The output $Y = i_x/I_0 = (i_1 + i_2)/I_0$ is obtained as

$$Y = \alpha X\sqrt{1-\beta X^2} \quad \left(|X| \le \sqrt{(n+1)/n}\right) \tag{7}$$

We can change the formula by following equation

$$i_x = \alpha\sqrt{kI_0}V_{XY}\sqrt{1-\beta k V_{XY}^2/I_0} \tag{8}$$

From (6c) and (7), the estimation of symmetrical dynamic-range of the cross-coupled input stage is

$$|V_{XY}| \le \sqrt{(n+1)/n}\cdot\sqrt{I_0/k} \tag{9}$$

and the roughly linear input range is

$$|V_{XY}| << \left((n+1)/\sqrt{n}\right)\cdot\sqrt{I_0/k} \tag{10}$$

For n = 10, in order to obtain better than 1 percent linearity, the actual linear input range is

$$|V_{XY}| \le \sqrt{I_0/k} \tag{11}$$

During the linear input range, we know the parasitic resistor is

$$R_x = \left(\frac{40}{11}\cdot\sqrt{kI_0}\right)^{-1} \tag{12}$$

For large n, we can obtain wider linear input range. For $n = 1$, we obtain $\alpha = 2$, $\beta = 0.25$, $\gamma = 0$, and the two equations become identical. With the value of n is increased, β becomes smaller, resulting in improved linearity in the transfer characteristics. For $n >> 1$, from (6c) we get $\alpha \cong 4$, $\gamma \cong 1$, and $\beta \cong 1/n$. In the limit as $n \to \infty$, $\beta \to 0$ and a linear parasitic resistance $R_x = 1/4\sqrt{kI_0}$ is obtained over the entire range $|X| \le 1$ (i.e.$|V_{XY}| \le \sqrt{I_0/k}$). Furthermore, the circuit is also operated for input voltages well

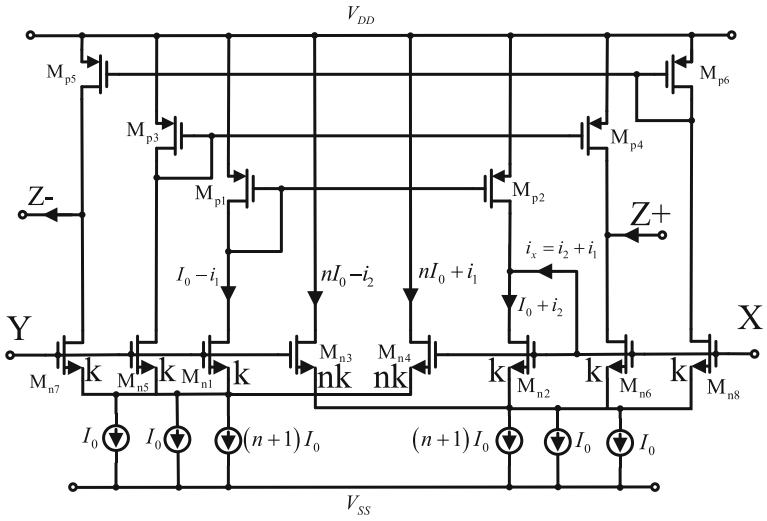

Fig. 5 The proposed CCCII ± circuit

outside this range, though in a nonlinear fashion. The maximum available input current is $(n+1)I_0$.

Figure 5 shows the proposed CCCII ± circuit, of which the Z ± differential pair is identical to the active loaded NMOS differential pair of the input stage. For maintaining the same value of drain current, M_{n5} and M_{n6}, M_{n7} and M_{n8} have the same size of M_{n1} and M_{n2}, while biased with I_0.

For the Z+ differential pair of Fig. 5, we can get:

$$i_{n6} = i_{n2} \tag{13}$$

$$i_{p4} = i_{p3} = i_{n5} = i_{n1} = i_{p1} = i_{p2} \tag{14}$$

Therefore, the i_x and i_z are approximated equal through the condition shown in (15):

$$i_z = i_{n6} - i_{p4} = i_{n2} - i_{p2} = i_x \tag{15}$$

The Z− differential pair which horizontally flipped from the Z+ differential pair yields:

$$i_{n5} = i_{n1} = i_{p1} = i_{p2} \tag{16}$$

$$i_{p3} = i_{p4} = i_{n6} = i_{n2} \tag{17}$$

From (16) and (17), we can get:

$$i_z = i_{n5} - i_{p3} = i_{p2} - i_{n2} = -i_x \tag{18}$$

In summary, any required output properties of the CCCII can be generated by putting the appropriate Z+ or Z− pairs in concurrent with the NMOS differential pair of the input stage. Three types of differential pairs illustrated in Fig. 6 are fundamental blocks for synthesizing a CCCII. As the input stage differential pairs must be existed, the number and type of output pairs can be selected to fulfill the requirement.

4 Performance Simulations

The proposed CMOS CCCII in Fig. 5 is simulated by PSPICE program. In the simulation process, the W/L ratios of each MOS transistor are shown in Table 1 and TSMC 0.18 μm CMOS RF technology parameters are used.

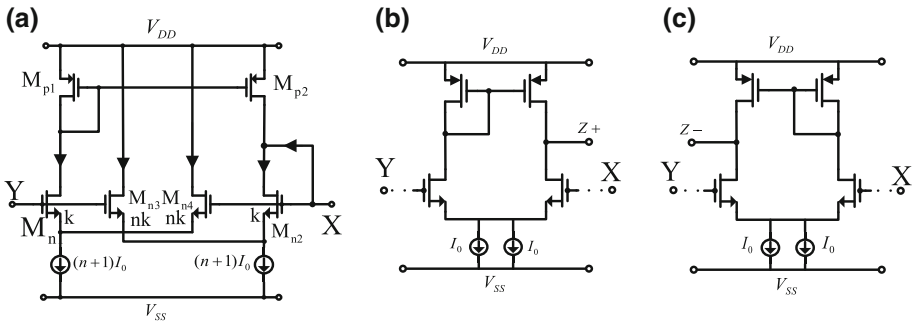

Fig. 6 Proposed structure **a** input stage, **b** Z^+ pair, **c** Z^- pair

Table 1 W/L ratios of MOSFETS in Fig. 6

MOS transistors	W/L ratio (μm)
M_{n1}–M_{n2}, M_{n5}–M_{n8}	0.18/0.18
M_{n3}–M_{n4}	1.8/0.18
M_{p1}–M_{p2}	0.9/0.18
M_{p3}–M_{p6}	3.6/0.18

The circuit uses 14 transistors with a ±1.5 V voltage supply and the DC biased current is 50 μA. From Table 1, we can get that M_{n3} and M_{n4} are made ten times wider than M_{n1} and M_{n2} with the same channel length of 0.18 μm.

In order to validate the correctness of (2), the static characteristic is firstly analyzed. By conducting DC scan for Y port, the voltage relationship between X and Y port is obtained and charted in Fig. 7. From the curve we can find that voltages of X and Y port meet the voltage relationship of (2) with very low offset-voltage. It exhibits a linear one-to-one voltage following characteristic over large voltage range as well as DC current transfer characteristics displayed in Fig. 8, but has little poor follower characteristic at port Z+.

In Fig. 9, the small signal current gain characteristics between terminals Z+ and X with grounded node Y is displayed. It is clearly that the 3 dB bandwidth of current gain approximates about 7.78 GHz. Fig 10 shows the small signal voltage gain between terminals X and Y when node Z is grounded. The 3 dB bandwidth of voltage gain is 11.61 GHz.

Table 2 compares the main performances of the proposed new CCCII described in Fig. 5 with those recently published relevant works. All these simulation results are obtained under a bias current of $I_0 = 50$ μA. The symbols α_0 and β_0 represent current transfer (between X and Z) and voltage transfer (between Y and X), respectively. As exhibited in Table 2, the CCCII of Fig. 5 provides higher input impedance in Y port, wide input voltage range and higher 3 dB bandwidth for current and voltage gain.

Figure 11 shows the characteristics of R_x at terminal X, and it is denoted that the simulation result of R_x is nearly equal to 2.25 kΩ in the frequency range from 1 to 630 MHz at bias current $I_0 = 100$ μA. Different R_x values are also obtained at various bias

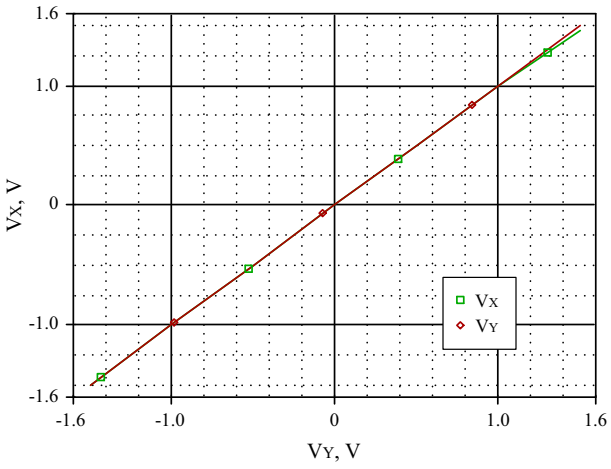

Fig. 7 DC transfer characteristic of Y and X port voltage

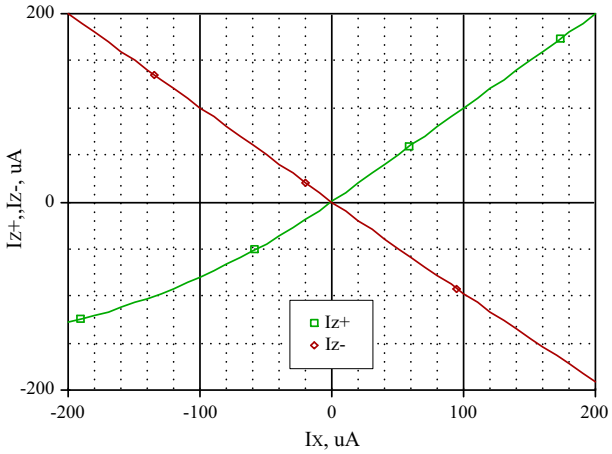

Fig. 8 DC current transfer characteristics of CCCII±

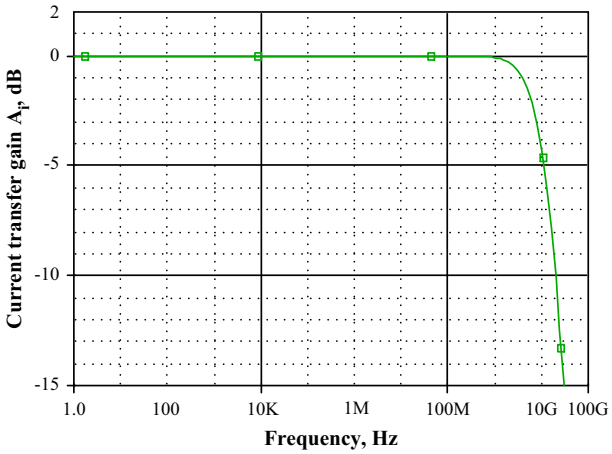

Fig. 9 Current transfer gain

current in the figure, which indicates that the transresistance of the new CCCII is electronically tunable in large bias current range.

5 Application of the CCCII to Current-Mode Filter

The CCCII can be made electronically adjustable in different applications. In this section, a novel universal filter with single-input, triple-output employing only four elements (include two proposed CCCIIs) is presented in Fig. 12.

This filter contains only two capacitors without requirement of any additional passive resistance and its structure can be characterized by the following expressions [26]:

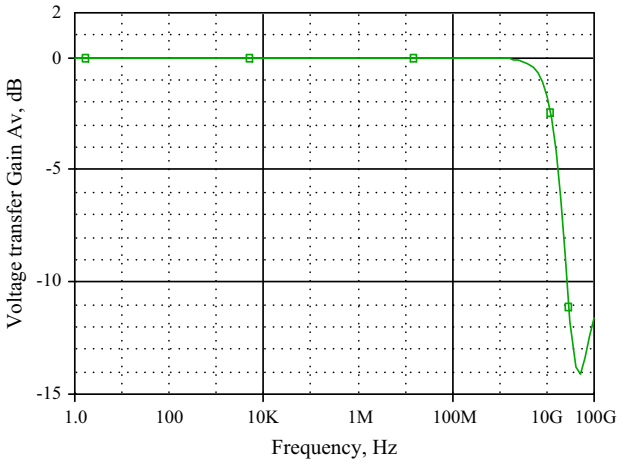

Fig. 10 Voltage transfer gain

Table 2 Simulation performances comparison of reported works and this paper

Performance parameters	CCCII in [13]		CCCII in [29]	This work
Technology	3 μm TUBITAK CMOS process model parameters		AMS's 0.35 μm CMOS model	0.18 μm TSMC CMOS RF model
Bias current	50 μA		50 μA	50 μA
	1st	2nd	N/A	N/A
α_0	1	1	0.991	0.9997
3-dB Bandwidth of α_0	151 MHz	1.44 MHz	487 MHz	7.78 GHz
β_0	0.98	0.99	0.9915	1
3-dB Bandwidth of β_0	Unmeasurable	Unmeasurable	527 MHz	11.61 GHz
Rx (Ω)	2.15 K	1.87 K	2.75 K	2.896 K
R_Y (Ω)	$\approx\infty(R_Y > 1\times10^{13})$	41.8×10^6	216 M	$\approx\infty(R_Y = 1\times10^{20})$
Rz (Ω)	33.8×10^6	2×10^9	305.1 K	512.5 K
Linear input range of VY	N/A	N/A	±165 mV	−1.5 to 1.22 V
Linear input range of VX	N/A	N/A	±50 μA	−0.06 to 0.21 mA
Output offset current at Z	N/A	N/A	1.06 μA	−1.02 μA
Supply voltage	±5 V	±5 V	±1.5 V	±1.5 V
Total dissipation	N/A	N/A	0.45 mW	3.9 mW

$$\frac{I_{in} - I_{o1} - I_{o2}}{SC_1} - I_{o1}R_{x1} = 0 \tag{19}$$

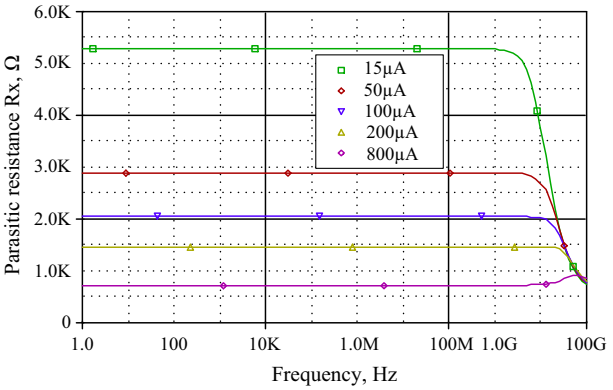

Fig. 11 Parasitic resistance R_x when n = 10

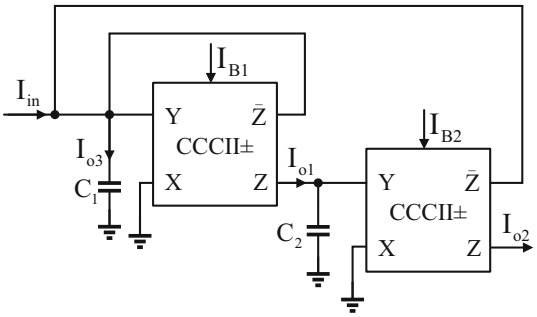

Fig. 12 Current-mode universal filter uses the proposed CCCII

$$\frac{I_{o1}}{SC_2} - I_{o2}R_{x2} = 0 \tag{20}$$

Then the transfer function of this circuit is given as follows:

$$\frac{I_{o1}}{I_{in}} = \frac{SR_{x2}C_2}{S^2R_{x1}C_1R_{x2}C_2 + SR_{x2}C_2 + 1} \tag{21}$$

$$\frac{I_{o2}}{I_{in}} = \frac{1}{S^2R_{x1}C_1R_{x2}C_2 + SR_{x2}C_2 + 1} \tag{22}$$

$$\frac{I_{o3}}{I_{in}} = \frac{S^2R_{x1}C_1R_{x2}C_2}{S^2R_{x1}C_1R_{x2}C_2 + SR_{x2}C_2 + 1} \tag{23}$$

$$\frac{I_{o3} + I_{o2}}{I_{in}} = \frac{S^2R_{x1}C_1R_{x2}C_2 + 1}{S^2R_{x1}C_1R_{x2}C_2 + SR_{x2}C_2 + 1} \tag{24}$$

$$\frac{I_{o3} - I_{o1} + I_{o2}}{I_{in}} = \frac{S^2R_{x1}C_1R_{x2}C_2 - SR_{x2}C_2 + 1}{S^2R_{x1}C_1R_{x2}C_2 + SR_{x2}C_2 + 1} \tag{25}$$

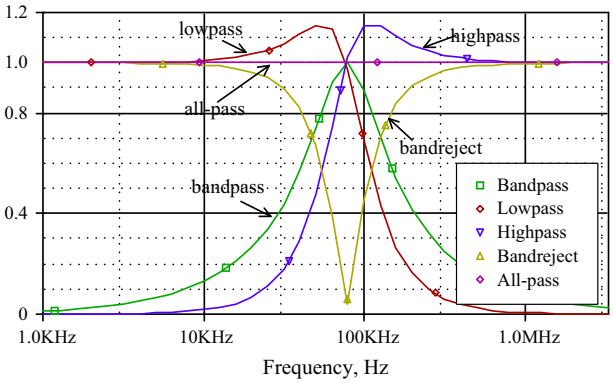

Fig. 13 Simulation result of the universal filter

Equations (21)–(25) show that the proposed filter produces bandpass, lowpass, high-pass, bandreject and all-pass responses simultaneously at its outputs. The natural frequency and the quality factor of the proposed circuit can be obtained as [26]:

$$\omega_0 = \frac{1}{\sqrt{R_{x1}C_1R_{x2}C_2}} \tag{26}$$

$$Q = \sqrt{R_{x1}C_1/R_{x2}C_2} \tag{27}$$

The validity of the proposed filter is verified using PSPICE. For these simulations, the passive components are configured as $C_1 = C_2 = 1$nF and CCCIIs are implemented using the model in Fig. 5. The voltage supplies are taken as ± 1.5 V and the bias current $I_{B1} = I_{B2} = 100$ μA. The results shown in Fig. 13 validate the feasibility of the proposed filter topology. By changing the bias current value of the two CCCIIs, the function of this filter can be adjusted.

6 Conclusion

This paper proposes a new CMOS CCCII based on cross-coupled differential transistor pair instead of source-coupled as input stage. By using cross-coupled differential transistor pair and other improvements in circuit design, the presented topology has merits of wide input voltage range and improved maximum operational frequency with competitive linear performance under lower supply voltage. Simulation results obtained from PSPICE shows that the proposed circuit not only meets the port characteristics of standard CMOS CCCII but also conforms theoretical behavior prediction. As compared with previously reported works and analyzed a universal filter based on it, the proposed CCCII can be potentially applied in many fields for accomplishing high performance circuit systems.

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