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Leakage Current Reduction Techniques for 7T SRAM Cell in 45 nm Technology

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Abstract In this paper the impact of gate leakage on 7T static random access memory (SRAM) is described and three techniques for reducing gate leakage currents and sub threshold leakage currents are examined. In first technique, the supply voltage is decreased. In the second techniques the voltage of the ground node is increased. While in third technique the effective voltage across SRAM cell Vd = 0.348V and Vs = 0.234V are observed. In all the techniques the effective voltage across SRAM cell is decreased in stand-by mode using a dynamic self controllable voltage level (SVL) switch. Simulation results based on cadence tool for 45 nm technology show that the techniques in which supply voltage level is reduced is more efficient in reducing gate leakage than the one in which ground node voltage is increased. Result obtained show that 437 FA reductions in the leakage currents of 7T SRAM can be achieved.

Keywords CMOS · Gate leakage current · Sub threshold current · Voltage level switch · SRAM · Stand-by power

1 Introduction

Design techniques for low-power circuits, for example, for use in battery-driven mobile phones, are not only needed for logic circuits (such as extremely fast adders and multipliers) but also for storage circuits (such as flip-flops, register files, and memories). An integrated static random access memory (SRAM) compiler is proposed to reduce both leakage and dynamic power at circuit and architectural level [1]. There are several techniques for

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reducing standby power Pst [2–4]. One is to use a multithreshold-voltage CMOS (MTCMOS). This technique reduces Pst by disconnecting the power supply through the use of pMOSFET switches with higher threshold voltage Vthp and nMOSFET switches with higher threshold Vthn voltage. However, it has serious drawbacks such as the need for additional fabrication processes for higher Vthp and higher Vthn and the fact that storage circuits based on this technique cannot retain data. To solve this drawback, a self controllable voltage level switch, which can significantly decrease stand-by power, while maintain the high speed performance [5]. There is a significant increase in the sub-threshold leakage due to its exponential relation to the threshold voltage, and gate leakage due to the reducing gate-oxide thickness [6]. The subthreshold leakage current is exponentially dependent on the gate-to-source voltage of a MOSFET [7]. When the SRAM circuit are in active mode, the SVL switch generated maximum supply voltage (e.g. Vd = 0.7V) and the minimum ground level voltage (Vs = 0V) to them through switches that are turned on. So the SRAM circuit can operate quickly. On the other hand when the SRAM circuit are in stand-by mode, it generates slightly lower supply voltage and relatively higher ground level voltage. The present work describes such an analysis and shows that use of SVL switch for reducing supply voltage yields the maximum reduction in leakage currents especially when the pre-charge transistors are put in cut-off state during the stand-by mode. An SVL switch can be used either to reduce the supply voltage to the SRAM cell or increase the potential of ground level and the two approaches can be combined as well. Although a technique similar to use of SVL for raising the ground potential has already been reported to yield significant reduction in gate leakage currents [8], a detailed comparison of these alternative approaches has not yet been undertaken. An analysis of leakage currents in 7T SRAM cell has been carried out and techniques for suppressing it are compared. It reduces the subthreshold leakage current by increasing the ground level during the idle (inactive) mode [9]. Of the several techniques which have been proposed to reduce sub threshold leakage in SRAM cells [10–12], use of a self-controllable switch (SVL) [13] which allows full supply voltage to be applied in active mode and reduced supply voltage in stand-by mode appears to be particularly promising for reducing gate leakage currents as well. A number of techniques have been proposed in literature for reducing the impact of leakage power dissipation such as gated-Vdd scheme [11], Dual-Vt SRAM [12] etc. As a result, even though supply voltage has also been reduced with new generations of technology, the magnitude of gate leakage current has increased steadily and is likely to become comparable or even larger than Sub-threshold leakage for future CMOS devices [14]. The SRAM instability and leakage dissipation in scaled-down technologies by presenting a novel design flow for simultaneous power minimization, performance maximization and process variation tolerance optimization of nano-CMOS circuits [15]. The 7T SRAM cell consumes higher hold power due to its extra cell area required for its functionality constraint [16].

In this paper we propose a 7T SRAM cell in 45 nm technology, its channel length is 45 nm and width is 120 nm. The 7T SRAM cell consists of seven transistors, in which two inverters (M1, M3 and M2 and M4) are connected in cross coupled manner, transistors M5 and M6 are write access transistor and transistor M7 is the read access transistor. It is designed in 45 nm technology because it occupies less chip area density as compares to other nanometre technologies.

The organization of the paper is as follows: Sect. 2 describes the read and write operation of the proposed circuit. Section 3 describes the leakage current that flows in 7T structure. Section 4 explains the various leakage current control strategies. Section 5 describes the advantages of the SVL techniques and Sect. 6 discusses the simulation results. Section 7 concludes the paper.

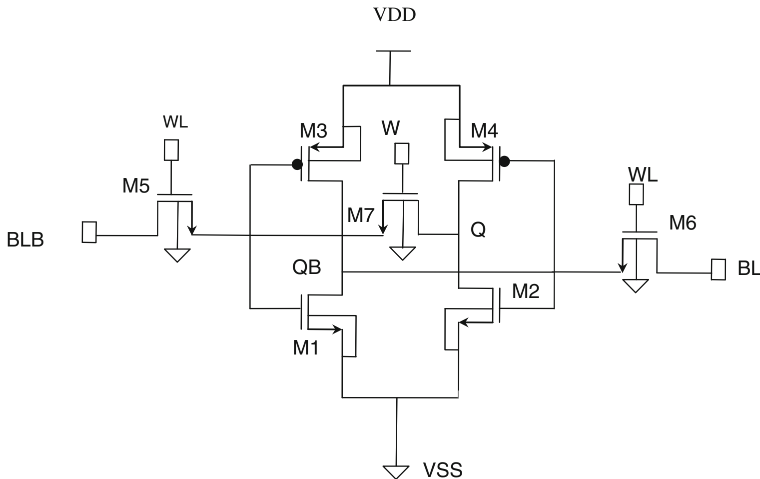

Fig. 1 Schematic of conventional 7T SRAM cell

2 Read and Write Operation of Circuit

The proposed write concept depends on cutting off the feedback connection between the two inverters, inv1 and inv2, before the write operation. The feedback connection and disconnection are performed through an extra NMOS transistor M7, as shown in Fig. 1, and the cell only depends on BLB (Bit line bar) to perform a write operation. The write operation starts by turning M7 off to cut off the feedback connection. BLB carries complement of the input data, M5 is turned on, and M6 is kept off. The SRAM cell looks like two cascaded inverters, inv2 followed by inv1. BLB transfers the complement of input data to input of another inverter which drives inv2, M2 and M4, to develop output, cell data, which drives inv1 and develops QB. The proposed cell can be applicable to the more advanced CMOS technology provided each process and device parameter is scaled to the same degree [17]. The increased device variations, lower supply voltages have enforced the usage of write-assist circuits in SRAMs in the nano-complementary metal oxide semiconductor (CMOS) regime [18]. Figure 1 is the schematic of 7T SRAM cell in this four transistors (M1, M2, M3 and M4) make two inverters which are connected in cross coupled manner. Transistors M5 and M6 are write access transistors, transistor M7 is read access transistor. The layout of conventional seven transistor SRAM using cadence tool is shown in Fig. 2. This is designed in virtuoso layout editor tool.

The output waveform of write and read operation are shown in Fig. 3.

3 Leakage Current in 7T SRAM Bit Cell

In 45 nm technology, the physical oxide thickness is 0.7 nm and channel length is 45 nm. Gate leakage and sub threshold leakage both are important in 7T SRAM bit cell. In the stand-by mode, the bit lines are charged to ‘Vdd’ and the word line is held at ‘low’ voltage. The leakage currents flowing through the transistors depend on the value stored in the cell. When ‘0’ is stored, there is significant gate leakage current through N-type transistors M1,

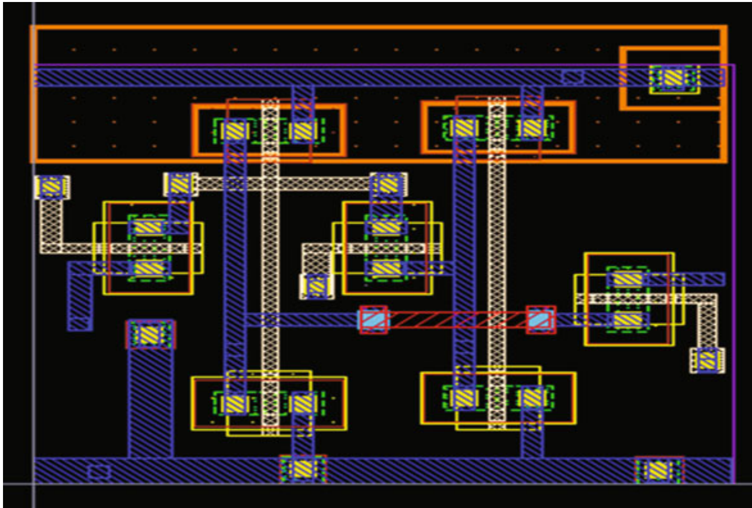

Fig. 2 Layout of conventional 7T SRAM cell

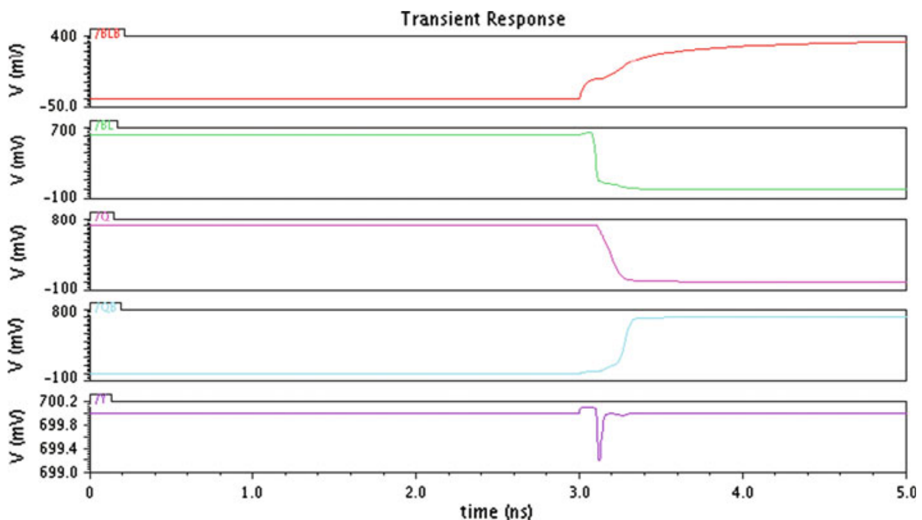

Fig. 3 Read and write waveform of conventional 7T SRAM cell

M5 and M6. Although a similar mechanism operates in transistors M3 as well, the gate leakage here is negligible because of its P-type nature. Gate leakage is maximum in transistors M2 and M7. Sub threshold currents originate in transistors that are in OFF state and that include transistors M1 and M4 in the cross coupled inverter pair and access transistors M5, M6 and M7. Except for transistors M6 and M7 whose drain-source voltage is zero. All three other transistors have significant sub threshold leakage currents. To summarize, there are five dominant components of gate leakage current through transistors M1, M2, M5, M6 and M7 three sub threshold leakage current components through transistors M1, M4 and M5. Gate leakage current of conventional seven Transistors SRAM is shown in Fig. 4.

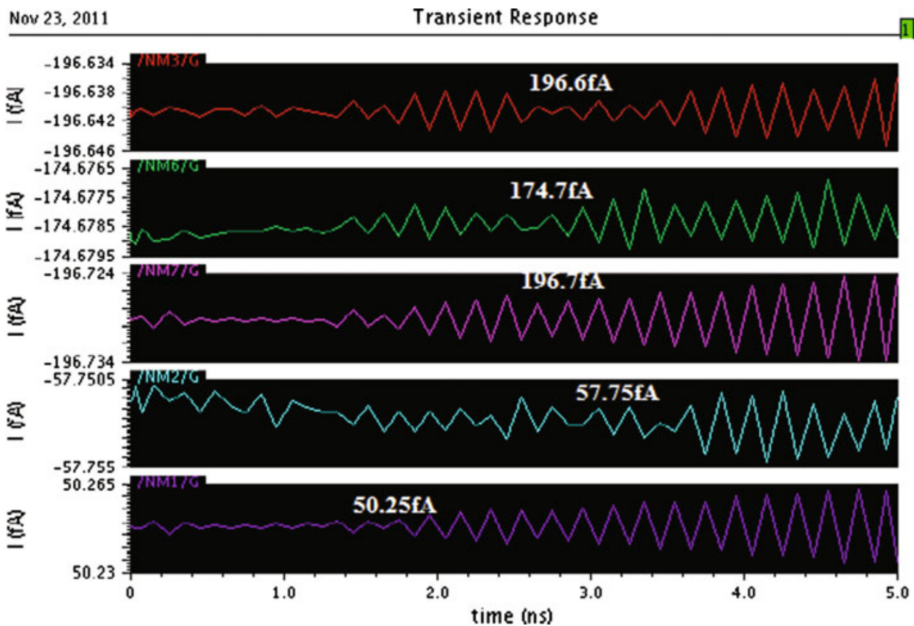

Fig. 4 Gate leakage currents in conventional 7T SRAM cell

4 Leakage Control in 7T SRAM Bit Cell

It was described earlier that self- controllable switch can be used either at the upper end of the cell to reduce supply voltage (USVL technique) or at the lower end of the cell to raise the voltage of the ground node (LSVL technique). The switching energy, the short-circuit energy, and the leakage current are assumed to remain constant under the same power supply [19]. The impact of these techniques on leakage currents is described in the next sections.

4.1 Leakage Control Using USVL

An SRAM cell consisting USVL techniques is shown in Fig. 5. In this technique, a full supply voltage is applied to SRAM cell in active mode, while the supply voltage level to SRAM is reduced to voltage level ‘Vd’ in stand-by mode. Since transistor M3 is in on state, voltage at the drains of M1 and M3 is also reduced to ‘Vd’. As before let us consider first the impact on gate leakage currents. As a result of a decrease in gate voltage of transistor M2, gate leakage current through it is sharply reduced. A decrease in drain voltage of transistor M1 results in lower gate-drain voltage across it and thus gate leakage current through it is also reduced. A decrease in source voltage of M6 results in a decrease in one component of EDT (Edge direct tunnelling) leakage across it while leaving the other unchanged. Gate leakage across transistor M5 remains unchanged. Transistor PU1 being a PMOS transistor does not result in any significant added leakage current as a result of transistors used in UVSL circuit. Gate leakage current is shown in Fig. 6.

USVL technique has a better effect on gate leakage current reduction. However, this technique is inferior with respect to sub threshold leakage current. While, sub threshold leakage

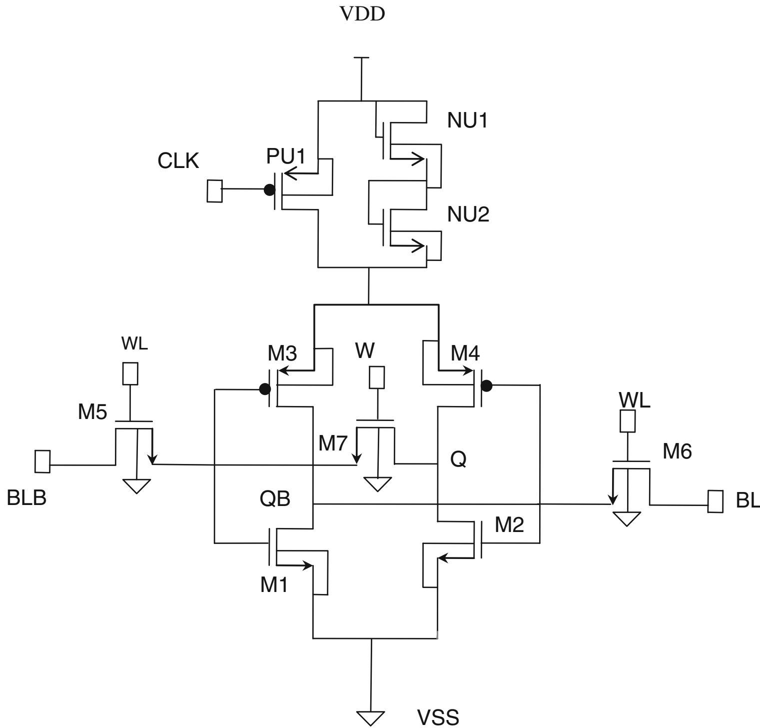

Fig. 5 Schematic of 7T SRAM cell after applying USVL technique

through transistors M1 and M4 is reduced, leakage across transistor M5 remains unchanged, as shown in Fig. 7. Further, a new sub threshold leakage current appears in transistor M6 as a result of reduction in its source voltage. To summarize, the USVL technique, while more successful in reducing gate leakage current, still leaves two gate leakage current components in access transistors unchanged. It also leaves one sub threshold current component in access transistor unchanged and results in an additional sub threshold leakage current across the other access transistor.

4.2 Leakage Control Using LSVL

Figure 8 shows a schematic of 7T SRAM cell in which LSVL technique is applied. The switch provides ‘0’ Volt at the ground node during the active mode and an increased ground voltage (virtual ground) during the stand-by mode.

This technique is similar to the diode footed cache design scheme proposed to control gate and sub-threshold leakages in SRAM cell, in which a diode designed with high Vt MOS transistors, was used to increase the ground voltage of SRAM in the stand-by mode [8].

Let us consider the effect of this technique on gate leakage. An increase in the virtual ground voltage (Vs) (as shown in Fig. 8), results in decrease of gate-source and gate-drain voltages of transistor M1 and gate-drain voltage of transistor M2 and results in sharp reduction in gate leakage currents of these two transistors. However, there is no improvement

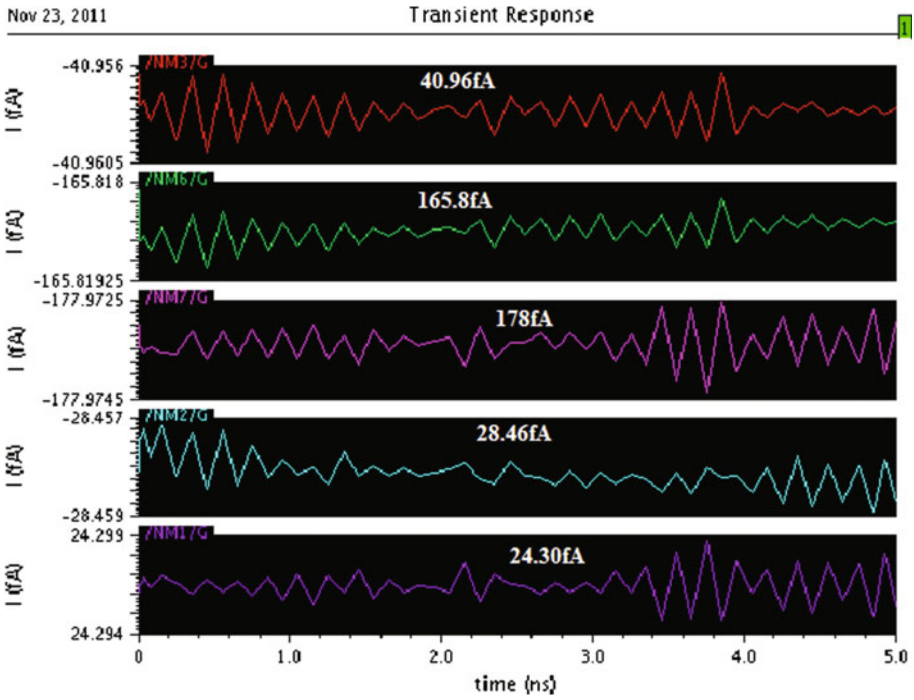

Fig. 6 Gate leakage currents in 7T SRAM cell after applying USVL technique

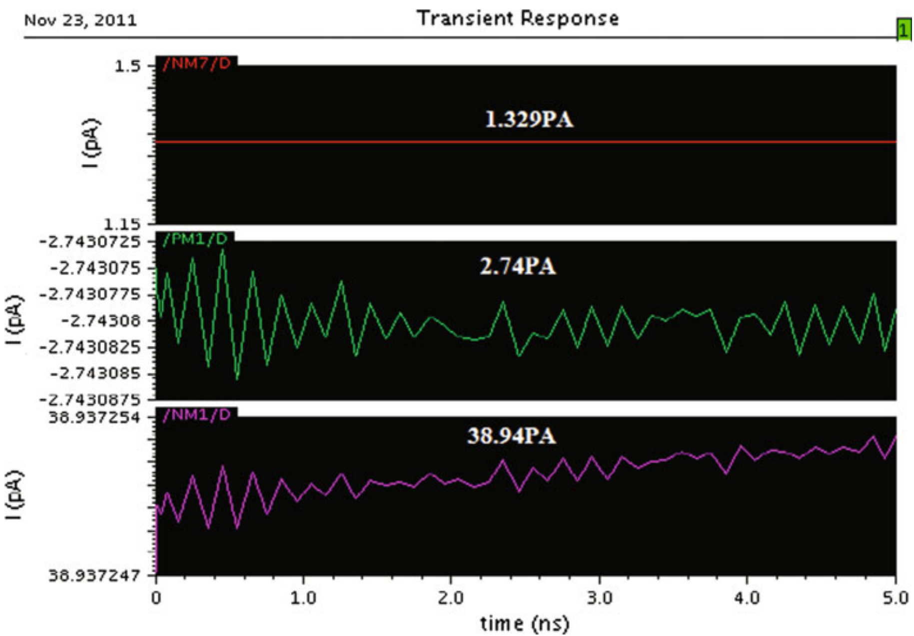

Fig. 7 Sub threshold leakage current in 7T SRAM cell after applying USVL technique

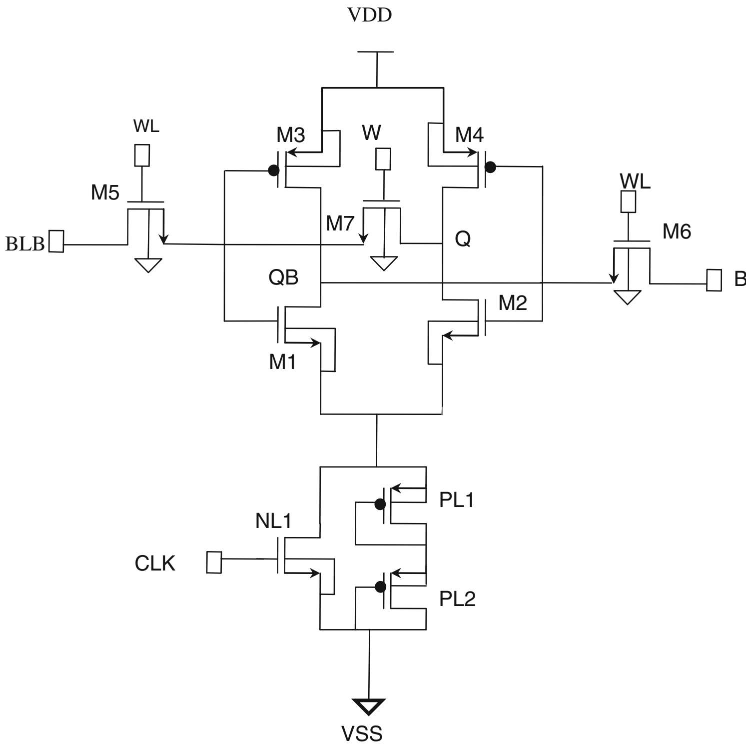

Fig. 8 Schematic of 7T SRAM cell after applying LSVL technique

in gate leakage currents for transistors M5 and M6. In fact, as a result of increase in drain voltage of M2, a new gate leakage current appears in transistor M7 as indicated in Fig. 9.

Incorporation of SVL results in another new gate leakage current through NMOS transistor NL1 in the SVL switch. As far as sub threshold leakage currents are concerned, LSVL approach is successful in reducing currents through M1, M4 and M5 as well. To summarize, one note that while all sub threshold currents are reduced using LSVL approach, it is only partially successful in reducing gate leakage currents. Sub threshold leakage current waveform is shown in Fig. 10.

4.3 Leakage Control Using Combined Technique (USVL plus LSVL)

Figure 11 shows the schematic of mixed technique (e.g. LSVL plus USVL). In this technique LSVL and USVL both are connected to the conventional seven transistors SRAM. By using this technique supply voltage is reduced to 0.348 V and ground voltage is increased up to 0.234 V.

By using this technique gate leakage current of the SRAM bit cell is reduced upto 437 FA, is shown in Fig. 12. Sub threshold leakage current of the SRAM bit cell is reduced upto 11.92 FA, which is shown in Fig. 13.

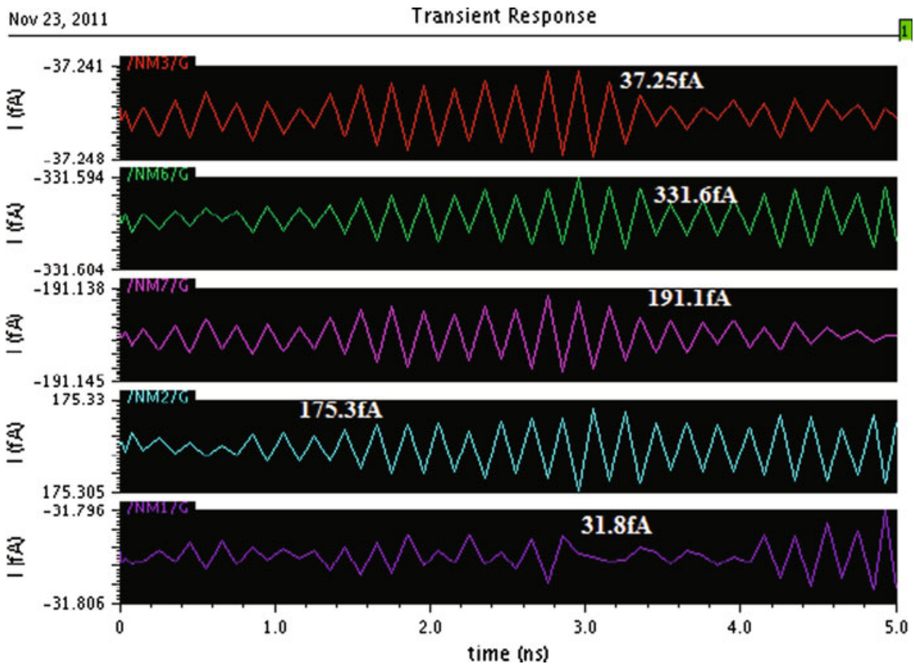

Fig. 9 Gate leakage currents in 7T SRAM cell after applying LSVL technique

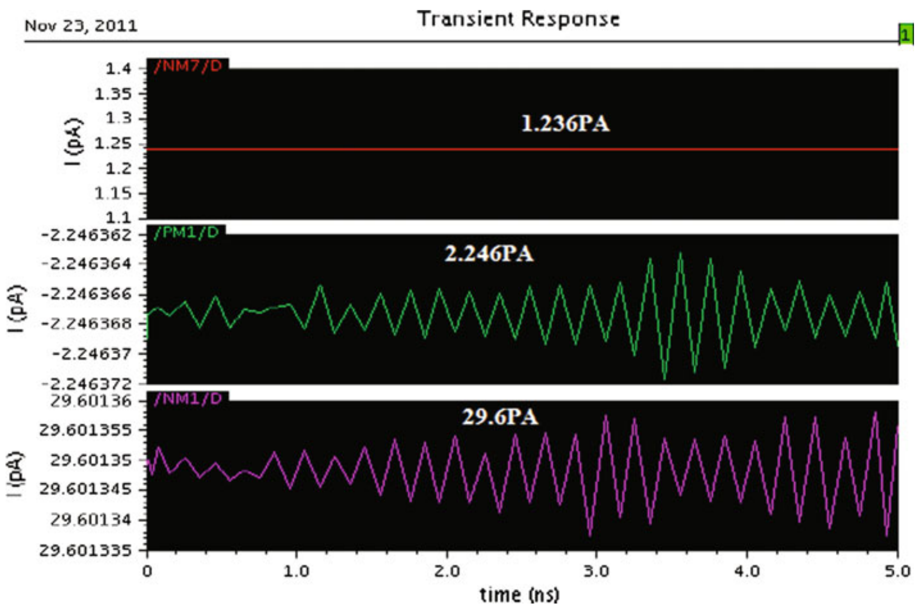

Fig. 10 Sub threshold leakage currents in 7T SRAM cell after applying LSVL technique

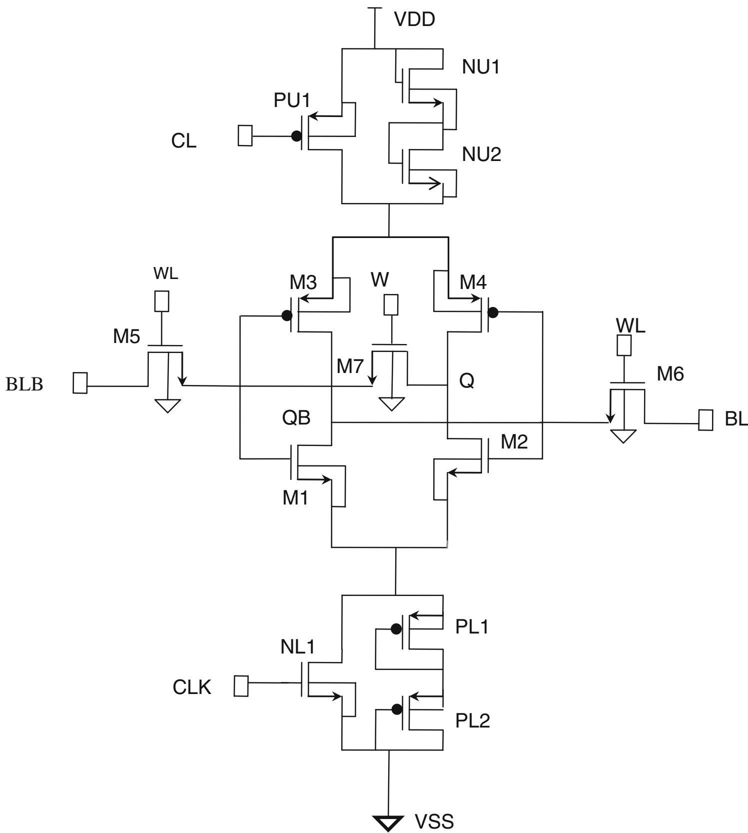

Fig. 11 Schematic of 7T SRAM cell after applying both techniques

5 Advantage of SVL Techniques

There are very important advantages of the SVL circuit. When the SRAM circuit are in active mode, the SVL circuit supplies maximum drain-source voltage Vds to the on MOS through on Switch, thus the SRAM circuit can operate quickly. On the other hand, when the SRAM circuit are in stand-by mode, it supplies slightly lower Vd and slightly higher Vs to MOS transistor through "weakly on switch", thus the SVL circuit not only retains data but also produces high noise immunity with minimal overheads in terms of silicon area. Furthermore the Vth increase and consequently sub threshold current (Isub) of the "off MOS" transistor decrease, so stand-by power Pst is greatly reduced.

6 Simulation Results and Discussion

The simulation of 7T SRAM cell has been done using Cadence Virtuoso tool at 45 nm technology. Although the circuit is simulated under ideal condition, there are various constrains on simulation parameter like transistor length and width, temperature effect, etc on the 7T SRAM cell. The leakage currents in conventional 6T SRAM cell and 7T SRAM cell as per

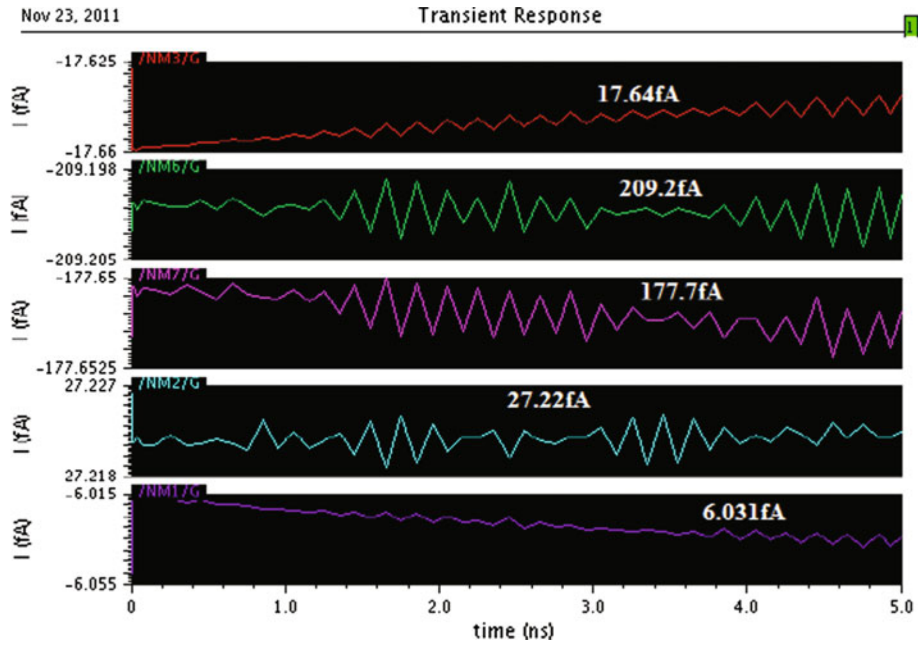

Fig. 12 Gate leakage currents in 7T SRAM cell after applying both techniques

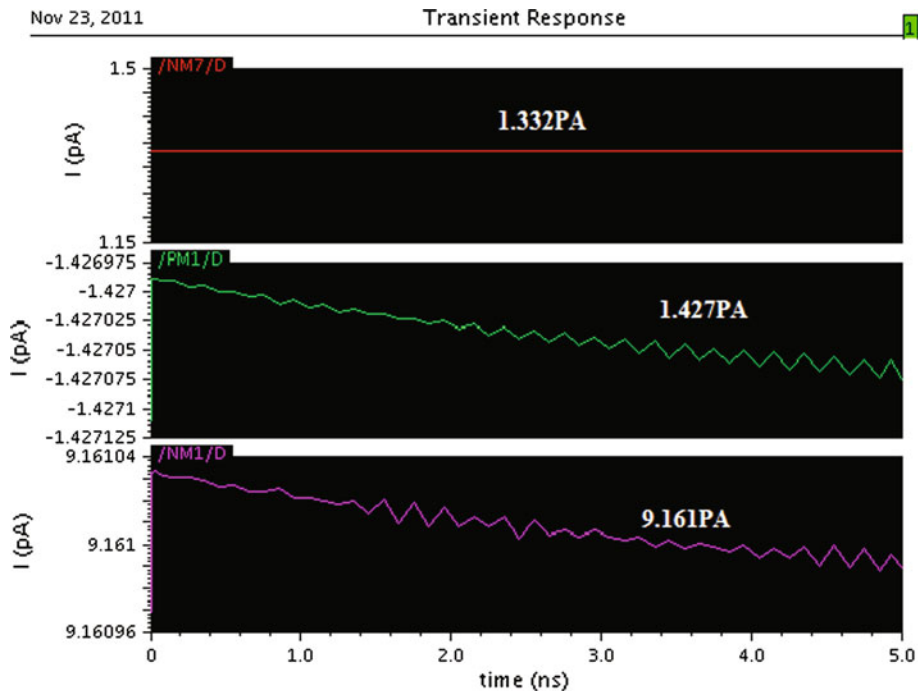

Fig. 13 Sub threshold leakage currents in 7T SRAM cell after applying both techniques

Table 1 Leakage current in 7T SRAM cell for different SVL techniques at temperatures of 27 °C

	M1		M2	M4	M5		M6	M7	Total Igate (FA)	Total Isub (PA)
	Igate (FA)	Isub (PA)	Igate (FA)	Isub (PA)	Igate (FA)	Isub (PA)	Igate (FA)	Igate (FA)		
Conv.	50.25	26460	57.75	910.39	196.7	1.207	174.7	196.6	676	27370.67
USVL	24.30	38.94	28.46	2.74	178	1.329	165.8	40.96	437.52	43.009
LSVL	31.8	29.6	175.3	2.246	191.1	1.236	31.6	37.25	467.05	33.082
USVL + LSVL	6.031	9.161	27.22	1.427	177.7	1.332	209.2	17.64	437.791	11.92

Table 2 Leakage current in 6T SRAM cell for different SVL techniques at temperatures of 27 °C

	M1	M2		M3	M5		M6	Icell (nA)
	Igate (nA)	Igate (nA)	Isub (nA)	Igate (nA)	Igate (nA)	Isub (nA)	Igate (nA)	
Conv.	37.1	13.92	0.86	0.56	9.84	0.6	19.56	83.6
USVL	2.38	1.14	0.58	–	9.84	0.6	10.64	25.51
LSVL	2.35	1.08	0.17	0.29	10.68	–	19.44	33.6
USVL + LSVL	2.78	1.14	0.58	–	0.32	0.32	1.2	5.49

the techniques suggested in Sects. 4.1, 4.2 and 4.3 at temperature of 27 °C are shown in Tables 1 and 2. The gate leakage being the only prevailing mechanism at room temperature, LSVL techniques achieves a gate leakage current of 467.05 FA and total leakage current in 7T SRAM and 33.6 nA in 6T SRAM cell, while USVL technique without changing bit-line voltages provides a leakage reduction of 437.52 FA in 7T SRAM cell and 25.31 nA in 6T SRAM cell. The effective supply voltage across the 7T SRAM is reduced from 0.7 to 0.582 V. while combined technique provides 437.791 FA gate leakage current (Igate) and maximum reduction in sub threshold leakage current (Isub) 11.92 PA. At the elevated temperature sub threshold leakage increases dramatically and gate leakage current almost constant. USVL technique is more efficient in gate leakage suppression but because LSVL technique is better for sub threshold leakage reduction.

7 Conclusion

An analysis of gate leakage currents in 7T SRAM cells for a 45 nm technology shows that both gate and sub threshold leakage currents contribute significantly to overall leakage power dissipation in stand-by mode. Reduction in supply voltage and increase in ground voltage using self-controllable voltage level switches for reducing leakage currents in 7T SRAM is examined in detail. It is found that while the LSVL approach is better in terms of reduction in sub threshold leakage current (Isub), the USVL approach performs better with respect to gate leakage currents (Igate). However, both these techniques are found to be inadequate for reduction of leakage currents through access transistors. A modified USVL + LSVL approach in which access transistors are put in off state during the stand-by mode is found to be very effective in reducing all significant components of leakage currents. Results show that 437.791 FA and 11.92 PA reductions in the total sub threshold leakage currents are achieved at 27 °C. In 6T SRAM cell we have got total leakage current 5.49 nA. So we can conclude that 7T SRAM cell is better as compared to 6T SRAM cell.

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