Journal of Signal Processing Systems (2022) 94:1293–1308
https://doi.org/10.1007/s11265-021-01648-0

A Survey on Application Specific Processor Architectures for Digital Hearing Aids

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Received: 7 August 2020 / Revised: 7 August 2020 / Accepted: 4 February 2021 / Published online: 20 March 2021

Abstract
On the one hand, processors for hearing aids are highly specialized for audio processing, on the other hand they have to meet challenging hardware restrictions. This paper aims to provide an overview of the requirements, architectures, and implementations of these processors. Special attention is given to the increasingly common application-specific instruction-set processors (ASIPs). The main focus of this paper lies on hardware-related aspects such as the processor architecture, the interfaces, the application specific integrated circuit (ASIC) technology, and the operating conditions. The different hearing aid implementations are compared in terms of power consumption, silicon area, and computing performance for the algorithms used. Challenges for the design of future hearing aid processors are discussed based on current trends and developments.

Keywords Survey · Hearing aid · Processor · ASIP · ASIC

1 Introduction

Modernhearing aids, like the one shown in Fig. 1, have to meeta variety of technical requirements. First of all, the power consumption of hearing aids is limited. To achieve an acceptable battery life, the average power consumption of hearing aids should be in the range of a few milliwatts. The reason for the low energy budget is the small physical size of battery-powered hearing aids. At the same time, the demand for more audio processing performance and memory capacity is steadily growing. There are newly developed algorithms with more or improved features and increasing demands on audio quality. In addition, it is required that hearing aids can be individually fitted to the hearing aid user, adapt to constantly changing environmental conditions, and connect wirelessly to other electronic devices. These requirements and the high degree of flexibility and programmability make the hardware design for hearing aid devices challenging.

Figure 2 shows the system components and peripherals of a state-of-the-art hearing aid. Typically, hearing aids contain a central processing unit that provides the functionality and connects all other components such as the receiver and microphones. The design and implementation of the processor is challenging and involves numerous trade-offs due to the wide range of requirements and the large design space. The implementation alternatives in a multi-dimensional design space are shown in Fig. 3. Various hearing aid processor architectures and implementations were introduced in the literature. There are analog, mixed-signal, or purely digital hearing aids. Some use hard-wired processing and control circuits, others use fully programmable application-specific instruction-set processors (ASIPs) with custom instructions and hardware accelerators. This survey compares these hearing aids from a hardware perspective.

The main focus of related work, i.e., technical studies, surveys or overview papers, addressing the hearing aid signal processing, is on current and future hearing aid algorithms. The first related study [26] presents state-of-the-art signal processing in hearing aids. Among the studied techniques and algorithms are feedback reduction,

This article belongs to the Topical Collection: *Survey Papers*

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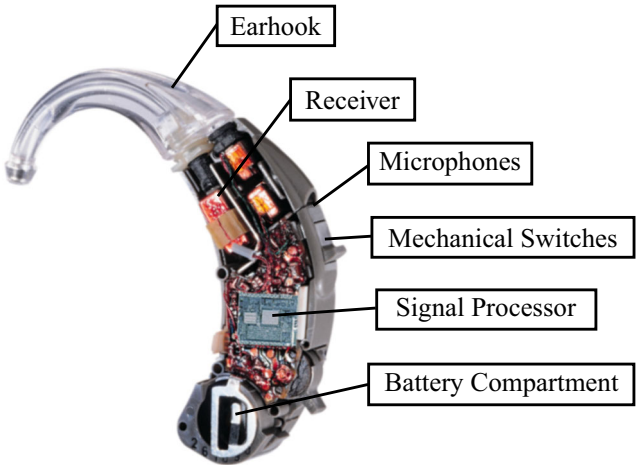

Figure 1 Components of a common behind the ear hearing aid device [11].

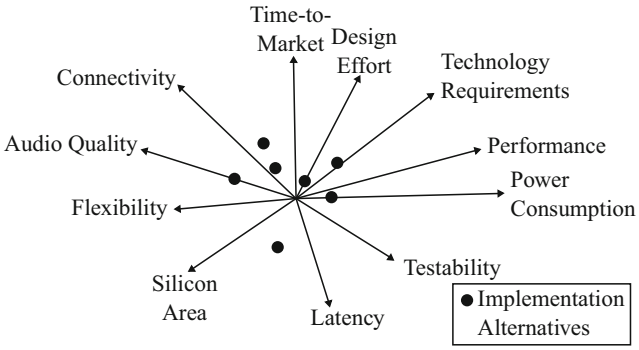

Figure 3 Implementation alternatives in a multi-dimensional design space.

directional microphones, environment recognition, and noise and distortion reduction. Current limitations as well as future trends like binaural and music processing are addressed. Binaural processing as a future hearing aid processing technique is also covered in the two surveys [21, 55] from 2005 and 2009. Both papers present state-of-the-art, challenges and future trends of signal processing in hearing aids. Physiological requirements due to hearing impairment are described as well as the different audio processing methods such as directional microphones, noise reduction, acoustic feedback suppression, classification, and compression. No related work focuses on the hardware perspective. Little information is given about the hardware architectures, circuit implementation, and the different design methods. This survey covers these hardware-related topics, including a review of the current processor architectures. A particular focus is on application-specific instruction-set processors (ASIPs).

The structure of this survey is as follows: Section 2 provides a list of the algorithms that are implemented on hearing aid processors, which are part of this survey. The hearing aid processors are described in detail in Section 3. The differences in the architecture of hard-wired and ASIP-based hearing aid processors are discussed. The remaining sections cover the ASIC technology and supply voltage (Section 4), power consumption (Section 5), silicon area (Section 6), operating clock frequency (Section 7), audio datapath width (Section 8) and on-chip memory in ASIP-based hearing aid systems (Section 9). Section 10 concludes this paper and points out possible future trends.

2 Algorithms for Hearing Aid Devices

A typical high-end hearing aid processing is shown as a block diagram in Fig. 4. Multiple microphones enable

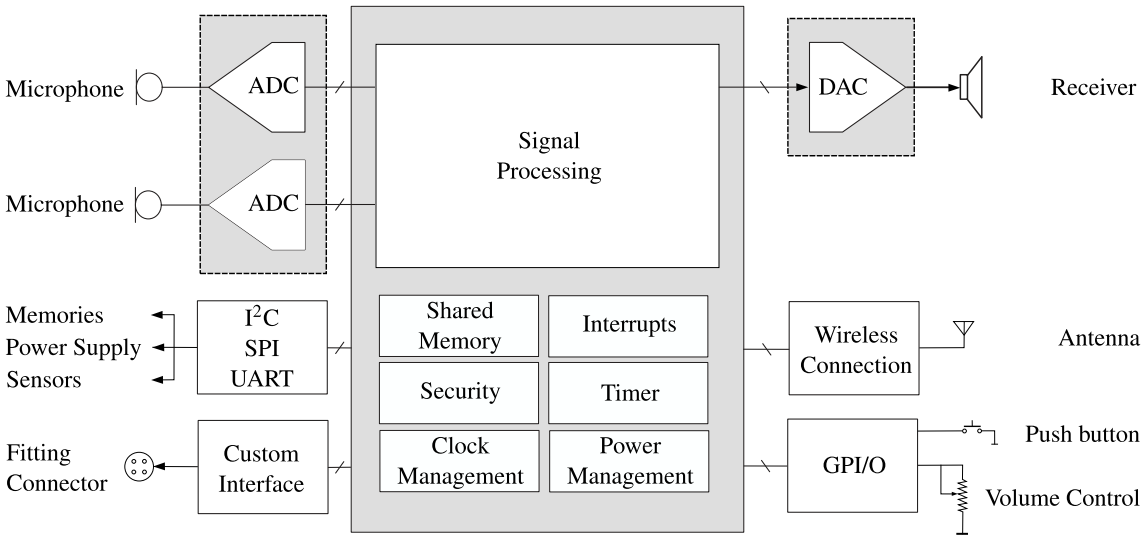

Figure 2 System components and peripherals of a modern hearing aid device [9, 63].

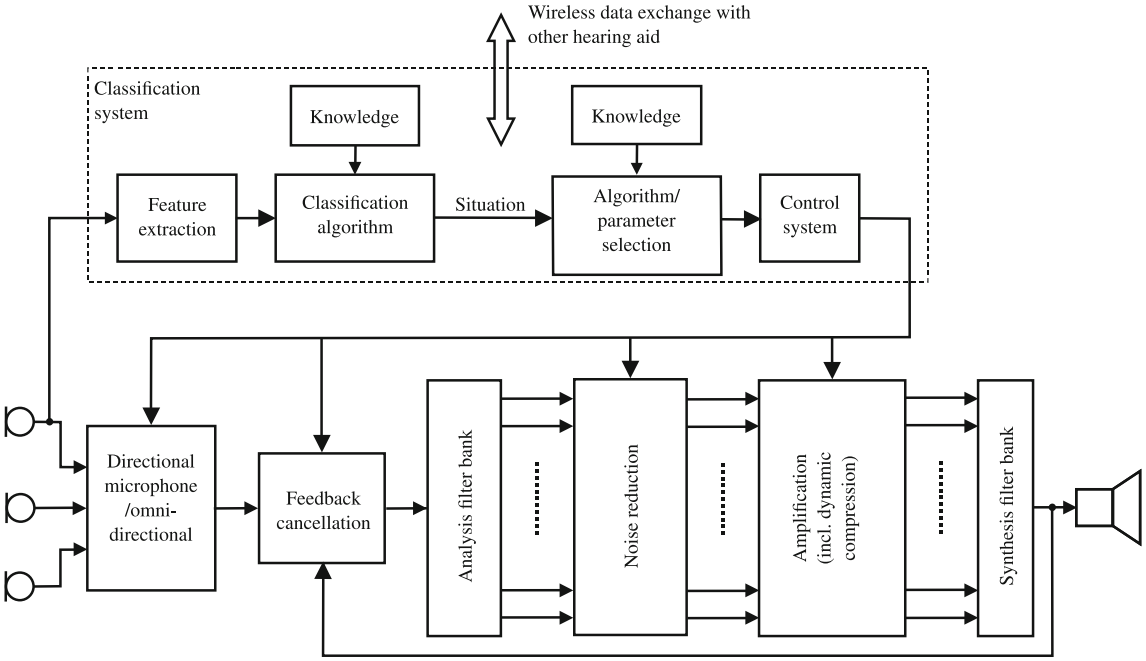

Figure 4 Block diagram of a typical hearing aid processing [22, 55].

directional filtering. Therefore, beamforming (BMF) and adaptive directional microphone (ADM) algorithms are the first in the chain and aim to increase the signal-to-noise ratio (SNR) by performing directional filtering. Feedback is then suppressed with a feedback cancellation (FBC) algorithm by analyzing the output signal and detecting feedback loops. The algorithms that process frequency domain data, such as the noise reduction (NR) and dynamic range compression (DRC) algorithms, require an analysis and synthesis filter bank. Classification algorithms generally generate control signals for the processing chain. A list of algorithms is included in Table 1. This list contains exclusively algorithms that are part of a processing chain in state-of-the-art hearing aids. Publications with the implementation, optimization, and application of these algorithms on the state-of-the-art hearing aid processors are also included in Table 1. There is a trend towards algorithms, that are computationally more demanding. In recent years, algorithms for machine learning and deep learning [40, 44, 52] and binaural processing algorithms [46] are used. Recently proposed algorithms of this kind [57, 67, 69], of which no implementation details on a hearing aid processor are known, are not listed in Table 1.

3 Hearing Aid Processor Architectures

In recent decades, various hearing aid processors have been proposed in the literature. All hearing aid processors are subject to comparable strict requirements regarding limited energy budget, available chip area, and performance requirements. However, a wide range of different architectures, algorithms, approaches, and technologies were introduced to meet these stringent requirements. 30 research and commercial processors published between 1996 and 2020 are listed in Table 2. This table provides a comparison of the architecture, ASIC technology, supply voltage, average power consumption, silicon area, and operating clock frequency of the various hearing aid systems.

The processor architectures are designed and optimized to efficiently execute particular hearing aid algorithms listed in Table 1. The architectures of these processors can be divided into three main classes: hard-wired with dedicated processing blocks, ASIPs, and ASIPs with hardware accelerators.

3.1 Hard-Wired Architectures

In case of a hard-wired architecture, all parts of the hearing aid processing chain are implemented by dedicated circuits. Their fundamental function is fixed and can only be changed before manufacturing. There are pure analog [45, 64, 70], mixed-signal [12, 17, 30–32], or pure digital [3, 65, 71, 72, 74] hard-wired hearing aids.

A digital hard-wired hearing aid is highlighted in the following. This dedicated architecture, originally proposed in [72] and published in 2014, is characterized by its flexibility compared to related architectures. It includes a core-based architecture consisting of a memory management unit for data exchange, a control unit, and an arithmetic unit for processing. Therefore, processing is easier to control

Table 1 List of algorithms, which are applied by the related work in hearing aid processors.

Year	Title of the algorithm publication	Class	Application
1982	An alternative approach to linearly constrained adaptive beamforming [20]	Beamforming (BMF)	[41, 56]
1984	Speech enhancement using a minimum-mean square error short-time spectral amplitude estimator [14]	Speech enhancement (SE)	[5]
1985	Speech enhancement using a minimum mean-square error log-spectral amplitude estimator [15]	Noise reduction (NR)	[9]
1995	Noise estimation techniques for robust speech recognition [23]	Noise reduction (NR)	[56]
1996	Speech enhancement based on a priori signal to noise estimation [59]	Speech enhancement (SE)	[56]
1997	Comparison of voice activity detection algorithms for wireless personal communications systems [13]	Voice Activity Detector (VAD)	[65]
1997	Adaptive digital filter in subbands: Design issues and experimental results for acoustic echo cancellation [16]	Feedback cancellation (FBC)	[33]
1999	A novel approach of adaptive feedback cancellation for hearing aids [10]	Feedback cancellation (FBC)	[9, 25]
2001	First-and second-order adaptive differential microphone arrays [68]	Adaptive directional microphone (ADM)	[3]
2001	Hearing aid digital filter [66]	Digital filter	[17, 30–32, 65, 74]
2001	Assessing local noise level estimation methods: Application to noise robust ASR [58]	Noise reduction (NR)	[5]
2002	Digital envelope detector for blood pressure measurement using an oscillometric method [38]	Adaptive SNR Monitor	[74]
2002	An improved entropy-based endpoint detection algorithm [24]	Voice Activity Detector (VAD)	[72]
2002	A multi-band spectral subtraction method for enhancing speech corrupted by colored noise [27]	Noise reduction (NR)	[9, 25, 33]
2002	Adaptive Null-Forming Scheme in Digital Hearing Aids [43]	Beamforming (BMF)	[19]
2005	Principles of digital dynamic-range compression [29]	Dynamic range compression (DRC)	[56]
2005	Speech enhancement for personal communication using an adaptive gain equalizer [73]	Speech enhancement (SE)	[19]
2006	New insights into the noise reduction Wiener filter [7]	Noise reduction (NR)	[9, 25]
2007	Speech enhancement: theory and practice [42]	Noise reduction (NR)	[72]
2008	Complexity-effective auditory compensation for digital hearing aids [36]	Dynamic range compression (DRC)	[71]
2008	Digital Hearing Aids: Feedback Cancellation [28]	Feedback cancellation (FBC)	[5]
2008	Digital Hearing Aids: Dynamic Range Compression [28]	Dynamic range compression (DRC)	[5, 9, 25, 33]
2008	Digital Hearing Aids: Directional Microphones & Adaptive and Multimicrophone Arrays [28]	Adaptive Directional Microphone (ADM)	[5]
2011	A probabilistic model for robust localization based on a binaural auditory front-end [46]	Sound source localization (SSL)	[19]
2013	Effect of individually tailored spectral change enhancement on speech intelligibility and quality for hearing-impaired listeners [8]	Speech enhancement (SE)	[41]
2013	Adaptive signal processing: applications to real-world problems [1]	Feedback cancellation (FBC)	[56]
2016	A fully convolutional neural network for speech enhancement [52]	Speech enhancement (SE)	[53, 54]
2017	Plastic multi-resolution auditory model based neural network for speech enhancement [37]	Speech enhancement (SE)	[40]
2019	DNN-based performance measures for predicting error rates in automatic speech recognition and optimizing hearing aid parameters [44]	Speech recognition (SR)	[19]

Table 2 Hearing aid processors and systems.

Year	Title of the publication	Proc. Arch.	Analog front end	Tech. [nm]	Supply [V]	Power [mW]	Area [mm^2]	Clock [MHz]
1996	VERDI: An acoustically programmable and adjustable CMOS mixed-mode signal processor for hearing aid applications [12]	hard-wired	yes	1200	1.30	1.300	28.00	0.200
1997	A DSP-Based Hearing Instrument IC [49, 50]	ASIP	yes	800	1.30	1.950	35.00	1.024
1999	A CMOS Hearing Aid Device [45]	hard-wired	yes	1200	1.40	0.100	1.10	0.640
1999	Algorithm and architecture of a 1 V low power hearing instrument DSP [47]	ASIP	no	500	1.00	0.800	28.00	2.000
2000	A 660-μW 50-Mops 1-V DSP for a Hearing Aid Chip Set [48]	ASIP	no [34]	250	1.05	0.660	20.00	2.500
2001	A heterogeneous multiprocessor architecture for low-power audio signal processing applications [51]	ASIP+acc.	no	250	1.00	0.011	5.00	0.192
2003	A 1.1-V 270-μA Mixed-Signal Hearing Aid Chip [17]	hard-wired	yes	600	1.10	0.290	12.00	2.560
2004	A True-1-V 300-μW CMOS-Subthreshold Log-Domain Hearing-Aid-On-Chip [64]	hard-wired	yes	120	1.00	0.300	7.50	0.150
2005	A 0.67-mm^2 45-μW DSP VLSI Implementation of an Adaptive Directional Microphone for Hearing Aids [3]	hard-wired	no	250	1.25	0.045	0.67	—
2006	A 10-μW digital signal processor with adaptive-SNR monitoring for a sub-1 V digital hearing aid [74]	hard-wired	no	180	0.90	0.010	0.30	0.064
2006	A 0.9-V 96-μW Digital Hearing Aid Chip with Heterogeneous Σ-Δ DAC [30]	hard-wired	yes	180	0.90	0.096	2.70	0.032
2007	A 0.9 V 96 μW Fully Operational Digital Hearing Aid Chip [31]	hard-wired	yes	180	0.90	0.096	3.08	0.032
2008	A fully integrated digital hearing aid chip with human factors considerations [32]	hard-wired	yes	180	0.90	0.107	3.74	0.032
2010	A low-power Mandarin-specific hearing aid chip [71]	hard-wired	no	90	0.60	1.095	3.10	8.000
2011	A 0.964 mW digital hearing aid system [56]	ASIP	no	65	0.80	0.964	0.49	11.000
2012	A Low Power Hearing Aid Computing Platform Using Lightweight Processing Elements [4]	ASIP+acc.	no	65	0.80	1.300	3.60	10.000
2013	Low-power digital signal processor design for a hearing aid [65]	hard-wired	no	180	0.90	0.025	0.50	0.032
2013	High Performance Hearing Aid System with Fully Programmable Ultra Low Power DSP [35]	ASIP	no	130	1.00	0.863	—	8.000
2014	Analysis and implementation of low-power perceptual multiband noise reduction for the hearing aids application [72]	hard-wired	no	90	0.60	0.083	1.53	6.000
2014	A programmable analog hearing aid system-on-chip with frequency compensation [70]	hard-wired	yes	130	1.00	1.600	5.24	—
2014	A sub-milliwatt audio-processing platform for digital hearing aids [25]	ASIP+acc.	yes	130	1.00	0.860	9.50	8.000
2015	A 1-V, 1.2-mA fully integrated SoC for digital hearing aids [9]	ASIP+acc.	yes	130	1.00	1.200	9.50	8.000
2016	A 1V, 1.1 mW mixed-signal hearing aid SoC in 0.13 um CMOS process [6]	ASIP+acc.	yes	130	1.00	1.100	9.30	8.000
2018	Wireless-Enabled Audio Processor for Hearing Aids [63]	ASIP+acc.	yes	65	1.18	0.870	—	10.240
2018	A 79-dB SNR 1.1-mW Fully Integrated Hearing Aid SoC [5]	ASIP+acc.	yes	130	1.00	1.100	9.30	2.000
2018	A 9-mm^2 ultra-low-power highly integrated 28-nm CMOS SoC for Internet of Things [54]	ASIP+acc.	no [53]	28	0.55	4.000	9.00	50.000
2019	High-performance DSP platform for digital hearing aid SoC with flexible noise estimation [33]	ASIP+acc.	no	65	1.00	1.300	2.71	8.000
2019	KAVUAKA: A Low Power Application Specific Hearing Aid Processor [19]	ASIP+acc.	no	40	1.10	0.600	3.60	10.000
2020	A 2.17-mW Acoustic DSP Processor With CNN-FFT Accelerators for Intelligent Hearing Assistive Devices [40]	ASIP+acc.	no	40	0.60	2.170	4.20	20.000
2020	A 1.5 mW Programmable Acoustic Signal Processor for Hearing Assistive Devices With Speech Intelligibility Enhancement [41]	ASIP+acc.	no	40	0.70	1.500	0.30	10.500

compared to related architectures. Its block diagram, architecture, and die photo are shown in Fig. 5. The authors of [72] propose a sample-based perceptual multiband noise reduction algorithm as a basis for the design of a dedicated digital hearing aid architecture. This noise reduction algorithm is part of the hearing processing chain and is represented as a block diagram in Fig. 5. An analysis and synthesis filter bank (AFB and SFB), a noise reduction (NR) algorithm [24, 42], an insertion gain (IG), and wide dynamic range compression (WDRC) are integrated on the hearing aid chip. The average power consumption is 83.7 μW. A 90 nm ASIC technology is used and the digital core voltage is 0.6V.

3.2 Application-Specific Instruction-Set Processors

Application-specific instruction-set processor (ASIP) architectures include a digital signal processor (DSP) for signal processing [35, 47–50, 56]. The DSP architecture is optimized for the typical hearing aid algorithms, therefore it is here also denoted as an (ASIP). The target algorithms can be modified or replaced by changing the program code. This offers greater flexibility compared to hard-wired architectures. However, due to the higher flexibility offered by the processor architecture and the increased memory requirements, the power consumption and silicon area requirements are generally higher compared to hard-wired architectures. Instruction-level and data-level optimizations improve the efficiency of signal processing. New custom instructions increase processing performance.

A hearing aid with a DSP for signal processing is presented in [48] and its block diagram and photo are shown in Fig. 6. This hearing aid publication is highlighted as the authors propose an algorithm to silicon flow in addition to the proposed hearing aid chip. This flow is integrated into the chip design flow and supports accurate and fast simulations, ASIC synthesis, optimization and verification [48]. These tools are useful for handling the overall complexity and drastically decrease the design time, if the underlying ASIC technology is changed. The DSP architecture consists of a datapath with several general purpose execution units, a complex-valued multiplier, and a controller with a program read-only memory. The operating clock frequency of the DSP is reduced by increased parallelism and reduced memory accesses. A fast Fourier transform (FFT) algorithm case study for the architecture shows how a radix-8 implementation can minimize memory accesses and increase the number of parallel operations. Over 20 operations per cycle are achieved. In addition to clock gating and low voltage operation techniques, the authors propose to partition the datapath and the read-only memory (ROM) of the complete architecture. The underlying concept is that there are different types of operations that do not require the same

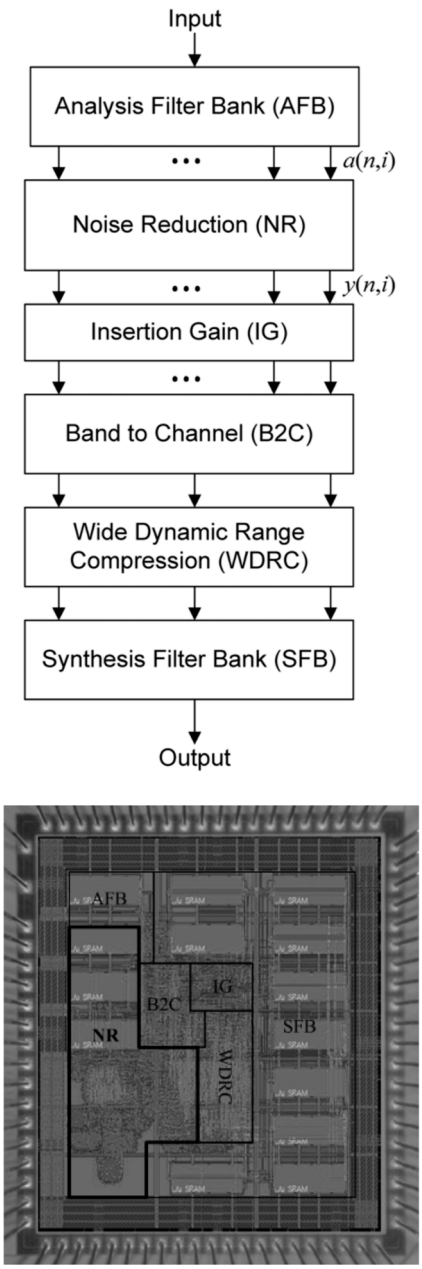

Figure 5 Block diagram and die photo of a hard-wired hearing aid [72] (Republished with permission of Institution of Engineering and Technology (IET), from [72]; permission conveyed through Copyright Clearance Center, Inc.).

hardware resources. This partitioning is implementedfor reasons of power consumption optimization and depends on the operation mode: FFT and non-FFT. Consequently, one of the ROMs needs to be accessed in each clock cycle, which reduces the power consumption of the DSP by about 40%. The DSP, the instruction read-only memorys (ROMs), and the parameter static random-access memorys (SRAMs) are integrated in one hearing aid chip. The final chip consumes on average 0.66 mW at a core voltage of 1.05 V.

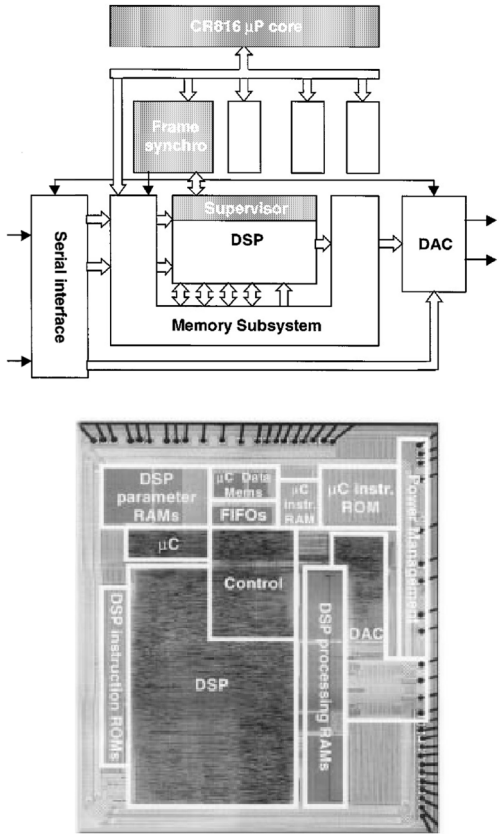

Figure 6 Block diagram and die photo of an ASIP hearing aid [48] (© 2020 IEEE. Reprinted, with permission, from [48]).

The analog front end including a digital-to-analog converter (DAC), programmable gain amplifier, and a serial interface are integrated on a separate chip [34].

3.3 ASIPs with Hardware Accelerators

There are hearing aid processing architectures that combine ASIPs with dedicated hard-wired accelerators. These accelerators are used for frequent and computationally intensive tasks. The flexibility and complexity of these accelerators varies. A list of accelerators for hearing aids can be found in Table 3. The hearing aid processing task is mapped to either the ASIP or the accelerator. The goal is to process the intensive computing tasks on the accelerator, while the ASIP performs computations in parallel and controls the accelerator processing [54].

The block diagram of a highlighted ASIP with accelerators [19] is shown in Fig. 7. The corresponding layout view is shown in Fig. 8. This research hearing system on chip contains four ASIPs on one chip to test different processor and algorithm configurations for processing performance and power efficiency. The ten co-processors, which can be used in parallel, accelerate the computation of the coordinate rotation digital computer (CORDIC) algorithm for hyperbolic and trigonometric functions such as sine, cosine, square root, exponential, tangent, and division with an average speed-up of 28 compared to a software implementation on the ASIP. The ASIP can configure several accelerators with different operating modes to calculate different results in parallel.

Using the same hardware accelerator for different audio signal processing tasks is also applied in other related work. In [40], an arithmetic unit with a dual MAC and butterfly unit can operate either in FFT mode or in CNN mode. By sharing hardware resources, 42% of hardware complexity can be saved. In [54], a streaming DSP hardware accelerator is introduced that can compute applications such as keyword recognition or other algorithms for classifications. Any of the co-processors in [19] can be disabled by clock gating, however, these operations are elementary and are often used in hearing aid applications. This also applies to the FIR filter accelerators presented in [4, 51]. The accelerators presented in [4–6, 9, 25, 33, 63] are more complex and specific, because they implement complete algorithms, such as noise reduction (NR), feedback cancellation (FBC) or

Table 3 List of hardware accelerators for hearing aids.

Work	Accelerator
[4, 51, 63]	Finite impulse response (FIR) filter accelerators
Lee et al. [40]	Convolutional neural networks (CNN) and fast Fourier transform (FFT) accelerators for speech enhancement
Pu et al. [54]	Streaming DSP for voice code word detection
Gerlach et al. [19]	Co-processors for hyperbolic and trigonometric functions
Lin et al. [41]	Noise reduction (NR) accelerator
Lin et al. [41]	Multiply-accumulate (MAC) unit accelerator
Lin et al. [41]	Fast Fourier transform (FFT) accelerator
[4–6, 9, 25, 33, 63]	Analysis filter bank (AFB) accelerator
[4–6, 9, 25, 33, 63]	Noise reduction (NR) accelerator
[4–6, 9, 25, 33, 63]	Feedback cancellation (FBC) accelerator
[4–6, 9, 25, 33, 63]	Wide dynamic range compression (WDRC) accelerator

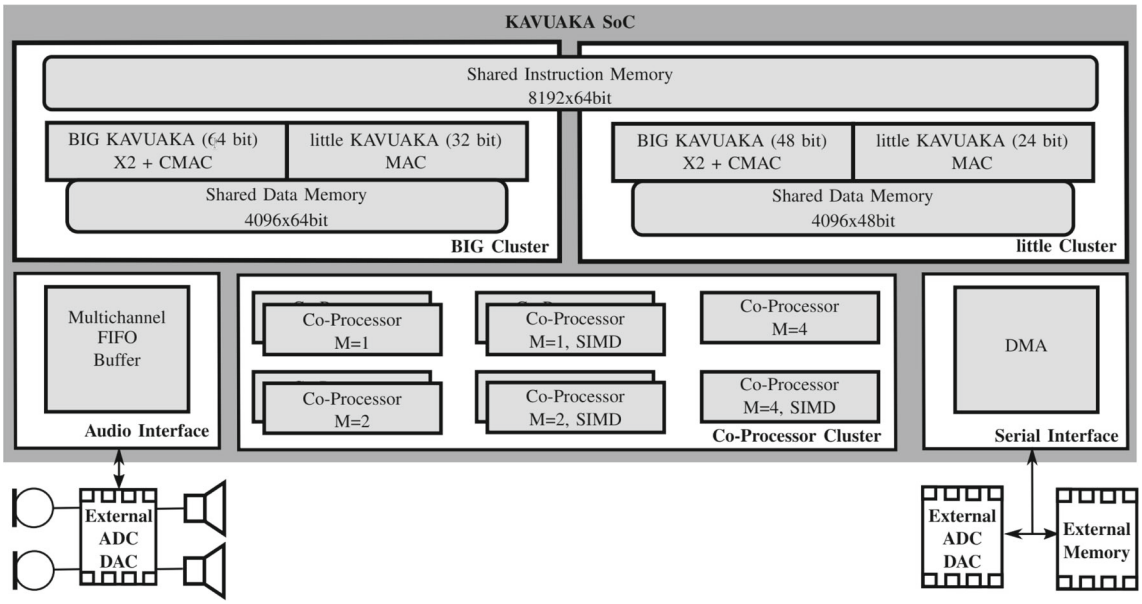

Figure 7 Block diagram of a hearing aid including multiple ASIPs and hardware accelerators [19] (© 2020 IEEE. Reprinted, with permission, from [19]).

others, in hardware. One advantage is the efficiency gained by the hard-wired implementation. If an algorithm needs to be changed, it is possible to use ASIP processing resources instead of the accelerators.

4 ASIC Technology and Supply Voltage

The advantages of the steadily decreasing feature sizes of CMOS semiconductor technology are exploited in commercial and research hearing aids. The feature sizes of modern hearing aids from 1996 to 2020 are shown in Fig. 9.

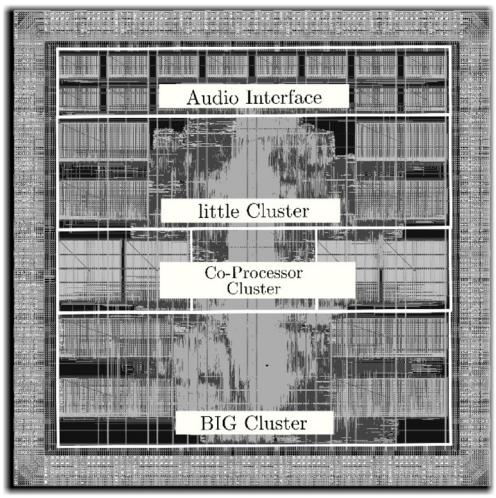

Figure 8 Layout view of an ASIP with hardware accelerators hearing aid [19] (© 2020 IEEE. Reprinted, with permission, from [19]).

Hearing aids with an analog front end (AFE), including analog-to-digital converters (ADCs), programmable gain amplifiers (PGAs), or digital-to-analog converters (DACs), are marked. These hearing aids are either mixed-signal or analog hearing aid designs, which have on average larger feature sizes due to more restrictive design rules and greater sensitivity to noise [61]. To overcome these limitations, the authors of [19, 34, 48, 53] propose a chip-level integration with two separate chips. Each chip is integrated with a different ASIC technology, to independently utilize the more appropriate feature size for both, the digital and the analog components of the hearing aid. The rate, at which the feature size shrinks, decreased significantly for hearing aid implementations in recent years. This is due to the higher costs for the design and manufacturing with smaller feature sizes [61]. The supply voltages of hearing aid implementations are shown in Fig. 10. Since the feature size remained almost constant over the last years (Fig. 9), the supply voltage also remains almost constant (Fig. 10). This is especially noticeable for hearing aids with analog components. The lowest supply voltages of 0.55 V to 0.8 V are used in digital hearing aid designs. Those hearing aid implementations, that employ undervoltage techniques through dynamic voltage scaling and use voltages close to the threshold voltage, are listed in Table 4.

5 Power Consumption

The average power consumption determines the battery life of the hearing aids. During normal operation, all components

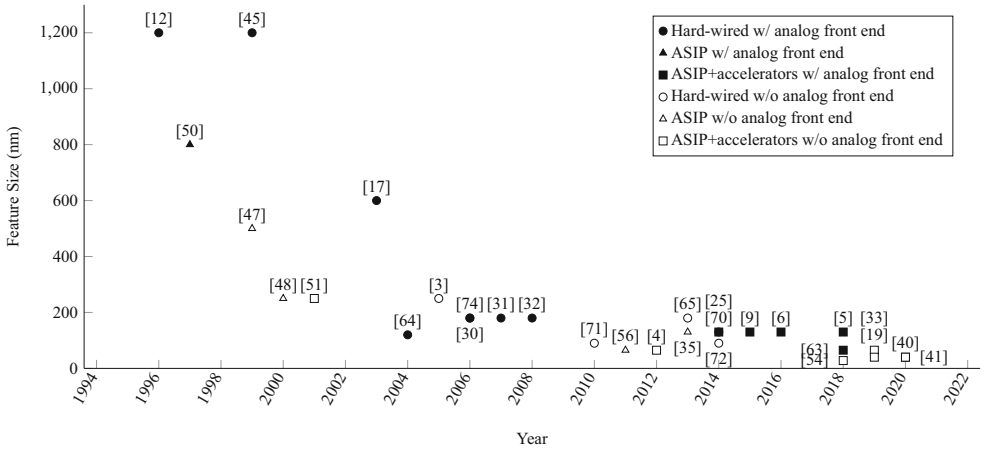

Figure 9 Feature sizes of commercial and research hearing aids.

of the hearing aid processing system are usually constantly active. The average power consumption for the hearing aid implementations is shown in Fig. 11. The computational complexity of the algorithms determines, among other things, the power consumption. The lowest achieved average power consumption for the given implementations is 10 μW. The hearing aids [74] and [51] consume this power for an adaptive signal-to-noise ratio (SNR) monitor based on an envelope detection and adaptive FIR and IIR filter calculations. On the other hand, when targeting hearables or smart headphones instead of hearing aid devices, deep-learning based noise reduction techniques require an average power consumption up to 4 mW [54]. Hard-wired architectures offer a comparatively low-power consumption compared to the ASIP architectures. The power distribution for the hardware components of the mixed-signal hearing aid [5] is 36% for the analog front end, 39% for the digital signal processor (DSP), 11% for the power on reset circuit and 13% for the remaining components. The digital signal processor of the hearing aid presented in [9], on the other hand, consumes up to 71%, while the analog parts consume the remaining 29%.

6 Silicon Area

The silicon area for each hearing aid is shown in Fig. 12. The analog front-end or wireless connection modules, which are not part of every hearing aid, require additional silicon area, which must be considered when comparing implementations. The area distribution for the mixed-signal hearing aid, which is presented in [9, 25], is 30% for the analog and 70% for the digital part. The digital part consists of a 24 bit application-specific instruction-set processor and five dedicated accelerators. The analog part consists of an audio front end with a programmable gain amplifier (PGA), an analogto- digital converter (ADC) and a class-D amplifier for the pulse density modulation (PDM) output. The total size is 9.50 mm^2 and this is the maximum chip size since 2004. The analog hearing aid presented in [70], which is manufactured using a 0.13 μm and a 0. 35 μm technology, requires 66% of the area for the automatic gain control, 15% for the driver and 20% for the filter circuit. The wireless control part of the analog hearing aid, which presented in [12], is based on a dual tone multi frequency (DTMF) receiver, occupies 1.16×4.6 mm^2, which is 16% of the total chip size

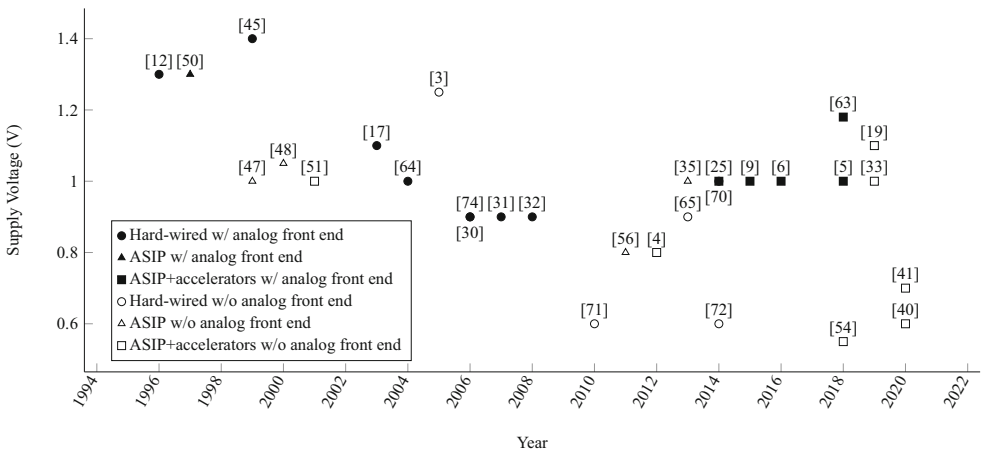

Figure 10 Supply voltages of commercial and research hearing aids.

Table 4 List of hearing aid implementations, which use dynamic voltage scaling.

Work	Operating Voltage	Default Voltage	ASIC Technology
Qiao et al. [56]	0.80 V	1.00 V	65 nm CMOS
Lin et al. [41]	0.70 V	0.90 V	40 nm CMOS
Wei et al. [71]	0.60 V	1.00 V	90 nm CMOS
Wei et al. [72]	0.60 V	1.00 V	90 nm CMOS
Lee et al. [40]	0.60 V	0.90 V	40 nm CMOS
Pu et al. [54]	0.55 V	1.05 V	28 nm CMOS

of 5.7×4.9 mm^2. The silicon area of a hearing aid may be pad limited. As a result, the total area is larger than effectively required for the digital or analog core parts. This is the case for the second largest ASIP-based hearing aid system in this study, which does not include an analog front-end [48]. Its size is 20 mm^2.

7 Operating Clock Frequency

The required operating clock frequency depends on the computing complexity of the hearing aid algorithms and the architecture-dependent processing power of the digital signa l processing system (Fig. 13). Most hard-wired hearing aids operate at comparatively low operating clock frequencies around 0.032 MHz to 8.000 MHz. The processing is sample-based, i.e., each processing unit or component like a digital filter or amplifier processes one sample per clock cycle. In [71, 72], a more computationally intensive sample-based processing is applied, using a noise reduction algorithm based on multiband spectral subtraction and an enhanced entropy voice activity detection. The audio samples are stored in local ping-pong buffer and processed sequentially for each sub-band at a clock frequency of 3MHz to 8MHz for the various processing blocks. Digital hearing aids with an application-specific instruction-set processor as the central processing unit require somewhere in the region of a thousand instructions to process the algorithms. An implementation of a related noise reduction algorithms (*mband*) on an ASIP with hardware accelerators [33] needs 2176 cycles for computation. Parallelism at data or instruction level, or application-specific instructions [4, 5, 9, 19, 25, 33, 35, 47, 51, 56] can reduce the clock frequency requirement. Accelerators are used for computing intensive tasks, where the pure software implementation on an ASIP is not feasible.

8 Audio Datapath Width

All digital hearing aids presented in this survey use fixed-point hardware architectures for signal processing, due to lower hardware cost in terms of area and power requirements compared to floating-point hardware [35]. The audio datapath width of the fixed-point data, i.e., the number of bits per audio sample, is a crucial parameter for the design and implementation of hearing aids, as it determines the maximum achievable signal-to-noise ratio (SNR). A high SNR value is a strict requirement for hearing aids [5, 31]. Each additional datapath bit increases the SNR by about 6 dB. However, this parameter also affects the area, power consumption, and processing performance of all components in the processing chain, digital processing blocks, memories, ADCs, and DACs [4, 19, 25, 56, 62]. The authors of [41] present a word length optimization to reduce the area and power of their MAC unit accelerator. They propose to optimize the number of bits based on the results of short-time objective intelligibility (STOI) measurements. Alternatively, signal-to-noise ratio (SNR) measurements are used in [33]. In [56], a 16-bit processor is extended with specific functional units that use 32-bit and 40-bit intermediate results to improve the fixed-point accuracy. Two separate processors are used in [62]. The 32-bit

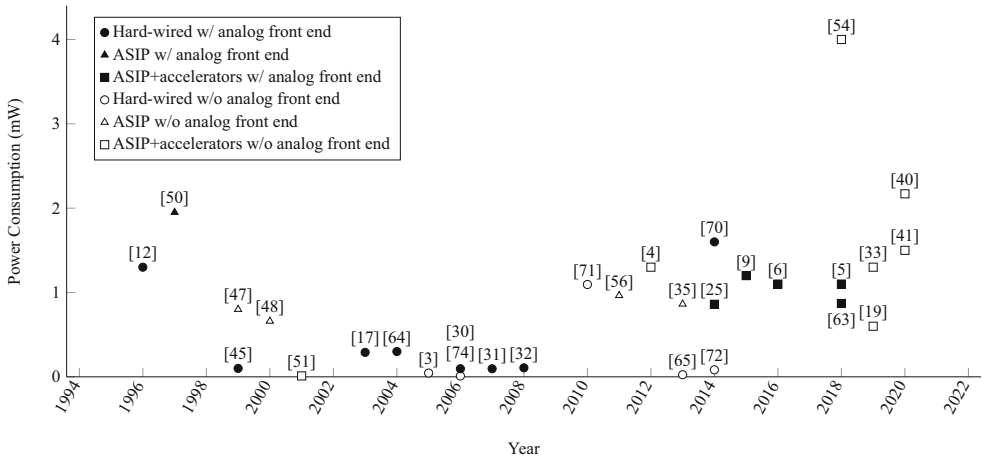

Figure 11 Power consumption of commercial and research hearing aids.

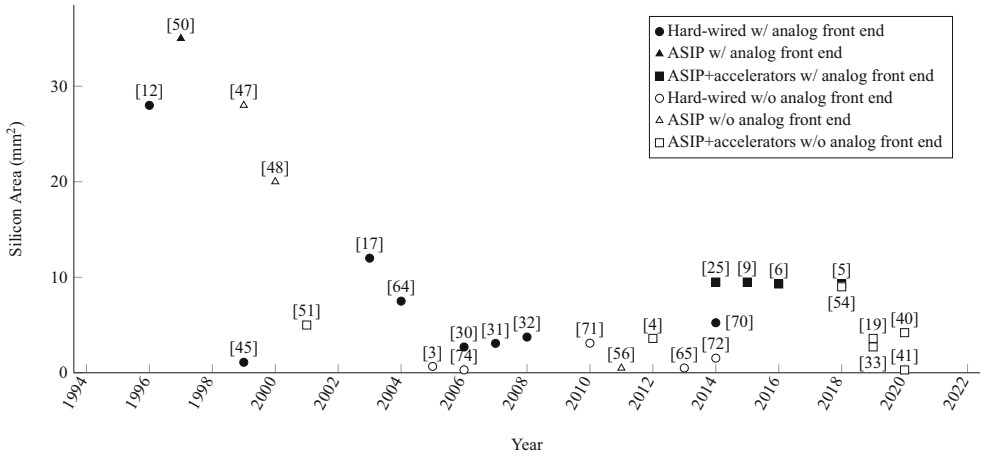

Figure 12 Silicon area of commercial and research hearing aids.

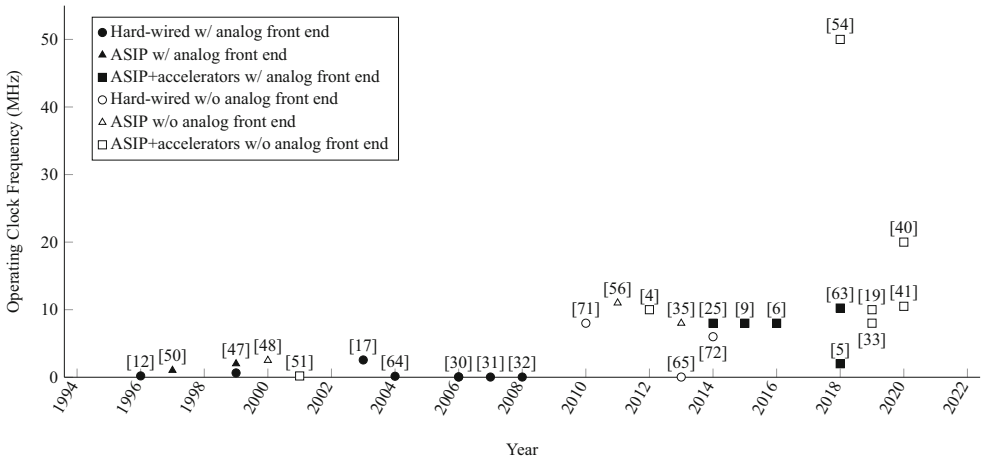

Figure 13 Operating clock frequency of commercial and research hearing aids.

Table 5 Fixed audio datapath width architectures.

Work	Analog data path	Digital data path	Sampl. Freq.	Processor Arch.
Wei et al. [71]	—	16-bit	24 kHz	hard-wired
[4, 40]	—	16-bit	—	ASIP+acc.
Lee et al. [40]	—	16-bit	16 kHz	ASIP+acc.
Kim et al. [30]	16-bit	16-bit	16 kHz	hard-wired
[47, 56]	—	16-bit	—	ASIP
Wei et al. [71, 72]	—	16-bit	24 kHz	hard-wired
Ku et al. [35]	—	16-bit	20 kHz	ASIP
Mosch et al. [48]	—	22-bit	—	ASIP
[5, 6, 9, 25, 62]	16-bit	24-bit	16 kHz	ASIP+acc.

Table 6 Variable audio datapath width architectures.

Work	Analog data path	Digital data path	Sampl. Freq.	Processor Arch.
Neuteboom et al. [49, 50]	13-bit	13 to 24-bit	16 kHz	ASIP
Paker et al. [51]	—	12 to 25-bit	16 kHz	ASIP+acc.
Lin et al. [41]	16-bit	6 to 32-bit	16 kHz	ASIP+acc.
Kim et al. [33]	16-bit	24 to 32-bit	16 kHz	ASIP+acc.
Qiao et al. [56]	—	24 to 40-bit	16 kHz	ASIP
Gerlach et al. [19]	—	8 to 64-bit	16 kHz	ASIP+acc.

Table 7 Optional floating-point audio datapath.

Work	Digital datapath	Processor Arch.
[47, 62, 63]	block floating-point	ASIP+acc.
Chang et al. [4]	static floating-point	ASIP+acc.
Gerlach et al. [18, 19]	emulated floating-point	ASIP+acc.

Arm Cortex M3 processor is used for debugging and wireless connectivity and the 24-bit ASIP processes the audio samples. In Table 5, a comparison of architectures implementing an audio datapath with fixed width is given. Most designs have a datapath width of 16-bit, for the digital and analog parts. The datapath width can be switched in some ASIP based architectures, which are listed in Table 6. This is possible by using different execution units with different datapath width, *micro*SIMD subword modes (single instruction multiple data) [39] or specialized accelerators. To take advantage of the increased dynamic range of floating-point data types, the architectures listed in Table 7 add hardware support for floating-point processing. The approaches used are block floating-point, static floating-point, or emulated floating-point.

9 Memory in Hearing Aid Systems

Due to strict power and area restrictions, on-chip memory is the only implementation option for the hearing aids listed in Table 8. On-chip area is limited and memory size is critical to the overall size of the chip. The area for the SRAM macros for the mixed-signal hearing aid presented in [9] is 1.35 mm^2. Compared to the logic size of 5.39 mm^2 and the analog size of 2.77 mm^2 the area of the SRAM is 14% of the total chip size for a 130 nm ASIC technology. The memory size depends on the complexity and type of the audio processing algorithms. Algorithms with a comparably high memory requirements are those based on trained models or data. Among those are localization algorithms [46, 60], deep learning based speech enhancement and speech recognitionalgorithms [37, 40, 44, 52]. As an example, the gaussian mixture model (GMM) of the localization algorithm requires about 90% of the total memory requirement of this algorithm [46, 60]. In this case 44,400 of 48,816 words are required only for the trained model. Another example is the hearing aid with the highest amount of on-chip memory, which is designed for computing intensive task as neural networks for speech enhancement [40]. The hearing aid with the least amount of on-chip memory is designed for IIR filters [49, 50].

10 Conclusion and Future Trends

In this survey the state-of-the-art processor architectures for hearing aids are presented. Among these architectures are analog, mixed-signal, and digital processors. The main focus is on application-specific instruction-set processors (ASIPs), which are compared to dedicated hardware architectures and hearing aid systems with hardware accelerators. Trends for the ASIC technologies, average power consumption, silicon area, and operating clock frequencies are presented. There is a clear trend towards more flexibility and growing complexity of the algorithms. Especially the deep neural network based speech enhancement and binaural processing algorithms for sound source localization are of current interest. These algorithms with higher processing

Table 8 On-chip memory sizes for hearing aid processors.

Work	Total	Details
Neuteboom et al. [49, 50]	0.85 kB	0.368 kB instruction RAM, 0.096 kB data RAM and 0.384 kB coefficient RAM
Paker et al. [51]	1.23 kB	0,62 kB data memory for mini-cores, 0,438 kB instruction memory and 0,172 kB coefficient memory
Chang et al. [4]	5.00 kB	4 processing elements (PEs) with 512 B instruction memory, 512 B shared memory for inter-PE communication and 2.5 kB local memory
Jia et al. [25]	6.00 kB	6 kB data memory
Moller et al. [47]	22.50 kB	6,125 kB RAM and 16,375 kB ROM
Mosch et al. [48]	68.00 kB	4 kB instruction ROM and 64 kB DSP parameter RAM
[2, 62, 63]	110.00 kB	6 separate logical memory banks, 24-bit data memory, 32-bit DSP instruction memory
Gerlach et al. [19]	140.00 kB	28 SRAMs, 65 kB instruction memory, 57 kB data memory and 16 kB audio interface memory
Lee et al. [40]	327.00 kB	4 processing cluster, each with 64 kB for the CNNs and 2 kB for the FFT accelerators

performance requirements have to be computed under the same strict constraints as power consumption and chip area.

Acknowledgements This work was funded by the German Research Foundation (Deutsche Forschungsgemeinschaft) under Germany's Excellence Strategy – EXC 2177/1 – Project ID 390895286.

Funding Open Access funding enabled and organized by Projekt DEAL.

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