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# Investigating multiple defects on a new fault-tolerant three-input QCA majority gate

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**Abstract**
Quantum-dot cellular automata (QCA) are a new technology used to fabricate digital circuits on the nanoscale in place of CMOS technology, which has limitations in device density. QCA devices are low in power consumption and high in speed due to their structure. Although some defects may occur during chemical fabrication, QCA gates and circuits can be designed to be fault-tolerant. The majority gate is most often used in QCA circuits; thus, many papers have investigated different structures for it and tried to design a fault-tolerant gate against only one defect. We have proposed a new structure for a three-input majority gate with a good percentage of truth output despite the multiple defects that may take place concurrently. A full adder is then designed using the proposed majority gate to demonstrate the degree of fault tolerance of QCA circuits made of fault-tolerant gates.

**Keywords** QCA majority gate · Fault-tolerant · Full adder

## 1 Introduction

According to Moore's law, the number of transistors in an integrated circuit doubles every 18 months [1]. The law has been in place since 1975, but today, there are some limitations in the technology of CMOS; therefore, efforts are being made to replace it with alternative technologies. Biocomputing and quantum

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computing are examples of studies in progress. Quantum-dot cellular automata (QCA) are one of alternative technologies that overcome the limitations of CMOS [2]. The advantages of this technology are high device packing density, low power consumption and high speed (THz). In QCA, there are two electrons in the opposite corners of hypothetical square (which called QCA cell). These electrons can be in the other opposite corners of square. Each of these two states of electrons means logical 0 and 1. We can make various logical circuits by placing a number of these cells together with various decorations. Unlike CMOS circuits, there is no electrical currents in QCA circuits and information is transferred by Columbic interactions among the cells.

We observe many papers about QCA fault-tolerant gates and circuits. It means that manufacturing may be defected in QCA. These defects may occur during the deposition or chemical phase. Therefore, many papers are about proposed QCA circuits against these defects in recent years. Three important types of QCA manufacturing defects were reported; cell misalignment, cell displacement and cell missing. We try to propose a QCA circuit with a true digital output for a certain input, despite these defects simultaneously. Also, new defects which have not yet been investigated may occur during manufacturing process should be investigated. New defects are important because they show that all possible defects in QCA circuits lead to real QCA ICs manufacturing which are exactly like simulations.

Simple QCA gates have been proposed, and common circuits have been designed using these gates. The full adder was introduced by Javid and Mohamadi [3] as being made up of majority and NOT gates. Common types of QCA defects also mentioned in [3]. A 2:1 multiplexer has been designed using majority gates [4]. A decoder is designed by new 3-input majority gate in [5]. Because 1-to-*n* bit full adders are useful, their QCA structure has been designed using proposed fault-tolerant majority gates [6, 7]. A fault-tolerant five-input majority gate also has been proposed [8, 9]. Different types of adders/subtractors have been introduced that are made up of QCA majority, XOR or NOT gates [10–15].

The design of multiplexers has been studied extensively because it is frequently used in the construction of several digital circuits [16, 17]. A QCA latch and 1-to-*n* bit counter also has been designed [18]. More complex circuits in QCA technology are also possible, such as the ALU [19], RAM [20, 21] and nanorouter [22].

In addition to the common defects in QCA circuits, new defects have been reported recently; cell rotation [23] and a single-electron fault [24].

Kink energy is a physical approach to improving the correctness of the behavior of QCA gates and circuits. The stable state of any electron in any cell can be determined by this method. All recent papers have used these calculations [25].

In this article, we try to propose a new structure for QCA majority gate that makes it resistant to the possibility of multiple defects occurring simultaneously; while similar articles have worked on making this gate resistant to only one or two defects. Two new defects that may occur during manufacturing process are investigated along with other defects in this article. These new defects have been introduced in papers, but investigation of their effects on QCA circuits has not been reported; thus, the design of fault-tolerant QCA circuits is essential for their reliable realization.

The rest of paper is as follows. Section 2 includes a brief overview of QCA technology and its faults. The proposed design of a fault-tolerant majority gate and its kink energy calculation are introduced in Sect. 3. In Sect. 4, the impact of different types of defects on the proposed majority gate is measured, and we will prove that the majority gate is fault-tolerant against all proposed defects. The conclusion is in Sect. 5.

## 2 Basics of QCA and faults

QCA is a new approach for nanoscale computing. A QCA cell consists of four quantum dots located at the corners of a square and contains two free electrons. These two free electrons can tunnel among the dots and settle either at polarization $P=-1$ or in $P=+1$ as shown in Fig. 1. A QCA cell with polarization $P=-1$ denotes the logic 0 state and with polarization $P=+1$ denotes the logic 1 state of the cell.

Logical data transfer in QCA is done by Coulombic interaction between the electrons of neighboring cells. One of the simplest QCA circuits is binary wire. The arrangement of cells is shown in Fig. 2 [6]. If we put the first cell at one of the two ends of the wire by applying an external field to be logical 0 or 1, the rest of the cells will put at the same polarization.

Another type of QCA wire (an inverted wire) is used to transfer data. In an inverted wire, all cells are rotated 45° from the normal position. As shown in Fig. 3, the polarization of each cell is reversed logic state of neighbor cell; thus, the logical state of output cell of wire can be same or inverted value of the input, depending on whether the number of cells between the input and output is odd or even [6].

Wire-crossing is very important in QCA ICs. *Coplanar* and *multilayer* are two types of crossing. Coplanar uses both two types of proposed wires in only one connecting (wire) layer of IC as shown in Fig. 4a and multilayer is using only binary

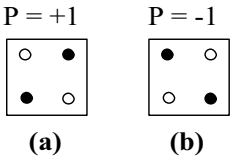



**Fig. 1** QCA cell **a** logic 1 state, **b** logic 0 state

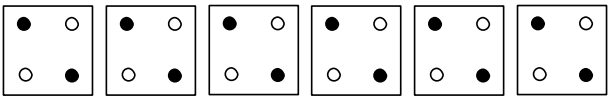


**Fig. 2** QCA binary wire

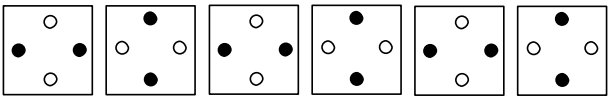


**Fig. 3** QCA inverted wire

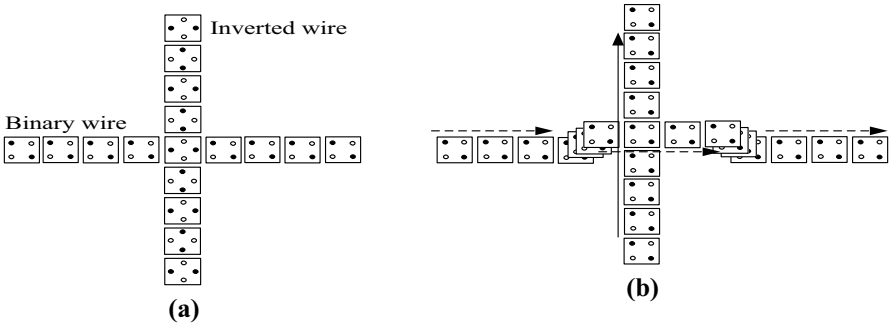



**Fig. 4** Wire-crossing in QCA **a** coplanar, **b** multilayer [6]

wire for wire-crossing, but IC designing needs more than one layer for wire connection as shown in Fig. 4b.

Unlike CMOS circuits, clocking is different in QCA circuits. There are four different clock zones as shown in Fig. 5 which are sequentially done for all cells by a certain technique named quasi-adiabatic. Each cell in QCA ICs has a wire for clock tuning; therefore, there is one layer in QCA ICs only for clock wiring in addition of other layers (Fig. 6) [26, 27]. For quasi-adiabatic switching, the four timing phases are Relax, Switch, Hold and Release [28]. Each phase is characterized by a specific color

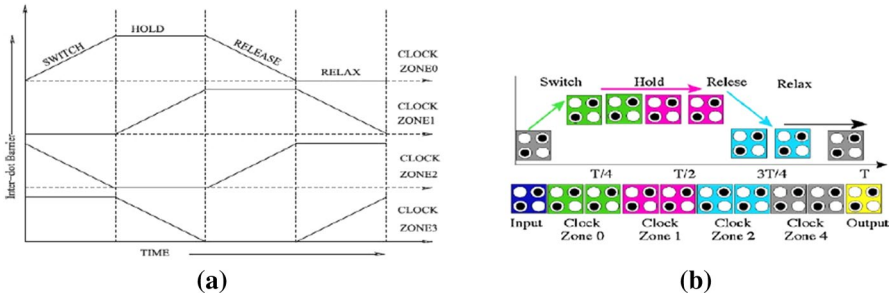



**Fig. 5** Clocking in QCA **a** four phases, **b** colors of each phase, input and output of binary wire cells

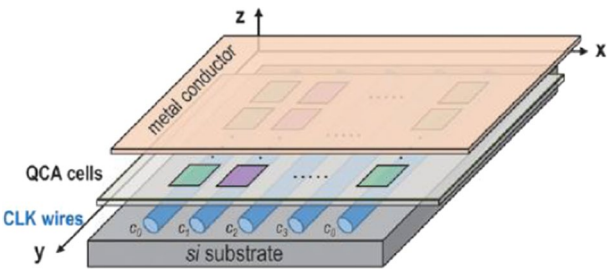



**Fig. 6** Schematic of a QCA IC layers

in articles and simulations as shown in Fig. 5. In order to create QCA circuits work properly, the cells must be positioned so that leverages the interaction between them.

We are reviewing a few important QCA devices in the rest of this section. NOT gate is shown in Fig. 7. It can be seen that there are different structures for this gate. Notice that different structures for a QCA gate can be proposed. This is the subject of discussion in various papers, so that each structure has advantages in comparison with other proposed structures.

The most usable QCA logic device is the majority gate. This gate always has an odd number of inputs with only one output. The value of the output cell becomes the majority vote of the inputs, such as for the three-input majority gate. Central cell of gate usually called device cell and affected by all input cells and sets the output cell. Figure 8a shows this gate. The truth table of a 3-input majority gate is shown in Fig. 8b. The logic function of the three-input majority gate is as follow.

$$\text{Majority}(A, B, C) = AB + AC + BC \tag{1}$$

Figure 9a shows that if one of inputs is always being at 0, we will have two input AND gate. If the same cell is always being at 1, we will have OR gate (Fig. 9b).

Using Eq. (2), the kink energy between two electron charges can be calculated. In this equation, $U$ is the kink energy, $k$ is the fixed colon, $q_1$ and $q_2$ are electric charges and $r$ is the distance between two electrical charges. By entering values for $k$ and $q$, Eq. (3) is obtained. $U_T$ is the summation of kink energies as calculated in Eq. (4). The stable state of each electron is the position where minimum kink energy is applied to all $i=0$ to $n^{\text{th}}$ neighboring electrons using Eq. (4) [8]. Using kink energy calculations, we can check the output accuracy of each QCA gate for all possible inputs.

$$U = \frac{kq_1q_2}{r} \tag{2}$$

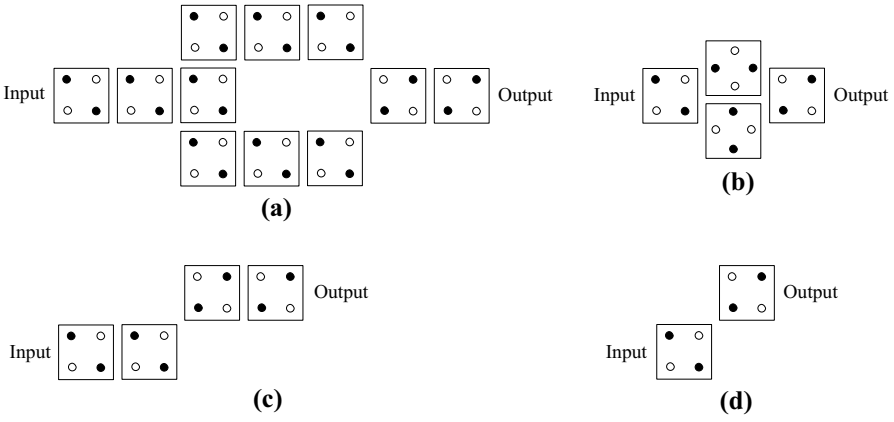
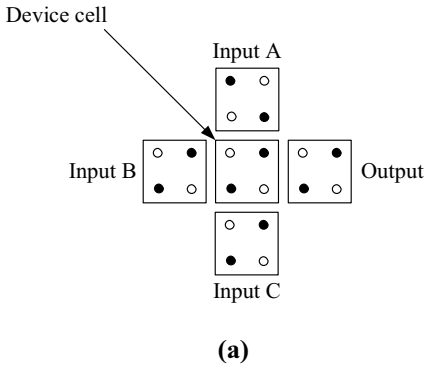



**Fig. 7** Different types of NOT gate




| A | B | C | out |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

(b)

**Fig. 8** **a** The three-input majority gate, **b** truth table of gate

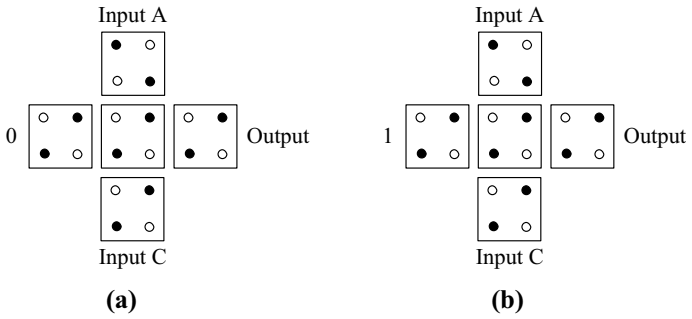



**Fig. 9** **a** AND gate, **b** OR gate

$$kq_1q_2 = 9 * 10^9 * (1.6)^2 * 10^{-38} = 23.04 * 10^{-29} = \text{constant} \tag{3}$$

$$U_T = \sum_{i=1}^{n} U_i \tag{4}$$

There are different types of QCA defects. All types of defects should be considered and simulated before manufacturing QCA ICs. The most famous defects are cell displacement, cell misalignment and cell missing [3]. Cell displacement is a defect in which the defective cell is displaced from its original direction. Figure 10b shows this type of cell displacement in a majority gate. In cell misalignment, the direction of the defective cell is misplaced. Figure 10c shows this type of defect in a majority gate. Cell missing is a defect in which a particular cell is missing, as compared to a defect-free arrangement. Figure 10d shows a cell missing defect.

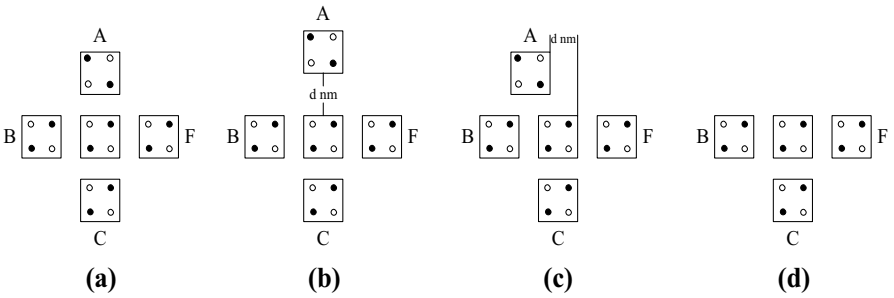



**Fig. 10** **a** Fault-free, **b** cell displacement, **c** cell misalignment, **d** cell missing

The theory of obtaining fault-tolerant rates in each QCA structure is such that simulation in the relevant software and apply the defect on the original structure to see the output. QCADesigner is the most famous simulation software for this [29].

## 3 Proposed fault-tolerant majority gate

Our proposed fault-tolerant three-input majority gate is implemented as shown in Fig. 11a. There are three inputs labeled **a**, **b**, **c** and one output cell denoted by **out**. The scheme can be justified based on physical relations. The size of the cells and the distance between them is depending on the manufacturing technology. For this scheme, we assume that the length of all cells is 18 nm. The distance between the adjacent cells is 2 nm. Rectangles in figures show a QCA cell, and inside circles mean the electrons in cell. Note that the arrangement of electrons in all cells is such that to minimum kink energy achieved.

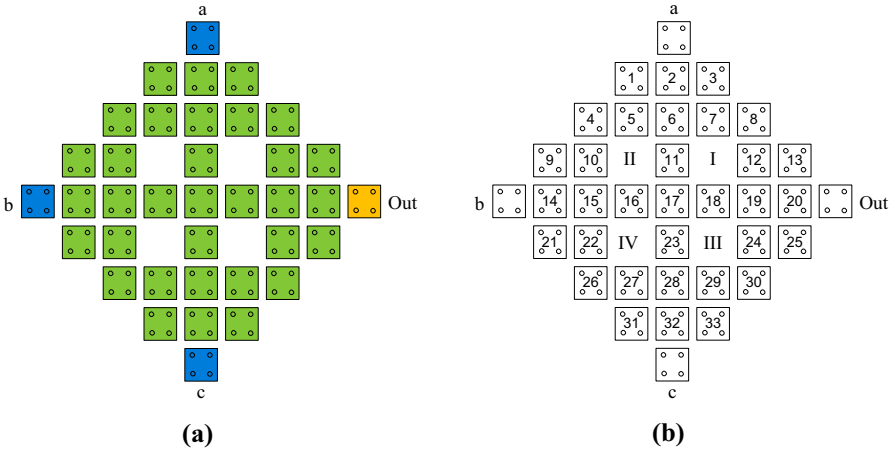



**Fig. 11** **a** Proposed majority gate, **b** cell numbering

As the proposed design has 33 different device cells, all possible inputs for all cells should be inspected to prove that the gate has true function. Kink energy calculations can do this. Note that the input and output cells are not considered in kink energy calculations.

Because it's not possible to show all possible situations by applying kink energy calculations, one specific case will be done as the following. According to cell numbering in Fig. 11b, 011 inputs are applied to gate. We expect 1 on output call. The output cell is the neighbor of cell 20, and the output cell value directly depends on cell 20. So, we investigate the situation of cell 20. In Fig. 12, we see the polarization of all cells except cell 20 when 011 inputs are applied to gate. Now, we calculate the kink energy of all cells neighboring cell 20 (cells 12, 13, 19, 24, 25) to determine the stable state (minimum kink energy).

In Fig. 13, two possible polarizations for cell 20 are shown. Using the kink energy calculations in Table 1, the minimum energy is +1 polarization (logic 1 state). This is the true position of this cell and the output cell will be in the logic 1 state, as expected. All these calculations can be done for other input values and cells to prove that the function of the gate is correct.

The proposed QCA majority gate was simulated in QCADesigner V2.0.3 simulation tool. For accuracy, the coherence vector engine was employed. This is a quantum mechanical engine using the Jacobi algorithm to calculate the values/vectors of the Hamilton matrix [29]. Figure 14 shows the simulation results.

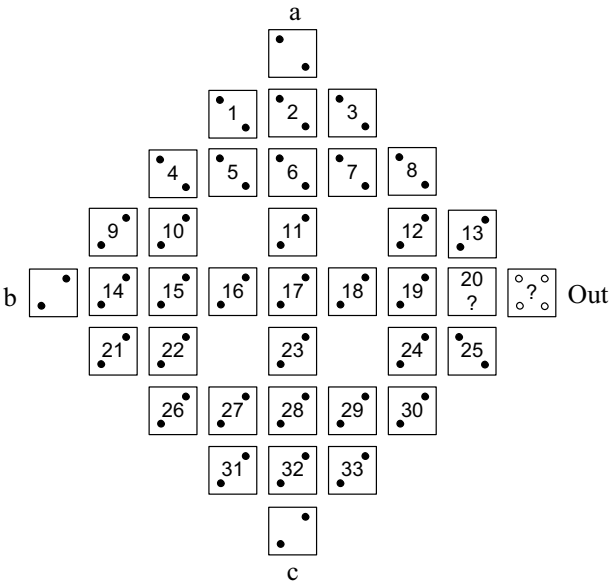



**Fig. 12** Cell polarizations when 011 inputs are applied

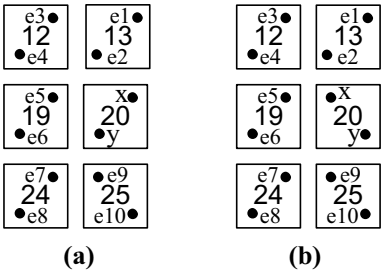



**Fig. 13** Two possible polarizations for cell 20

**Table 1** Kink energy calculations for cell 20 polarization

| Electron $y$ | Electron $x$ | Electron $y$ | Electron $x$ |
|---|---|---|---|
| Figure 13a | | Figure 13b | |
| $U1 = 0.547 \times 10^{-20}$ | $U1 = 1.152 \times 10^{-20}$ | $U1 = 0.606 \times 10^{-20}$ | $U1 = 0.856 \times 10^{-20}$ |
| $U2 = 1.152 \times 10^{-20}$ | $U2 = 1.272 \times 10^{-20}$ | $U2 = 0.856 \times 10^{-20}$ | $U2 = 11.52 \times 10^{-20}$ |
| $U3 = 0.605 \times 10^{-20}$ | $U3 = 0.814 \times 10^{-20}$ | $U3 = 0.428 \times 10^{-20}$ | $U3 = 1.146 \times 10^{-20}$ |
| $U4 = 0.814 \times 10^{-20}$ | $U4 = 0.605 \times 10^{-20}$ | $U4 = 0.536 \times 10^{-20}$ | $U4 = 1.146 \times 10^{-20}$ |
| $U5 = 1.272 \times 10^{-20}$ | $U5 = 1.152 \times 10^{-20}$ | $U5 = 0.547 \times 10^{-20}$ | $U5 = 11.52 \times 10^{-20}$ |
| $U6 = 1.152 \times 10^{-20}$ | $U6 = 0.547 \times 10^{-20}$ | $U6 = 0.606 \times 10^{-20}$ | $U6 = 0.856 \times 10^{-20}$ |
| $U7 = 1.146 \times 10^{-20}$ | $U7 = 0.814 \times 10^{-20}$ | $U7 = 1.146 \times 10^{-20}$ | $U7 = 1.146 \times 10^{-20}$ |
| $U8 = 0.814 \times 10^{-20}$ | $U8 = 0.428 \times 10^{-20}$ | $U8 = 0.536 \times 10^{-20}$ | $U8 = 0.536 \times 10^{-20}$ |
| $U9 = 11.52 \times 10^{-20}$ | $U9 = 0.856 \times 10^{-20}$ | $U9 = 1.272 \times 10^{-20}$ | $U9 = 1.152 \times 10^{-20}$ |
| $U10 = 0.856 \times 10^{-20}$ | $U10 = 0.606 \times 10^{-20}$ | $U10 = 1.152 \times 10^{-20}$ | $U10 = 0.548 \times 10^{-20}$ |
| $U_T = 28.124 \times 10^{-20}$ | | $U_T = 38.111 \times 10^{-20}$ | |

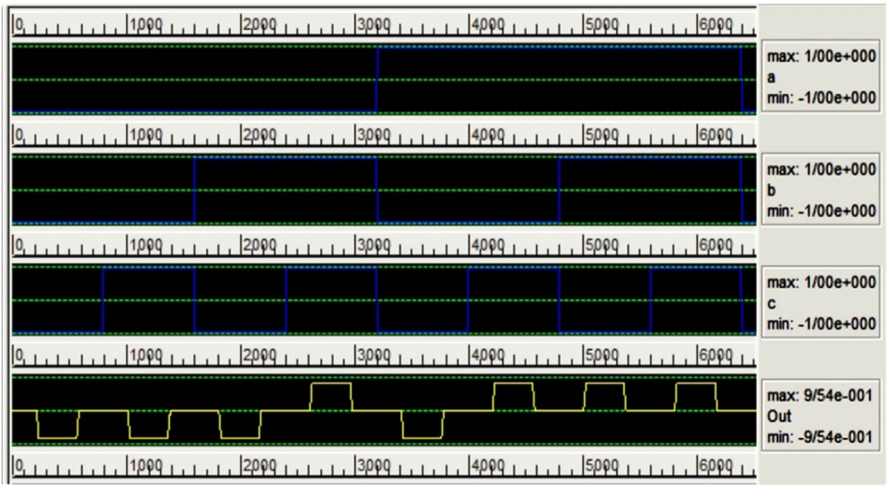



**Fig. 14** Simulation result of the proposed majority gate

**Table 2** Effect of single-cell missing on output in proposed majority gate

| # Cell | Output | # Cell | Output | # Cell | Output | # Cell | Output | # Cell | Output |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Correct | 8 | Correct | 15 | Correct | 22 | Correct | 29 | Correct |
| 2 | Incorrect | 9 | Correct | 16 | Correct | 23 | Incorrect | 30 | Correct |
| 3 | Correct | 10 | Correct | 17 | Correct | 24 | Correct | 31 | Correct |
| 4 | Correct | 11 | Incorrect | 18 | Correct | 25 | Correct | 32 | Incorrect |
| 5 | Correct | 12 | Correct | 19 | Incorrect | 26 | Correct | 33 | Correct |
| 6 | Correct | 13 | Correct | 20 | Correct | 27 | Correct | | |
| 7 | Correct | 14 | Correct | 21 | Correct | 28 | Incorrect | | |

**Table 3** Effect of extra-cell deposition on output in proposed majority gate

| Cell position | Output | Cell position | Output |
|---|---|---|---|
| I | Incorrect | III | Incorrect |
| II | Correct | IV | Correct |

## 4 Fault-tolerance parameters

Cell missing usually is the first defect to be checked. Using the cell numbering in Fig. 11b, the logic function of the proposed majority gate is true in 82% cases of single-cell missing. Table 2 shows the effect of missing of each cell for all 33 device cells.

Extra-cell deposition is a form of defect that is usually traditionally investigated. Figure 11b shows four empty cell places numbered I, II, III and IV. What happens for gate functionality if these places are filled by a cell? This type of defect is shown in Table 3 as 50% fault tolerance against the extra-cell deposition defect.

It is possible for two cells to be missed simultaneously. This type of defect called double-cell missing. Considering that the proposed majority gate has 33 device cells, there are 528 possible conditions for double-cell missing. Table 4 shows the output for different conditions of this defect. All functions that may be expected on output when this defect occurs are listed in the table. In 317 conditions, we have true output, so the fault-tolerance rate for this defect is 66%.

The cell displacement defect can be investigated in the proposed majority gate. Permissible displacement from one or more directions in the four possible directions of any cell is shown in Table 5. All cell numbers are based on Fig. 11b. The important matter in this defect is that only certain cells in distinct directions can be affected by cell displacement. Only cells that are free on one side and have a neighboring cell on the opposite side can be affected by this defect on the free side. It is evident that because the distance between two neighbors is only 2 nm, the cell will not be affected by cell displacement on the neighbor's side. For example, input cell **a** has a neighbor on the south side and can be affected by this defect in the north direction. This cell has no neighbor on the east side, so it will not be affected by cell displacement in the west direction. Input cell **a** cannot be affected by cell displacement

**Table 4** Effect of double-cell missing deposition on output in proposed majority gate

| Function | Number of defects |
|---|---|
| $a$ | 28 |
| $a'$ | 9 |
| $b$ | 13 |
| $b'$ | 7 |
| $c$ | 49 |
| $c'$ | 7 |
| Maj($a$, $b$, $c$) | 317 |
| Maj($a'$, $b$, $c$) | 8 |
| Maj($a$, $b'$, $c$) | 15 |
| Maj($a$, $b$, $c'$) | 8 |
| Maj($a'$, $b'$, $c'$) | 28 |
| Undefined | 39 |

**Table 5** Permissible cell displacements for the proposed majority gate (nm)

| # Cell | North | South | West | East | # Cell | North | South | West | East |
|---|---|---|---|---|---|---|---|---|---|
| $a$ | 12 | – | – | – | 12 | – | – | 11 | – |
| $b$ | – | – | 12 | – | 13 | 5 | – | – | 3 |
| $c$ | – | 12 | – | – | 21 | – | 14 | 10 | – |
| Out | – | – | – | 3 | 22 | – | – | – | 11 |
| 1 | 14 | – | 10 | – | 24 | – | – | 11 | – |
| 3 | 14 | – | – | 10 | 25 | – | 5 | – | 3 |
| 4 | 7 | – | 8 | – | 26 | – | 7 | 8 | – |
| 5 | – | 5 | – | – | 27 | 5 | – | – | – |
| 7 | – | 5 | – | – | 29 | 5 | – | – | – |
| 8 | 7 | – | – | 8 | 30 | – | 7 | – | 8 |
| 9 | 14 | – | 10 | – | 31 | – | 14 | 10 | – |
| 10 | – | – | – | 11 | 33 | – | 14 | – | 10 |

in the east direction for the same reason. The cell has a neighbor on the south side and cannot be affected by this defect. Cells 2, 6, 14, 15, 17, 19, 20, 28 and 32 have neighbors on all four sides, making the cell displacement defect impossible to investigable. Cells 11, 16, 18 and 23 have neighbors on two opposite sides and are free on the other two opposite directions; thus, this defect again is not investigable.

If cell displacement or another similar defect, such as cell misalignment, occurs, the output value is true and only the amplitude of the output signal drops out. In this case, we should determine a threshold for amplitude. Consider some amount of a defect as the fault; if the defect occurs, the output amplitude drops out below the determined threshold. For example, the out cell in Fig. 11b is displaced to the east direction 5 nm. The simulation result is shown in Fig. 15. The output value is true, but the output amplitude is drops out when compared with the amplitude of the

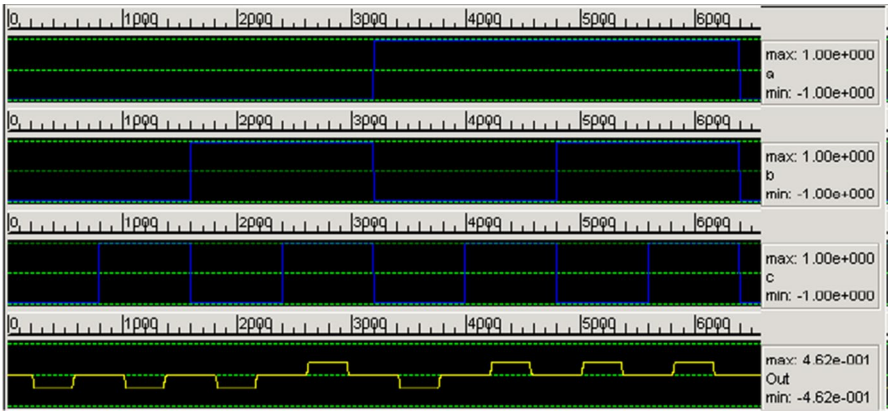



**Fig. 15** Simulation result of the proposed majority gate in 5-nm displacement on output cell

input signal. Is this a fault? Consider a downsizing of the output amplitude to less than half the input amplitude as the fault. Because of this, we set a 3-nm displacement for the output cell in Table 5.

Cell misalignment defect can be investigated for cells which have a neighboring cell in one direction and also have a free side in the opposite direction. When cell misalignment occurs, the cell might be located in the wrong place in the predicted direction. For example, according to Fig. 11b, cell **a** has a southern neighbor in the north–south direction and is free in the west–east direction. Cell misalignment may occur in this free direction. Cell deposition in any place except for these definitions is not a standard fault and designing a fault-tolerant QCA structure against such a fault is not possible. The reason for this is clear; placing a cell in a direction for which the cell has a neighbor at a distance of 2 nm causes two cells to overlap. There is no method of designing a QCA circuit that is resistant to this non-standard fault. The only way to confront overlapping is to consider more distance between neighboring cells. Permissible cell misalignment for our proposed majority gate is shown in Table 6. Only the cells conforming to the cell misalignment definition on defined sides are included.

The point about cell displacement and misalignment is that sometimes a cell displacement defect in one of the neighboring cells may be cell misalignment in another neighboring cell. For example, in Fig. 11b, cell displacement on cell 1 to the north through cell 5, is cell misalignment through cell number 2. Also, cell displacement

**Table 6** Permissible cell misalignments for our proposed majority gate (nm)

| # Cell | North | South | West | East | # Cell | North | South | West | East |
|---|---|---|---|---|---|---|---|---|---|
| *a* | – | – | 6 | 6 | 11 | – | – | 2 | 2 |
| *b* | 6 | 6 | – | – | 16 | 3 | 3 | – | – |
| *c* | – | – | 6 | 6 | 18 | 3 | 3 | – | – |
| Out | 3 | 3 | – | – | 23 | – | – | 2 | 2 |

on cell 1 to the west through cell number 2 is cell misalignment through cells 4 and 5. In many cases, a cell displacement defect is similar to a cell misalignment defect. This is mentioned once in Table 5 and is not repeated in Table 6. Cells 11, 16, 18 and 23 should not be affected by cell displacement, only by cell misalignment. Cells **a**, **b**, **c** and **out** can be affected cell displacement as well as cell misalignment.

One new defect in QCA circuits that has been studied in many papers is cell rotation. As mentioned by Yang [23], a cell might rotate in place during manufacturing. This is a type of cell displacement defect. First, the electromagnetic force between two neighboring cells $M$ and $N$ as shown in Fig. 16 is investigated as follow:

$$E^{M,N} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{i=1}^{4}\sum_{j=1}^{4}\frac{q_i^M q_j^N}{d_{ij}} \tag{5}$$

where $\varepsilon_r$ is the relative dielectric constant, $q^M$ and $q^N$ are the charge in dot $i$ of $M$ and $N$ cells, and $d_{ij}$ denotes the distance between the $i$th dot in the cell $M$ and the $j$th dot in the cell $N$.

Now assume that there is no rotation of either cell. As a result, the electrons of the $M$ cell are located in places 1 and 3 and the electrons of the $N$ cell are located in places $1'$ and $3'$. The distance between 1 and $1'$ is $L+S$. If cell $N$ rotates to angle $\theta$, the distance will be equal to:

$$d_{11'} = \sqrt{\left(\frac{L}{2}\sin\theta + \frac{L}{2}\cos\theta - \frac{L}{2}\right)^2 + \left(\frac{L}{2} + s - \frac{L}{2}\sin\theta + \frac{L}{2}\cos\theta\right)^2} \tag{6}$$

Other distances can be calculated in the same way. The amount of electromagnetic energy between two cells having different angles and for two positions of the same and opposite neighboring cells, as shown in Fig. 17, is calculated according to the Eq. (7). This relationship is actually kink energy.

$$E^{M,N}_{\text{kink}} = E^{M,N}_{\text{opposite polarization}} - E^{M,N}_{\text{same polarization}} \tag{7}$$

The energy between two cells can be calculated for all angles and the polarity of each cell can be determined at each angle. It will then be clear at which angles the circuit operates correctly. Accordingly, the diagram of the correct functioning of the

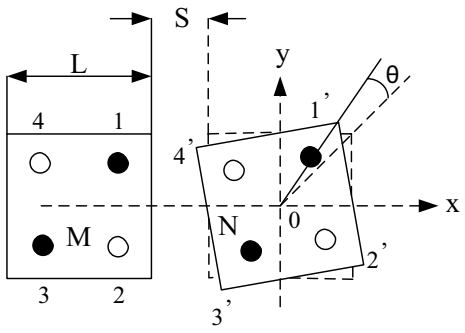



**Fig. 16** Description of cell rotation

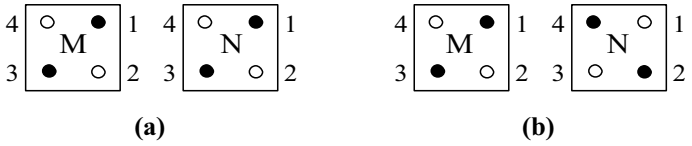



**Fig. 17** Kink energy between two cells **a** same polarization, **b** opposite polarization

circuit can be drawn for different rotation angles. Resistance to cell rotation in the proposed majority gate was investigated for the simultaneous rotation of all cells, and the results are presented in Fig. 18. It can be seen that changing the cell dimensions did not make much difference.

This is discussed by Yang [23] and is shown in our proposed gate that most of these graphs are U-shaped. The only difference in the cell-rotation defect resistance chart for different circuits and gates is that the floor level of the graph which obviously, it usually happens around the 45-degree rotation angle. This floor level is the lowest output correctness rate and varies depending on the number of cells and the complexity of the circuit. This error is not common for rotation of single cells in circuits with many gates. The results are related to simultaneous rotation of all cells. A larger value of success rate indicates a more rotation defect-resistant structure. According Fig. 18, floor level of our proposed majority gate is 33%.

A new type of defect has been investigated by Mukherjee [24], which may occur during manufacturing when one of the electrons of a cell disappears. This causes tunneling of the remaining electron to the wells of the neighboring cell. This can cause the accumulation of two, three, four or more electrons in a cell and is called the single-effect upset. This defect was investigated in the proposed majority gate.

The single-effect upset may occur for each cell, but here, only the fault in cell 20 has been investigated (using the cell numbering shown in Fig. 11b), because it is the most sensitive cell. If one of the electrons of cell 20 disappears, one of the four remaining wells in the cell should accept the one electron remaining for each of the eight input modes. To do this, each time one input mode is applied to the

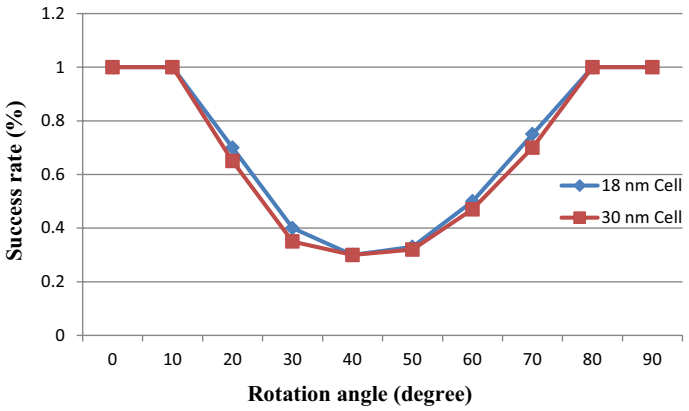



**Fig. 18** Simulation results of the proposed majority gate with cell-rotation defect

gate, the location of the electrons of the cells neighboring cell 20 are considered. The kink energy is then calculated to determine the minimum kink energy from the neighboring cells in which exist one of the four wells. This will be the location of the single electron.

Assume that input 011 is applied to the gate. The positions of the electrons in the cells neighboring cell 20 are shown in Fig. 19. A single electron will be located in one of the four wells *p*, *q*, *r* or *s*. The kink energy of the electrons from neighboring cells 1 to 10 is calculated for single-electron 20 in each of the four possible states shown in Table 7. The minimum kink energy occurs in well *s*; therefore, for the input of 011, single-electron 20 in well *s* is taken.

The same calculations are performed for other input modes and the stable position of the single electron in cell 20 is summarized in Table 8. Using Table 9, the logical value of the output cell obtained for each input, despite the stable condition of single-electron 20, can be obtained and compared with the expected value.

To compare the robustness of different structures of a QCA gate against single-electron defect, usually this defect is checked only for neighboring cell of the output cell which has the most effect on the output. The resistance rate of our proposed majority gate against the single-electron defect in cell 20 is 62.5%.

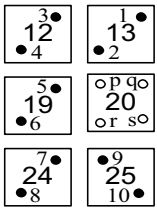



**Fig. 19** Investigating single-electron defect on cell 20 in proposed majority gate

**Table 7** The kink energy coming to each well from neighboring electrons (values $\times 10^{-20}$ J)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | Total energy |
|---|---|---|---|---|---|---|---|---|---|---|---|
| *p* | 0.856 | 11.52 | 1.146 | 1.146 | 11.52 | 0.856 | 1.146 | 0.536 | 1.152 | 0.548 | 30.426 |
| *q* | 1.152 | 1.272 | 0.814 | 0.605 | 1.152 | 0.547 | 0.814 | 0.428 | 0.856 | 0.606 | 8.246 |
| *r* | 0.547 | 1.152 | 0.605 | 0.814 | 1.272 | 1.152 | 1.146 | 0.814 | 11.52 | 0.856 | 19.878 |
| *s* | 0.606 | 0.856 | 0.428 | 0.536 | 0.547 | 0.606 | 1.146 | 0.536 | 1.272 | 1.152 | 7.685 |

**Table 8** Stable position of single electron in cell 20 per all input modes (values $\times 10^{-20}$ J)

| 111 | 110 | 101 | 100 | 011 | 010 | 001 | 000 | Test case |
|---|---|---|---|---|---|---|---|---|
| 28.262 | 28.262 | 30.121 | 28.262 | 30.426 | 9.897 | 30.121 | 9.897 | $U_p$ |
| 5.431 | 5.431 | 13.967 | 5.431 | 8.246 | 18.031 | 13.967 | 18.031 | $U_q$ |
| 17.543 | 17.543 | 8.011 | 17.543 | 19.878 | 19.975 | 8.011 | 19.975 | $U_r$ |
| 7.320 | 7.320 | 8.671 | 7.320 | 7.685 | 18.269 | 8.671 | 18.269 | $U_s$ |
| *q* | *q* | *r* | *q* | *s* | *p* | *r* | *p* | Stable position |

**Table 9** Logic values of proposed majority gate under single-electron defect

| Input | Stable position | Output | Result |
|---|---|---|---|
| 000 | *p* | 0 | Correct |
| 001 | *r* | 1 | Incorrect |
| 010 | *P* | 0 | Correct |
| 011 | *s* | 0 | Incorrect |
| 100 | *q* | 1 | Incorrect |
| 101 | *r* | 1 | Correct |
| 110 | *q* | 1 | Correct |
| 111 | *q* | 1 | Correct |
| Success rate | | | 62.5% |

Applying the proposed majority gate to a QCA circuit and examining fault propagation in it is another requirement for analysis of faults in the proposed structure. In this way, the input and output relationships of a full adder can be defined as follows and implemented using the proposed majority gate as shown in Fig. 20.

$$\text{Sum} = M(\overline{C_{\text{out}}},\ C_{\text{in}},\ M(X,\ Y, \overline{C_{\text{in}}})) \tag{8}$$

$$C_{\text{out}} = M\left(X,\ Y,\ C_{\text{in}}\right) \tag{9}$$

When investigating the fault for the proposed full adder, only the majority gates were considered because the connections between them are not fault-tolerant and the purpose of this review was to determine resistance to defects during the use of three majority gates (fault propagation). In simulations carried out on the full adder, the resistance to the single-cell missing defect was 65%, the resistance to the double-cell missing was 60% and the resistance to the extra-cell defect was 50%. By comparing these values with the values for the proposed majority gate reported individually, it can be seen that its use in the construction of other circuits had little effect on its resistance to a variety of faults. Indeed, fault propagation is insignificant when proposed gate is used to form a circuit that is full adder here.

Notice that the full adder in Fig. 20 may have some design problems. Such as the input cells ($x$ and $y$) are surrounded by other cells; thus, there is no single layer accessibility to the inputs. The focus of this paper is only on proposing a fault-tolerant majority gate (as mentioned in the title of the article), and this proposed full adder is used only for showing fault propagation of our proposed majority gate. For this reason, in the rest of paper, there is not any comparison of this full adder to similar works, and all comparisons are about majority gate.

To further investigate fault propagation when using the proposed majority gate to construct the various functions shown in Table 10, eleven functions were implemented and tested for resistance to the three faults. This indicates the low fault shift when multiple gates are used at the same time.

Tables 11 and 12 compare the proposed majority gate with similar gates, in particular for resistance to various types of defects. All comparisons are based on the

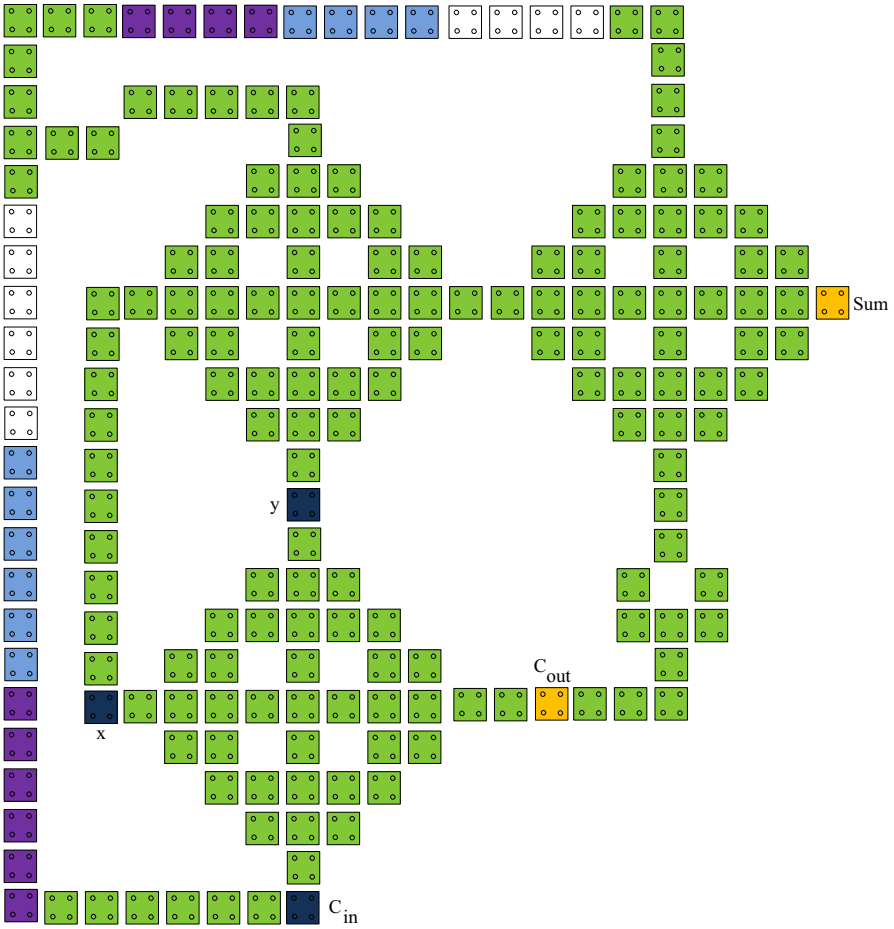



**Fig. 20** Full adder using proposed majority gate

18 * 18 nm cell size and a distance between neighboring cells of 2 nm. If another dimension had been used in a paper, it was used for comparative simulation at the same dimensions. The bold values summarized in Table 12 indicate that the item has not been reported in the original paper, but was obtained during simulation and re-measurement.

Because all the previous similar 3-input majority gates listed in Table 11 are fault-tolerant against only one or two defects, they may use fewer cells and occupy less space than our proposed gate. Whereas, our proposed gate is fault-tolerant against multiple defects concurrently, so it is necessary to use more cells and occupy more space. Therefore, a column is added in Table 11 that shows 'area' to 'number of cells' ratio. Using this ratio, we can compare our proposed gate with other similar works in terms of the cost-effectiveness of manufacturing. According to this, we see that the ratio is lower for our proposed gate than

**Table 10** Investigating three defects in making 11 functions using proposed majority gate

| | Number of used majority gates | Number of used gates | Single-cell missing (%) | Double-cell missing (%) | Extra-cell deposition (%) |
|---|---|---|---|---|---|
| $ab'c$ | 2 | 3 | 68 | 55 | 50 |
| $a'bc+a'b'c'$ | 5 | 9 | 58 | 45 | 45 |
| $a'bc+ab'c'$ | 5 | 8 | 58 | 45 | 45 |
| $a'b+bc'$ | 3 | 5 | 65 | 50 | 50 |
| $ab'+a'bc$ | 4 | 6 | 63 | 48 | 50 |
| $a'bc+abc'+a'b'c'$ | 8 | 13 | 53 | 40 | 45 |
| $ab+bc+ca$ | 5 | 5 | 60 | 46 | 45 |
| $a'b+b'c$ | 3 | 5 | 65 | 50 | 50 |
| $a'b+bc+ab'c'$ | 6 | 9 | 55 | 40 | 45 |
| $ab+a'b'$ | 3 | 5 | 65 | 50 | 50 |
| $abc'+a'b'c'+ab'c+a'bc$ | 11 | 17 | 50 | 35 | 40 |

**Table 11** Comparison of proposed majority gate with similar gates

| Majority gate | Number of cells | Area ($\mu m^2$) | Area/number of cells | Clock zone |
|---|---|---|---|---|
| [5] | 36 | 28 | 0.77 | 1 |
| [6] | 16 | 12 | 0.75 | 2 |
| [7] | 25 | 96 | 3.84 | 1 |
| [19] | 10 | 8 | 0.8 | 2 |
| [21] | 13 | 12.1 | 0.93 | 2 |
| Proposed gate | 37 | 26.2 | 0.7 | 1 |

**Table 12** Comparison of proposed majority gate with similar gates at all defects

| Majority gate | Single-cell missing (%) | Double-cell missing (%) | Extra-cell deposition (%) | Cell displacement (nm) | Cell misalignment (nm) | Cell rotation (%) | Single electron (%) |
|---|---|---|---|---|---|---|---|
| [5] | 93.8 | 65 | **20** | **1–2** | **1–3** | **10** | **50** |
| [6] | **70** | **30** | Undefined | **1–2** | **1–3** | **10** | **50** |
| [7] | 70 | **30** | Undefined | **1–2** | **2–3** | **10** | **50** |
| [19] | 80 | 40 | Undefined | **2–9** | **3–7** | Undefined | **50** |
| [21] | 88 | **40** | **30** | **3–11** | **2–5** | **20** | **50** |
| Proposed gate | 82 | 66 | 50 | 3–14 | 2–6 | 33 | 62.5 |

similar works. It shows that spending more cost for manufacturing our proposed gate is valuable to be multiple fault-tolerant concurrently.

The number of clock zones is so important in QCA gates and circuits. We see in Table 11 that although the number of cells and the area of the proposed majority gate are slightly greater than in similar works, the proposed gate has only one clock zone even though our gate is multiple fault-tolerant.

In Table 12, we see comparison of our proposed majority gate with similar gates at all previous discussed defects. Our proposed majority gate has a higher resistance rate than similar works or it's close to them at single-cell missing. Our proposed majority gate has a higher resistance rate than similar works at double-cell missing and extra-cell deposition.

Due to Tables 5 and 6, we have obtained an average rate of displacement and misalignment of all cells mentioned in these tables. These average rates are expressed in Table 12. This average rate is done for similar works too and shown in Table 12. We see the amount of movement of a cell of our proposed majority gate is greater than other works at cell displacement and cell misalignment. For example, on average, one cell in our proposed majority gate can displaced $(14-3=9)$ 9 nm. While it's only $(2-1=1)$ 1 nm for [5] or $(11-3=8)$ 8 nm for [21]. So, if cell displacement occurs during manufacturing, our gate is more resistant to similar works. It means a cell can have placed on average 9 nm from its original direction. But it's 1 nm for [5] or 8 nm for [21]. The higher average rate of displacement, the more resistance cell displacement for a gate.

All of the above about cell displacement are true for cell misalignment. Average rate of misalignment are extracted from Table 6 and expressed in Table 12. We see if cell misalignment occurs during manufacturing, our gate is more resistant to similar works. For example, on average, one cell in our proposed majority gate can misaligned $(6-2=4)$ 4 nm. It means direction of a cell can have misplaced on average 4 nm from its original direction. While it's only $(3-1=2)$ 2 nm for [5] or $(5-2=3)$ 3 nm for [21].

The values in the cell-rotation defect column in Table 12 are the minimum accuracy percentage obtained for the range of rotation of all cells from zero to ninety degrees. We see our proposed majority gate has the most value (33% calculated in Fig. 18).

As described in the paragraph Table 9, the values in the single-electron defect column in Table 12 are obtained for our proposed majority gate and similar works. We see our gate has the highest rate of resistance against this defect.

In general, Table 12 shows that our proposed gate has better values compared to similar works on all kinds of defects simultaneously. Similar works are strong against only one or two defects. It means that our proposed majority gate is multiple fault-tolerant. It's the first novelty of our design. Cell-rotation and single-electron defects are two new defects which were introduced in [23, 24]. In no article, the majority gate was introduced which is resistant to these defects. It is the second novelty of our design.

## 5 Conclusion

Our proposed gate is fault-tolerant enough for multiple defects. This gate is strong against new defects such as cell-rotation and single-electron defect in addition of usual defects (cell displacement, cell missing, cell misalignment and additional/extra-cell deposition) while other previous gates are strong against only few defects. This gate is also optimal in area, complexity, number of cells and delay. Multiple defect fault-tolerant is very important in QCA technology circuits, because this matter will give confidence to the QCA circuit constructor that the circuit has a perfectly correct output. Designing these multiple fault-tolerant QCA circuits needs using strong gates against faults such as our proposed gate at first.

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