Optimal demultiplexer unit design and energy estimation using quantum dot cellular automata

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Abstract

Quantum dot cellular automata (QCA)-based demultiplexer or DeMUX is a basic module of nanocommunication and nanocomputation, like a multiplexer. However, the design and analysis of demultiplexer using QCA have been neglected by researchers, unlike multiplexer. This article proposed and analyzed a simple and optimized QCA-based single-layered demultiplexer only using two majority gates, one inverter and two clocks. Our proposed area-efficient DeMUX has a complexity of 21 QCA cells, which covered a total area of 20,412 nm^2 and a cell area of 6804 nm^2 with area usage of 33.33%. The latency of the proposed block is 0.5 clock, and the calculated cost is 20. The energy dissipation analysis using QDE tool shows that the total energy dissipation is 8.64e−003 eV and the average energy dissipation per cycle is 7.85e−004 eV of QCA demultiplexer. Also, energy has been calculated using the popular tool QCAPro in three tunneling levels with $\gamma = 0.5E_K, \gamma = 1.0E_K$ and $\gamma = 1.5E_K$ at 2K temperature, and the total energy dissipated as 32.86 meV, 41.41 meV and 52.21 meV, respectively.

1 Introduction

Scaling down or shrinking down of complementary metal oxide semiconductor (CMOS) technology is reaching toward saturation, which enables the development of quantum dot cellular automata. Quantum dot cellular automata or QCA term was introduced by Lent et al. [1]. It took only a few years to be a popular technology and an interesting research topic due to its faster switching speed, lower density

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and lower power consumption compared to popular CMOS technology [2]. QCA is the most acceptable nanotechnology to design nanocircuits for nanoelectronics and nanocomputing as a substitute to CMOS-based circuits. QCA technology is a transistor-less technology unlike the CMOS, and it works on the theory of tunneling mechanism and Coulombic interactions [3]. Being a new technology, QCA is very emerging and there are several research works to be done in this area. The recent trend of QCA-based designs is to minimize the complexity and cost of circuits. In this paper, we proposed a simple QCA demultiplexer layout and calculated the energy dissipation, cost, etc.

1.1 Brief literature review of QCA

The literature of QCA is crowded with the variety of works and the elementary implementations. It is a long list that already has been reported. Few of the works of the list are the design of fundamental QCA blocks, the study of basic logic gates, the implementation of combinational and sequential circuits, the design of highly complex memory, different nanocommunication blocks implementation and other different types of works. Few of the works are included as follows:

The most important QCA building block is the majority gate, and it has been explored by many researchers like Goswami et al. [4] and Ahmadpour et al. [2]. They also discussed about the fault-tolerant majority gates [2, 4]. The other two fundamental blocks are QCA wire and inverter. Khan et al. [5, 6] searched the behaviors of them and calculated the kink energy of those blocks. Bahar et al. [7] investigated few digital logic circuits like XOR gate, adders, etc., using the concept of modified majority gate. The area-efficient QCA reversible logic circuits have been employed by Singh et al. [8]. Several works have been studied on QCA combinational circuits, and adder is one of them. Adder has been studied by many researchers, like Perri et al. [9] who designed novel adders, Balali et al. [10] who implemented adders using XOR gate, Mokhtari et al. [11] who tested QCA full adders, Roshany et al. [12] who presented multilayer ripple carry adders, and Cho et al. [13] who realized both adders and multipliers. Multiplexers and demultiplexers are very important combinational items; however, QCA demultiplexers are seldom designed, unlike multiplexers. Few works on multiplexers have been carried out by AlKaldy et al., Khan et al., Singh et al., etc., and several other works are also done on QCA multiplexers [14–16]. However, there are very limited numbers of works on demultiplexer that exists in the QCA literature and few of the works mentioned in Refs. [17–23] have been discussed in Sect. 3 of this article. There are plenty of research works that exist on sequential circuit analysis in the QCA literature. For example, Huang et al. [24] reported D flip-flop, RS flip-flop etc., Abdullah-Al-Shafi et al. [25] devised counter circuits and calculated its energy, and Sabbaghi-Nadooshan et al. [26] presented shift registers using QCA multiplexers, etc. Different complex sequential circuits have already been reported in the literature, like serial and parallel memory that have been designed by Vankamamidi et al. [27, 28], programmable logic array (PLA) that is employed by Hu et al. [29], arithmetic logic unit (ALU) and microprocessor that have been implemented by Niemier et al. [30], etc. Recently, QCA

technology has been extended at its highest level and involved in the research area of nanocommunication also. Circuit switching [20] and nanorouter [23] for nanocommunication have already been reported earlier. Recently, De et al. [31] presented a very interesting and remarkable discussion on nanocommunication channel fidelity for code converter. Another successful design of a butterfly switching network for nanocommunication has been implemented recently by Bahar et al. [32]. Therefore, QCA literature is flooded by plenty of such works, whereas this article only focused on demultiplexer.

1.2 Motivation

The main purpose of this paper is to present a QCA demultiplexer or DeMUX unit and do the analysis of different parameters. The design stage has been carried out using the tool QCADesigner 2.0.3 [33]. The analysis part includes the complexity, area requirement, area usage, cost, etc. Also, the energy dissipation of the proposed structure has been checked successfully using the tool QDE [34] and QCAPro [35]. Finally, comparisons have been made with the existing designs. The strength of this work is summarized as follows:

- Very simple layout.
- Signal flow direction considered.
- Detail energy calculation using QD-E and QCAPro both.
- Analysis considering all important parameters.
- Compared with few best similar type of existing designs.

1.3 Organization

After the introduction, the rest of the article is organized as follows: Sect. 2 provides an overview of QCA terminologies including the cells, basic gates and clocking. The existing work of QCA demultiplexer is provided in Sect. 3. The proposed work including the layout and simulation result is addressed in Sect. 4. The energy calculation part of the proposed structure is provided in Sect. 5. The analysis part is covered in Sect. 6. In Sect. 7, a rigorous comparison has been made. Finally, the paper will come to the conclusions in Sect. 8.

2 QCA basic terminologies

A square shape 'cell' is the smallest unit of QCA, which is formed by four quantum dots, located at four corners of the square [1]. A cell may stay at a null state or two polarized states as shown in Fig. 1. Two extra electrons located inside a cell can move among the four dots due to the tunneling effect. However, these electrons always occupy the diagonal positions of the square due to Coulombic repulsion force, hence generating two forms of arrangements [36, 37]. One of the arrangements produces polarization '1' or logic '1,' and another arrangement produces the polarization '0' or logic '0' [38].

Fig. 1 QCA cells
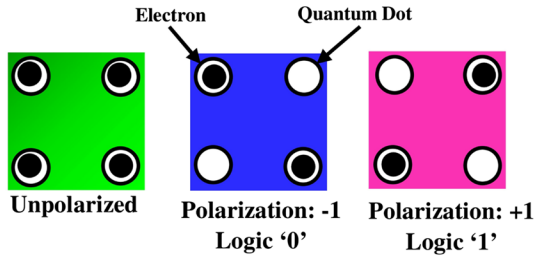
Before discussing basic QCA building blocks in Figs. 2, 3 and 4, let us first discuss QCA clock as shown in Fig. 5. To change the state of polarization, clocks are obligatory. QCA clocks empower the movement of the electrons inside a cell by dropping the tunneling barriers and permit these electrons to change the positions. The clocks in QCA are responsible to transfer the data perfectly in a circuit. There are four clocks in QCA and work in a particular sequence as clock0 → clock1 → clock2 → clock3 → clock0, as shown in Fig. 5. Again, each clock has four stages and they are switch, hold, release and relax. The switch phase infers a rising edge, the hold phase implies a high level, the
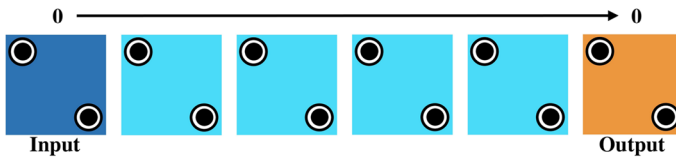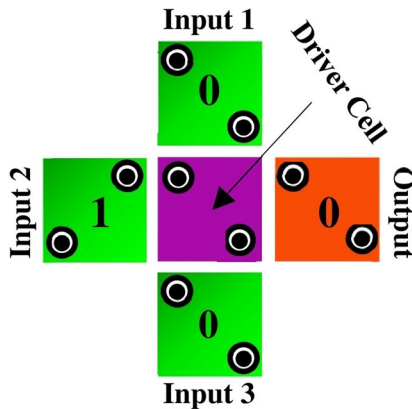

Fig. 2 QCA wire

$$M(A, B, C) = AB + BC + CA$$
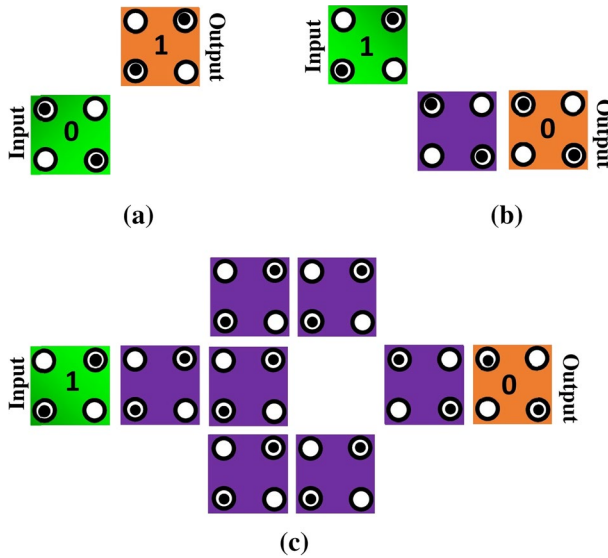
Fig. 3 QCA majority gate

Fig. 4 Few QCA inverters

release phase infers a falling edge, and the relax phase implies a low level [37]. However, there are limitations in the conventional adiabatic clocking scheme [39]. The main three fundamental blocks of QCA are 'wire,' 'majority gate' and 'inverter' as shown in Figs. 2, 3 and 4, respectively. When there are a series of cells located one after another, then it is called 'wire'; the input cell polarization transfers to the output cell maintaining the same logic state during the entire path of a 'wire' as shown in Fig. 2. The 'majority gate,' shown in Fig. 3, can be expressed as Eq. (1), which acts as a two-input AND gate as well as a two-input OR gate by simply keeping one of the inputs of MAJ(A, B, C) constant at '0' or '1,' respectively [36–38].

$$MAJ(A, B, C) = AB + BC + CA \tag{1}$$

The 'inverter' just inverts the input like the digital NOT gate, as shown in Fig. 4 [36]. These basic gates are used to make larger logic circuits and blocks in QCA circuit designs.

3 Existing work on QCA demultiplexer and gaps

QCA demultiplexer is a very important block in nanocommunication and nanocomputation area. But there are very few QCA demultiplexers in the existing literature, unlike multiplexers. Few popular and notable existing works are discussed below:

Iqbal et al. [17] proposed $2^n - 1 - 2^n$ MUX–DeMUX circuits in 2013, using QCA where 27 QCA cells have been used for 1:2 demultiplexer with cell area 8748 nm^2, total area 23,328 nm^2 and latency of 2 clocks as mentioned in the paper. They designed 1:2 demultiplexer using two clocks, two majority gates and two inverters.
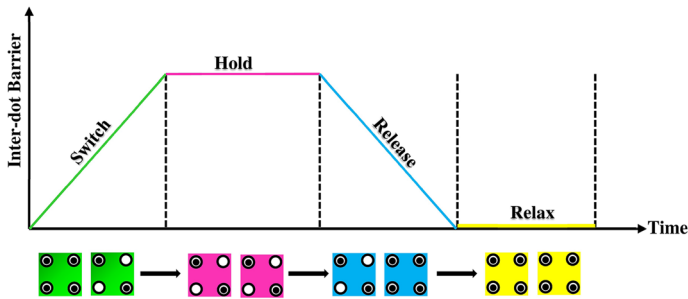
Fig. 5 QCA clocking

They demanded that the design is advantageous due to small area requirements, less delay and less power consumption [17].

In 2017, Ahmad [18] proposed QCA-based $2^n : 1/1 : 2^n$ multiplexer/demultiplexer and calculated the power consumption using QCAPro tool. Here, the projected 1:2 demultiplexer has a covered area of 6804 nm^2, total area 23,328 nm^2 with a complexity of 21 cells and latency of 0.5 clock as mentioned in the paper. Using two clocks, five inverters and without using any majority gate, they have designed 1:2 demultiplexer. The author mentioned that this design is superior in terms of area and complexity [18].

Safoev et al. [19] designed 1:2 multilayer demultiplexer in 2016, using 21 cells with covered area 6804 nm^2 and total area 17,496 nm^2. They used two clocks, one inverter and two majority gates. However, there is a latency of one clock at the circuit output. The authors predicted that the proposed block may lead to construct more efficient complex circuits [19].

Das et al. [20] mentioned one 1:2 demultiplexer in 2017, during the design of a circuit switching network using QCA. They used 32 cells, three clocks, one inverter and three majority gates to design this DeMUX, and it is used as an internal block of a communication network. It has a latency of 0.5 clock with covered area 10,368 nm^2 and total area 26,244 nm^2 [20].

Shah et al. [21] in 2011 designed 1:2 demultiplexer using 56 QCA cells with covered area 18,144 nm^2 and total area 58,320 nm^2. Using three clocks, two inverters and four majority gates, they designed it. A 0.5-clock latency exists in the demultiplexer. The authors stated that the modular design of the proposed circuit is very simple and may be used to build higher-order circuits [21].

Recently in 2019, Das et al. [22] effectively designed 1:2 demultiplexer using 3-dot QCA cells which covered a cell area of 3888 nm^2 and used a total area of 4860 nm^2. It was a completely new approach, and the complexity of the demultiplexer is 21 QCA cells only. This design has a remarkable high area usage of 80% [22]. But there is no information regarding simulation and layout design parameters. This design is not comparable with the design of this article, but it is a part of the existing work.

In 2013, Sardinha et al. [23] proposed a demultiplexer unit as a part of QCA nanorouter which has been used as an intermediate part of the main circuit using 149

cells. It has covered a cell area of 48,276 nm^2 and used a total area of 208,656 nm^2. Using eight clocks, three inverters and seven majority gates, the design has been implemented. The latency of the circuit is 0.5 clock [23]. It is a 1:4 demultiplexer and is not comparable with the proposed circuit of this article; rather, it is just a part of the existing work. The details of this 1:4 demultiplexer are not mentioned as it is not the main aim of that paper.

All the above-discussed designs are suffering from different issues. For example, many are complex and did not consider energy dissipation or signal flow representation in their analysis. The key gaps in the literature are summarized as follows:

- Seldom design of demultiplexer, unlike multiplexer.
- Simple layout for DeMUX.
- Energy calculation not considered anywhere.
- Detailed analysis with all important parameters missed.

However, this work included all those study gaps and proposed a simple demultiplexer layout. Therefore, this work is novel and would open the scope of higher-ordered demultiplexer design even more easily. The strong point of this article is that here a few top-listed existing demultiplexers [17–22] have been compared with the proposed one. None of the existing articles has focused on all the comparing parameter, whereas this article cares. Energy dissipation analysis using two popular tools QDE and QCAPro is also covered here. This article also included signal flow picture and power dissipation mapping picture.

4 Proposed work

4.1 Brief theoretical explanations

A demultiplexer or DeMUX is a very frequently used and important block in communication systems and digital electronics. It is a combinational circuit that takes single input data and then passes it to anyone of the multiple numbers of output lines, hence known as data distributor. One can say that DeMUX is a converter as it converts input serial data into many output parallel lines. The truth table and block diagram of a digital demultiplexer have been shown in Fig. 6. The demultiplexer has an input line (*D*), output lines (*Y*1, *Y*2) and select line (*S*). The proposed circuit has been designed using two majority gates and one inverter. Both of the majority gates are working as AND gate. The single input of the demultiplexer is directly connected to one of the input lines of the majority gates. Let us consider each majority gate separately. For the lower majority gate, the three inputs are *D*, $\underline{S}$ and '− 1,' whereas the three inputs for the lower majority gates are D, *S_bar* or $\overline{S}$ and '− 1.' The output *Y*1 of the demultiplexer is directly connected to the output of the upper majority gate, and the output *Y*2 of the demultiplexer is directly connected to the output of the lower majority gate. The fixed input '− 1' ensured that the majority gates are acting as AND gate mode. The inverter is used to get the output *S_bar* or
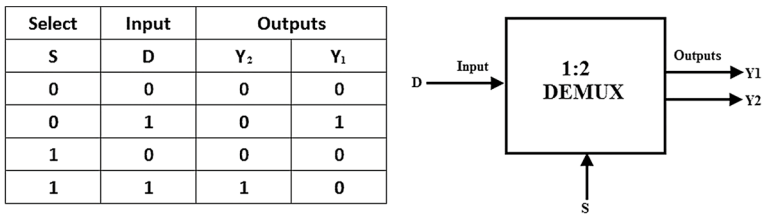
Select	Input	Outputs	
S	D	Y_2	Y_1
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

Fig. 6 Truth table and symbol of 1:2 demultiplexer

$\overline{S}$ from S. The next subsection and the signal flow diagram would help the readers to understand the theoretical and mathematical explanations in further detail.

4.2 Mathematical background

From the basic concept of digital electronics, we know that if there are 'n' output lines and 'm' select lines, then they follow the relation $n = 2^m$ or $m = \log_2 n$. For 1:2 demultiplexer, input line $= 1$, $n = 2$ and $m = 1$. Let, S is the select line, D is the input of the proposed 1:2 QCA demultiplexer and the outputs are $Y1$ and $Y2$ of the proposed demultiplexer. The output lines follow the following equations: $Y1 = D \cdot \overline{S}$ and $Y2 = D \cdot S$ Four input–select line combinations are as follows: For $S = 0$ and $D = 0$, both outputs $Y1$ and $Y2$ are 0; if $S = 0$ and $D = 1$, then $Y1 = 1$ and $Y2 = 0$. For $S = 1$ and $D = 0$, both the outputs $Y1 = Y2 = 0$. If $S = 1$ and $D = 1$, then $Y1 = 0$ and $Y2 = 1$. The implementation of this circuit is possible using two AND gates and one inverter only.

4.3 Simulation: layout

The layout of simple 1:2 DeMUX has been designed in QCADesigner 2.0.3 tool [33] as shown in Fig. 7. The design is very simple as it only used two majority gates where both of them act as AND gates and one NOT gate. It has the D input and two outputs as $Y1$ and $Y2$. The input signal D is going to both of the majority gates; then, the lower majority gate (as shown in Fig. 7) performs AND operation using the select line S and produces the output $Y2$, whereas the upper majority gate (as shown in Fig. 7) performs AND operation using $\overline{S}$ and produces the output $Y1$.

The design specifications are:

Number of cells $= 21$
Cell size $= 18$ nm $\times$ 18 nm
Space between cells $= 2$ nm
Cell area $= 21 \times (18 \times 18) = 6, 804$ nm^2
Area covered $= (9 \times 18) \times (7 \times 18)$ nm$^2 = 20{,}412$ nm^2

How the signal flows from input toward output through internal nodes has been shown in pictorial form in Fig. 8. For simplicity, we have designed the layout only using single layer like most of the existing QCA demultiplexers, whereas it is also
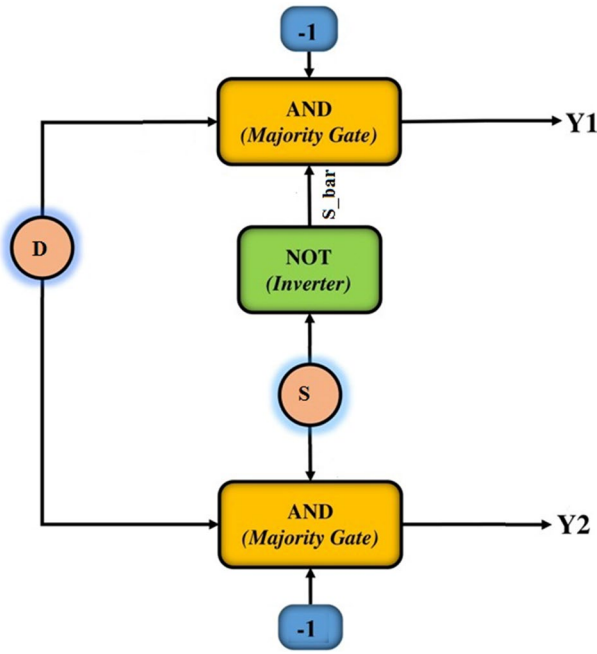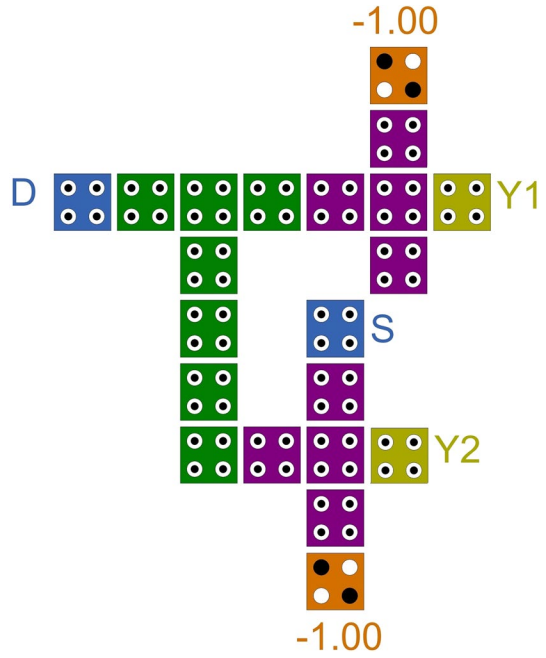
Fig. 7 Proposed DeMUX layout

Fig. 8 Signal flow diagram

possible to implement the proposed design using double layers if the select input 'S' has been put into another layer, but it creates difficulty in higher-order circuit design and energy analysis using QCAPro. Therefore, our design may be considered as the simplest and one of the best QCA layouts.

4.4 Results

The QCA simulation layout and the result can be realized by taking into account the quantum interactions of the resultant electrostatic energies for all possible logic states in every clocked set of QCA cells. Total simulation performed at the environment of the QCADesigner 2.0.3 tool [33] with default simulation parameters of the coherence vector engine. The resultant output for the proposed 1:2 demultiplexer is shown as the normal form of simulation tool in Fig. 9, and the same as the bus form of simulation tool in Fig. 10. The simulation result is justified with the truth table as shown in Fig. 6. For input $D = 0$ and select line $S = 0$, the output will be as $Y1 = 0, Y2 = 0$. Similarly, for input $D = 1$ and select line $S = 0$, the output will be $Y1 = 0, Y2 = 1$. Next, if $D = 1$ and $S = 0$, then both $Y1 = Y2 = 0$. Lastly, for input $D = 1$ and select line $S = 1$, the output will be $Y1 = 1$ and $Y2 = 0$. It is very clear from the simulation result that there is an input–output delay of 0.5 clock of the proposed layout as shown in the outputs, as shown in Figs. 9 and 10.

5 Energy calculation

A detailed analysis of total energy dissipation has been performed using the QCADesigner-E (or QDE) tool [34] and QCAPro tool [35].

5.1 Energy calculation using QDE

As introduced in QDE, QCA cells form a 'bath' of energy if they are separated for each clock cycle. The sum of energy that transfers to the QCA 'bath' is represented as E_{BATH} [40, 41]. Therefore, the total energy dissipation can be expressed as the sum of all energies of E_{BATH}. Three primary components of energy dissipation are E_{CK}, E_{EV} and E_{IO}. All these three energy terms are engaged to transfer energy as follows: E_{CK} transfers to clocks, E_{EV} transfers to environment, and E_{IO} is related to transfer neighbor QCA cells. A point to be noted is that $E_{BATH} = E_{EV}$, and it is indeed an inconsistency [15, 42]. If E_{IN} is the amount of energy entering in cell and E_{OUT} is the amount of energy leaving the cell, then these terms are related as $E_{IO} = E_{IN} - E_{OUT}$. There may be some error E_{RR} in energy calculation, and it may be expressed as $E_{RR} = E_{EV} - (E_{CK} + E_{IO})$ [15, 42]. If the error is negative, then it indicates that the energy has been transferred from the above-mentioned three components. This paper focused on the energy dissipation of the proposed QCA demultiplexer. According to QDE, this energy dissipation has been measured using the 'array coordinates' of QCA cells [34]. The lowest position of the 'co-ordinates' is '[1][3],' and the highest position is '[7][3]' as shown in Fig. 11. The calculation
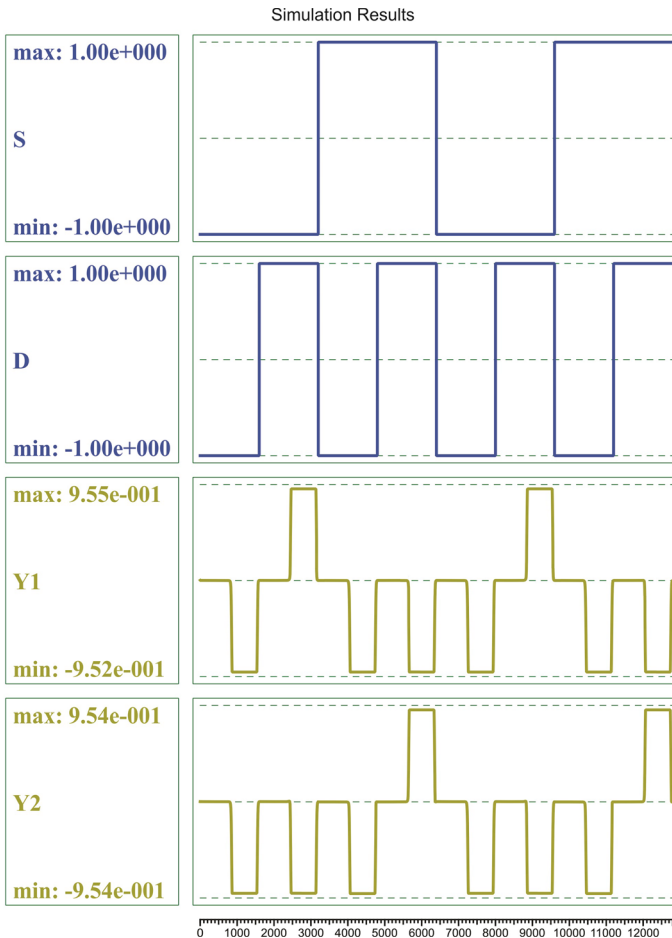
Fig. 9 Simulation output in normal mode

of energy dissipation has been done using 500,000 samples at the coherence vector simulation mode. The total energy consumption of the demultiplexer is 8.64e−003 eV including a negligible error of −8.43e−004 eV, whereas the average energy dissipation per cycle is 7.85e−004 eV with a minute error of −7.66e−005 eV. Energy dissipation of each coordinate has been calculated using the QDE tool, and the highest 'coordinates' energy distribution is shown in Table 1.

5.2 Energy calculation using QCAPro

At the beginning of the clock cycle, all QCA cells are in the depolarized state. Energy is taken from the clocks and neighboring cells to get polarization. Most of this energy is restored to the clock and distributed to the neighboring cells until the
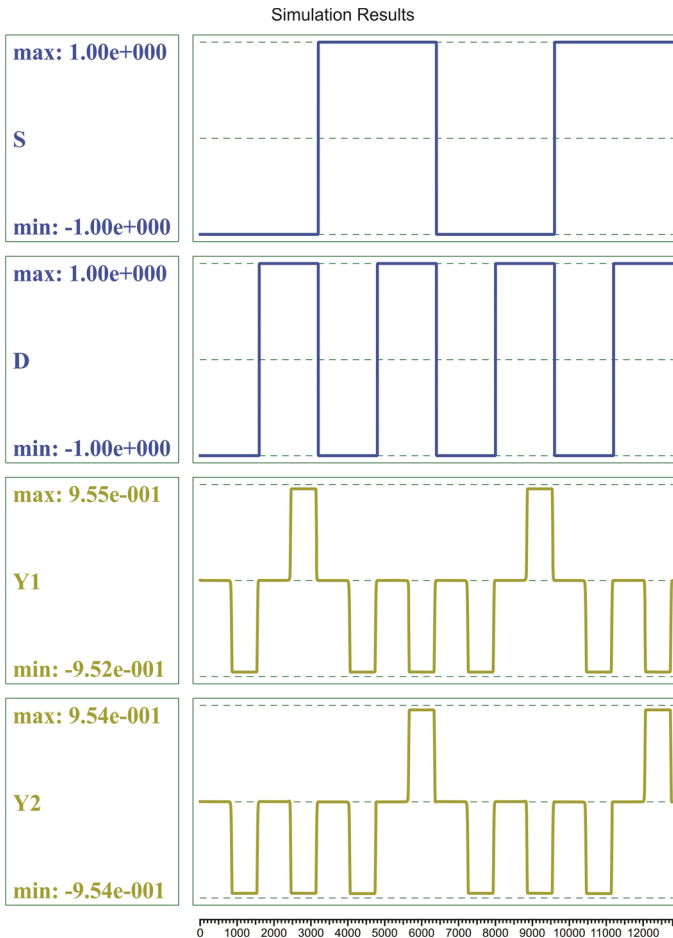
Fig. 10 Simulation output in bus mode

cell becomes depolarized again. However, some portion of the energy dissipates to the environment.

According to [44], there are two energy vectors λ and Γ. Both of them are three dimensional, and QCA cell behavior is completely described by them. λ, known as coherence vector, has three components, namely λ_x, λ_y and λ_z. Γ is known as energy vector and expressed as

$$\Gamma = \frac{1}{\hbar}[-2\gamma, 0, \phi] \tag{2}$$

where $\hbar$ is the reduced Plank constant, γ is the parameter related to tunneling behavior and ϕ is the Coulombic force between cells.

The QCA cell polarization is expressed using the expectation value of the Pauli spin operator as $C = -\langle \hat{\sigma}_z \rangle$.

Fig. 11 Array coordinate of the proposed demultiplexer
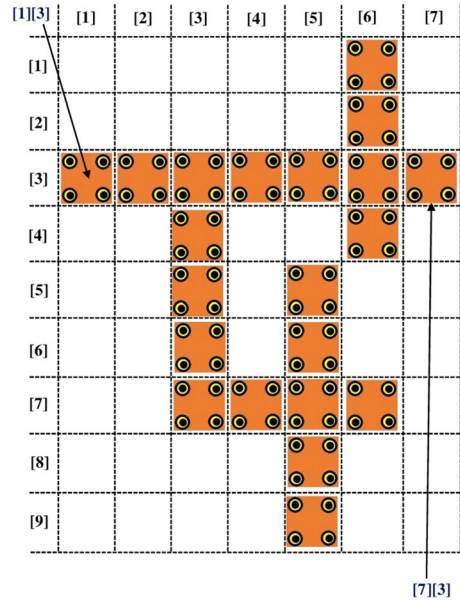
$\widehat{H}_i$ is a 2×2 matrix that represents the Hamiltonian of the ith cell, and $\widehat{H}_i$ is expressed using Hartree–Fock approximation as follows:

$$\widehat{H}_i = \begin{bmatrix} -\frac{E_K}{2} \sum_{j \neq i} C_j f_{i,j} & -\gamma \\ -\gamma & +\frac{E_K}{2} \sum_{j \neq i} C_j f_{i,j} \end{bmatrix} \tag{3}$$

or

$$\widehat{H}_i = \begin{bmatrix} -\frac{E_K}{2}(C_{i-1} + C_{i+1}) & -\gamma \\ -\gamma & +\frac{E_K}{2}(C_{i-1} + C_{i+1}) \end{bmatrix} \tag{4}$$

Here, $\sum_j$ is the sum over the cells, H_i represents the Hamiltonian of the ith cell, $f_{i,j}$ is the geometric factor indicating the electrostatic interactions between ith cell and jth cell and specifies the electronic falloff with the distance between cells, C_j is the polarization of the jth cell and $-C_j = \langle \widehat{\sigma}_z(j) \rangle$, γ = the tunneling energy between two cell states and is controlled by the clocking mechanism. $(C_{i-1} + C_{i+1})$ is the summation of neighboring polarizations. E_K is the kink energy or the energy cost of two neighboring cells having opposite polarization. In other words, if the space is equal between neighboring cells, the $f_{i,j}$ is known as kink energy, the energy affiliated with the energy cost of two cells at ith position and jth position. Kink energy can be expressed as

Table 1 Energy dissipation (eV) of coordinates [7][3] of proposed demultiplexer using QDE

E_{BATH}	5.4783e−006	5.2912e−006	5.7274e−006	5.4783e−006	5.2912e−006	5.7274e−006	5.4783e−006	6.5862e−005	5.2912e−006
E_{CK}	2.3244e−005	1.3205e−005	−6.5951e−005	2.3244e−005	1.3205e−005	−6.5951e−005	2.3244e−005	1.1749e−005	1.3205e−005
E_{IO}	−2.8900e−005	−1.8663e−005	5.9976e−005	−2.8900e−005	−1.8663e−005	5.9976e−005	−2.8900e−005	−8.4373e−005	−1.8663e−005
E_{IN}	−2.8900e−005	−1.8663e−005	5.9976e−005	−2.8900e−005	−1.8663e−005	5.9976e−005	−2.8900e−005	−8.4373e−005	−1.8663e−005
E_{OUT}	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000
E_{RR}	−1.7792e−007	−1.6642e−007	−2.4724e−007	−1.7792e−007	−1.6642e−007	−2.4724e−007	−1.7792e−007	−6.7621e−006	−1.6642e−007
$E_K[0]$:−3.225745e−004	$E_K[1]$:−1.974610e−006	$E_K[2]$:−5.727103e−006	$E_K[3]$:−9.219376e−006	$E_K[4]$:−3.225745e−004	$E_K[5]$:−1.021058e−005	$E_K[6]$:1.483611e−003	$E_K[7]$:4.413817e−005		
$E_{BATH_{total}}$	3.1936e−004	8.9644e−004	1.1801e−003	3.1936e−004	8.7658e−004	1.1801e−003	3.1936e−004	8.9644e−004	8.7658e−004
$E_{CK_{total}}$	8.8491e−004	5.4918e−004	2.8471e−004	8.8491e−004	2.7005e−004	2.8471e−004	8.8491e−004	5.4918e−004	2.7005e−004
$E_{RR_{total}}$	−9.9832e−005	−2.3593e−005	−1.0894e−004	−9.9832e−005	−8.4870e−005	−1.0894e−004	−9.9832e−005	−9.9832e−005	−8.4870e−005

$$E_{i,j} = \frac{1}{4\pi\varepsilon_0\varepsilon_r} \sum_n \sum_m \frac{q_{i,n}q_{j,m}}{|r_{i,n} - r_{i,j}|} \tag{5}$$

For every clock cycle, the expectation value of QCA energy is expressed as

$$E = \langle H \rangle = \frac{\hbar}{2} \times \mathbf{\Gamma} \times \lambda \tag{6}$$

where $\hbar$ is the reduced Plank constant, $\mathbf{\Gamma}$ is the energy environment vector of the cell and the coherence vector is λ. The explicit form of the Hamiltonian vector corresponding to Hamiltonian (5) is

$$\mathbf{\Gamma} = \frac{1}{\hbar}[-2\gamma, 0, E_{\mathrm{K}}\overline{C}] \tag{7}$$

Here, $\overline{C} = C_{i-1} + C_{i+1} =$ the sum of the neighboring polarizations.

The instantaneous power of a QCA cell is expressed as

$$\begin{aligned} P_t &= \frac{\mathrm{d}E(t)}{\mathrm{d}t} \\ &= \frac{\hbar}{2}\left[\frac{\mathrm{d}\mathbf{\Gamma}}{\mathrm{d}t} \cdot \lambda\right] + \frac{\hbar}{2}\left[\mathbf{\Gamma} \cdot \frac{\mathrm{d}\lambda}{\mathrm{d}t}\right] \\ &= P_1 + P_2 \end{aligned} \tag{8}$$

Here, $P_1 =$ the difference of input and output signal power and clocking power to the cell and $P_2 =$ dissipate power [43].

The total energy dissipation of a QCA cell during a complete clock period T_{CK} is

$$\begin{aligned} E_t &= \int_{t_0}^{t_0+T_{\mathrm{CK}}} P\mathrm{d}t' \\ &= \frac{\hbar}{2}\int_{t_0}^{t_0+T_{\mathrm{CK}}} \left(\frac{\mathrm{d}\mathbf{\Gamma}}{\mathrm{d}t} \cdot \lambda + \mathbf{\Gamma} \cdot \frac{\mathrm{d}\lambda}{\mathrm{d}t}\right)\mathrm{d}t' \\ &= \underbrace{\frac{\hbar}{2}\int_{t_0}^{t_0+T_{\mathrm{CK}}} \frac{\mathrm{d}\mathbf{\Gamma}}{\mathrm{d}t} \cdot \lambda\mathrm{d}t'}_{\text{part 1}} + \underbrace{\frac{\hbar}{2}\int_{t_0}^{t_0+T_{\mathrm{CK}}} \mathbf{\Gamma} \cdot \frac{\mathrm{d}\lambda}{\mathrm{d}t}\mathrm{d}t'}_{\text{part 2}} \end{aligned} \tag{9}$$

The 'part 1' in Eq. 9 refers to the energy transfer with the clock (E_{CK}) + the energy transfer to neighboring cells (E_{IO}) during a clock cycle.

$$\underbrace{E_{\mathrm{CK}} + E_{\mathrm{IO}}}_{\text{part 1}} = \frac{\hbar}{2}\int_{t_0}^{t_0+T_{\mathrm{CK}}} \frac{\mathrm{d}\mathbf{\Gamma}}{\mathrm{d}t} \cdot \lambda\mathrm{d}t' \tag{10}$$
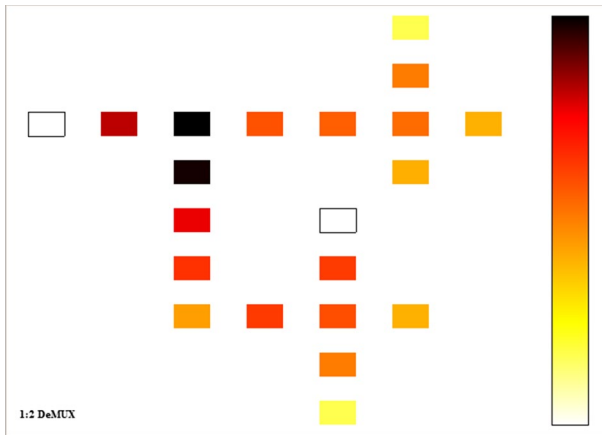
where

Fig. 12 Power dissipation mapping at 2K temperature with $0.5E_k$ tunneling energy

$$E_{\text{CK}} = \frac{1}{2} \int_{t_0}^{t_0+T_{\text{CK}}} \left[\frac{\text{d}(-2\gamma)}{\text{d}t} \cdot \lambda_x \right] \text{d}t' \tag{11}$$

and

$$E_{\text{CK}} = \frac{1}{2} \int_{t_0}^{t_0+T_{\text{CK}}} \left[\frac{\text{d}\varphi}{\text{d}t} \cdot \lambda_z \right] \text{d}t' \tag{12}$$

The 'part 2' in Eq. 9 is the energy transfer to the environment (E_{EV}) during a clock cycle, expressed as

$$E_{\text{EV}} = -\frac{\hbar}{2\tau} \int_{t_0}^{t_0+T_{\text{CK}}} [\mathbf{\Gamma} \cdot \lambda + |\mathbf{\Gamma}| \cdot \tanh(\eta_{\text{th}})]\text{d}t' \tag{13}$$

Here, τ is a technology-dependent parameter and $\eta_{\text{th}} = \hbar|\mathbf{\Gamma}|(2k_{\text{B}}T)^{-1}$= thermal ratio with k_{B} as a Boltzmann constant and T = temperature [35, 43, 44].

The analysis of energy using QCAPro [35] at a fixed temperature of 2K and at three tunneling is shown in Table 2. The leakage energy dissipation at $\gamma = 0.5E_{\text{K}}, \gamma = 1.0E_{\text{K}}$ and $\gamma = 1.5E_{\text{K}}$ is 5.68 meV, 17.81 meV and 32.10 meV, respectively. The switching energy dissipation at $\gamma = 0.5E_{\text{K}}, \gamma = 1.0E_{\text{K}}$ and $\gamma = 1.5E_{\text{K}}$ is 27.18 meV, 23.60 meV and 20.11 meV, respectively, whereas the total energy dissipation at $\gamma = 0.5E_{\text{K}}, \gamma = 1.0E_{\text{K}}$ and $\gamma = 1.5E_{\text{K}}$ is 32.86 meV, 41.41 meV and

Table 2 Energy dissipation using QCAPro

Circuit	Leakage energy dissipation (meV)			Switching energy dissipation (meV)			Total energy dissipation (meV)		
DeMUX	$0.5E_{\text{K}}$	$1.0E_{\text{K}}$	$1.5E_{\text{K}}$	$0.5E_{\text{K}}$	$1.0E_{\text{K}}$	$1.5E_{\text{K}}$	$0.5E_{\text{K}}$	$1.0E_{\text{K}}$	$1.5E_{\text{K}}$
Energy	5.68	17.81	32.10	27.18	23.60	20.11	32.86	41.41	52.21

52.21 meV, respectively. Corresponding power dissipation mapping at temperature 2K with $\gamma = 0.5E_K$ is shown in Fig. 12. The simple color scale of power dissipation mapping using QCAPro [35] is well known, and it states that the lighter coloured cells are dissipating smaller energy than deep coloured cells. Figure 12 ensues that there are only few deep-coloured cells; therefore, it has very small energy dissipation.

6 Analysis

Analysis of various important parameters has been considered below:

Complexity The number of QCA cells necessary to design the layout is the measure of complexity. Low complexity is desirable. The proposed circuit has been designed using 21 QCA cells; therefore, the complexity of the proposed demultiplexer is 21.

Total area It is the total rectangular area required to design the architecture. There are 7 cells horizontally and 9 cells vertically. As we know the area of a small cell is $18 \times 18 \text{ nm}^2$, the total area is $18 \times 18 \times 7 \times 9 \text{ nm}^2$. Here, it is $20,412 \text{ nm}^2$. For a good design, the total area should be small.

Cell area For a good design, the cell area should be small too. It is complexity × one cell area. As we know the area of a small cell is $18 \times 18 \text{ nm}^2$, the proposed comparator has a cell area of $6,804 \text{ nm}^2$.

Area usage The % of area usage is calculated as $\frac{\text{cell area}}{\text{total area}} \times 100\%$. The area usage of the proposed design is 33.33%, and it is a good figure in design perspective as high % value is desirable.

Clocking zones The number of clocking zones used in the proposed design is two, though there are four available clocking zones. For a good design, the use of minimum clocks is desirable.

Inverters used QCA inverters are an important building block. For a good design, the inverter count should be small. Only one inverter is used in the proposed demultiplexer.

Majority gates used The majority gate is another unavoidable building block of QCA circuits. It is used as AND/OR logical functions to implement circuits, and a designer should try to use a minimum number of majority gates. In this design, only two majority gates have been used and both are working as AND functions.

Cross-wiring Wire crossing in QCA layout design should be avoided. The proposed layout completely avoided wire crossing; therefore, the number of wire crossing is zero.

Layer Multilayer QCA layout design is difficult and complex; therefore, single-layer design is preferable. The proposed demultiplexer has been designed in QCA single-layer mode.

Latency It is the input-to-output delay, and there should not be any latency. However, it is almost unavoidable in QCA circuits. This demultiplexer has a latency of 0.5 clock.

QCA-specific cost The cost of QCA circuit is expressed as figure of merit (FoM) [45, 46] with the expression of FoM $= (M^k + I + C^l) \times T^p$, M is the number of majority gates, I is the number of inverters, C is the number of crossovers, T is the delay of the circuit (in terms of numbers of clock phases), and k, l and p are the exponential weightings for majority gate count, crossover count and delay, respectively [45]. Here, we considered $k = l = p = 2$ [46]. For the projected QCA demultiplexer, $M = 2, I = 1, C = 0$ and $T = 2$; therefore, the FoM or cost of the proposed circuit is $(2^2 + 1 + 0) \times 2^2 = 20$. Hence, the cost is very low, as we know a lower cost is desirable.

The cost of QCA circuit may be calculated using another formula as $\text{cost}_{\text{QCA}} = \text{latency}^2 \times \text{total area}$; however, it has not been discussed in this article.

Energy dissipation According to QDE tool [34], the total energy consumption of the demultiplexer is 8.64e−003 eV and the average energy dissipation per cycle is 7.85e−004 eV. However, there are errors in calculations; for example, there is an error of − 8.43e−004 eV in total energy calculation and an error of − 7.66e−005 eV exists in average energy calculation.

According to QCAPro tool [35], the leakage energy dissipation at $\gamma = 0.5E_K, \gamma = 1.0E_K$ and $\gamma = 1.5E_K$ is 5.68 meV, 17.81 meV and 32.10 meV, respectively. The switching energy dissipation at $\gamma = 0.5E_K, \gamma = 1.0E_K$ and $\gamma = 1.5E_K$ is 27.18 meV, 23.60 meV and 20.11 meV, respectively, whereas the total energy dissipation at $\gamma = 0.5E_K, \gamma = 1.0E_K$ and $\gamma = 1.5E_K$ is 32.86 meV, 41.41 meV and 52.21 meV, respectively.

7 Comparisons

This section includes the comparison of the proposed demultiplexer with few topmost existing designs [17–22]. As we discussed, only a few QCA demultiplexers exist in the literature and not all the existing items are efficient. Therefore, we have chosen a few good QCA demultiplexers from the literature that can compete with the proposed design. The detailed comparison is given in Table 3, and it is clear that the design of [19] is the best competitor of the proposed design. However, recently

Table 3 Comparison table

Properties	Iqbal et al. (2013) [17]	Ahmad (2017) [18]	Safoev et al. (2016) [19]	Das et al. (2017) [20]	Shah et al. (2011) [21]	Das et al. (3-dot approach) (2019) [22]	Proposed
Complexity	27	21	21	32	56	12	21
Cell area (nm^2)	8748	6804	6804	10,368	18,144	3888	6804
Total area (nm^2)	23,328	23,328	17,496	26,244	58,320	4860	20,412
Area usage	37.50%	29.16%	38.88%	39.50%	31.11%	80%	33.33%
No. of clocks used	2	2	2	3	3	Not mentioned	2
Latency	2	0.5	1	0.5	2	Not mentioned	0.5
No. of inverters used	2	5	1	1	2	Not mentioned	1
No. of majority gates used	2	0	2	3	4	Not mentioned	2
No. of wire crossing	0	0	0	0	0	0	0
Layer	Single	Single	Single	Single	Single	Single	Single
Cost	24	20	20	90	162	Not applicable	20

proposed 3-dot QCA cell-based demultiplexer is very efficient, but it is not comparable with the current design as many design parameters are not mentioned there and no simulation information is found.

The design proposed by Das et al. [22] has very low complexity, very low cell area and very low total area. But the complexity and cell area of the proposed demultiplexers are comparable with the demultiplexers proposed by Ahmad [18] and Safoev et al. [19]. However, the total area covered by the design in [19] is notable. 1:2 demultiplexer designed in [18, 20] is advantageous in terms of latency and comparable with the proposed design. The total used clocks of the proposed demultiplexer are the same as demultiplexers of [17–19]. The number of inverters used in [19, 20] is the same as the proposed design, and the number of majority gates used in the proposed circuit is equal as the 1:2 demultiplexer in [17, 19]. All designs [17–22] including the proposed one are single-layer design and did not use any cross-wire. However, the cost of the proposed design is comparable to the design mentioned in [18, 19].

Though the DeMUX in [18, 19] is comparable with the proposed DeMUX, DeMUX in [19] has larger latency or input–output delay and DeMUX in [18] is inferior in other values of parameters. Therefore, as a whole, our demultiplexer would be very efficient module to design higher-order circuits.

The comparisons of complexity, cost and latency are shown in Fig. 13. As the authors of [22] have used 3-dot QCA approach and have not mentioned any design details, this design should be ignored. It is clear from the figure that the complexity and the cost of [18, 19] are the same as the proposed design. The latency of [18, 20] and the proposed circuit is equal.

The area comparison is shown in Fig. 14, and the design of [22] has a smaller value. But the cell area of the circuit in [18, 19] is comparable with the current design; however, the total area of the proposed design is comparable with the demultiplexer in [19].
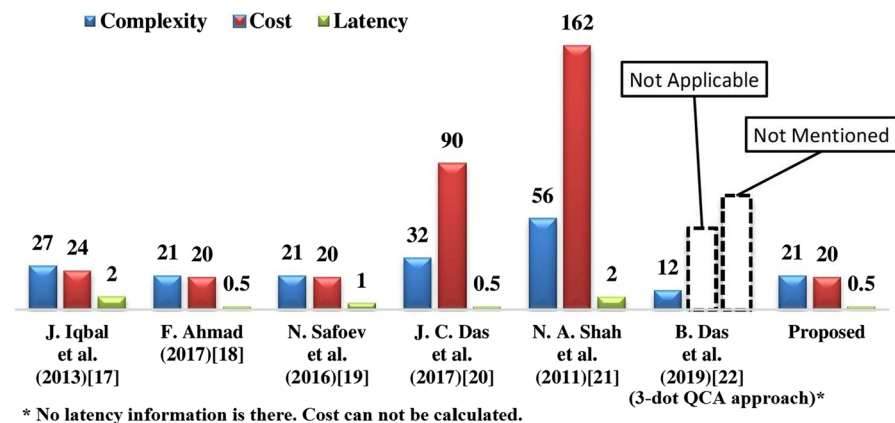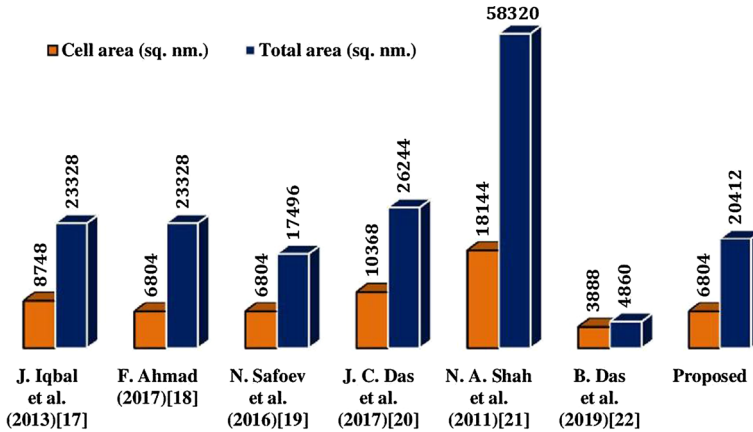

Fig. 13 Complexity, cost and latency comparisons
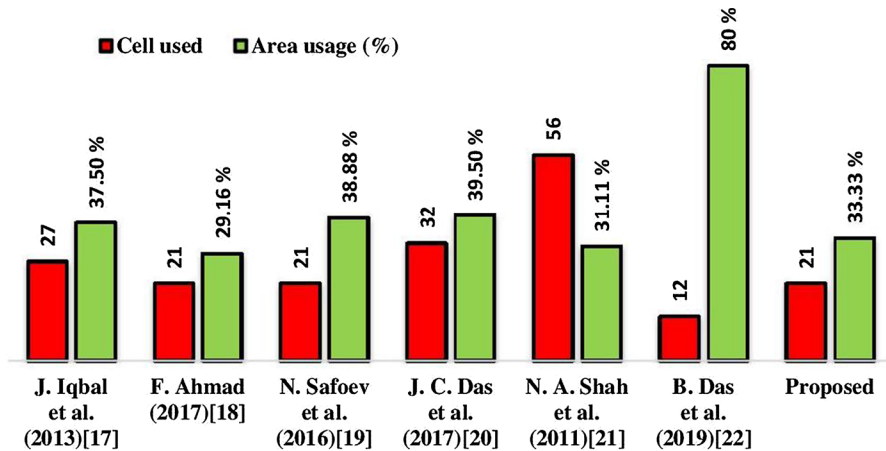
Fig. 14 Area comparisons

Fig. 15 Cell used and area usage comparisons

Used cell and area usage comparisons are shown in Fig. 15 to clearly understand the comparison. The used cell is nothing but complexity, which has been reported already. According to this figure, the best design is mentioned in [22]. But the area usage of the proposed design is comparable with the design mentioned in [18, 21].

Different design parameters-related comparisons are shown in Fig. 16. Total used clocks of the proposed demultiplexer is the same as demultiplexers of [17–19]. The number of inverters used in [19, 20] is the same as the proposed design, and the number of majority gates used in the proposed circuit is equal as the 1:2 demultiplexer in [17, 19].
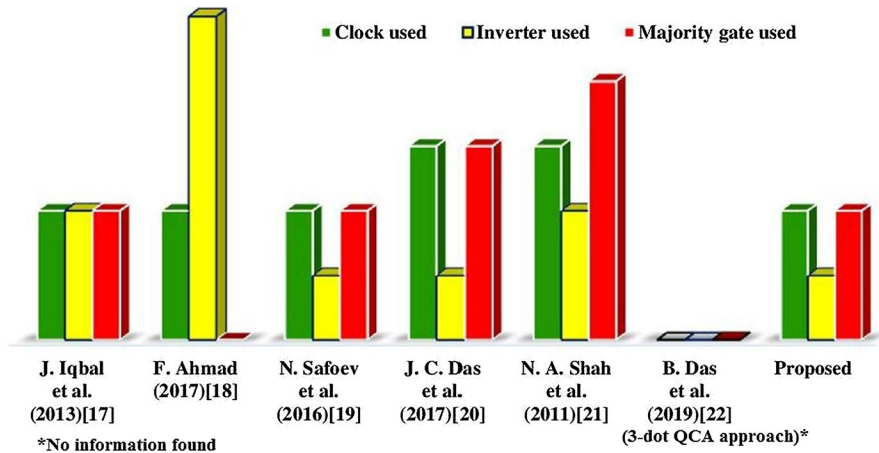
Fig. 16 Clock, inverter and majority gate comparisons

8 Conclusions and future perspective

This paper encompasses novel and proficient 1:2 demultiplexer which signifies almost every characteristic of quantum dot cellular automata. This paper proposed a very simple design, and it has many key advantages. We are hopeful about a significant contribution to QCA research by designing this work. The major advantage of the proposed structure is that it has a simple layout and modular approach with negligible latency; therefore, it can be used in different areas such as nanocommunication, reversible computing and nanocomputing. The proposed logic is too simple as it is coplanar and the proposed design uses only three basic logic gates including two traditional 3-input majority gates and one inverter, which make the cost comparable. The proposed design does not have any wire crossing, which makes it simpler and opened the avenue to build a larger device using it. The proposed structure is notably robust enough as per the energy dissipation analysis, which is very minute. There is a detailed analysis in almost every parameter of QCA circuits' like cell count, cell area, the number of clock zones and, last but not the least, energy dissipation. Like all QCA circuits, the proposed design also has a small latency, but it is negligible. However, the authors planned to eliminate it and left it as the next work.

In the future, it is possible to design higher-order circuits using the proposed block, especially in nanocommunication areas. The proposed QCA demultiplexer may help to design nanorouter or nanoswitch for nanocommunication network. It may also help to design higher-order demultiplexer-based circuits for nanocomputing.

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