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Parity-preserving reversible flip-flops with low quantum cost in nanoscale

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Abstract
In recent years, reversible logic has attracted high importance because of its in-cognitive property of reduction in energy dissipation which is the main requirement in low-power digital circuits. Reversible logic is one of emerging fields of research, which is used in various fields such as low-power CMOS, DNA computing, quantum computing, fault tolerance and nanotechnology. A circuit is reversible if it has the same number of inputs and outputs, and there is a one-to-one correspondence between them. A reversible circuit is parity-preserving if the EXOR of the inputs is equal to the EXOR of the outputs. Flip-flops are considered as one of the most important digital designs that are widely used as building blocks in the design of sequential circuits. In this paper, two new 4×4 parity-preserving reversible blocks are first proposed, called PNM1 and PNM2, respectively. Quantum syntheses of the proposed blocks are carried out using the Miller et al. method. In the following, effective designs of parity-preserving reversible D, T and J-K flip-flops along with their master–slave versions are introduced using the proposed parity-preserving reversible blocks and DFG gates. Finally, a 4-bit asynchronous up-counter is designed using the proposed parity-preserving reversible D flip-flop and FRG gate. The results of the comparisons show that although the proposed structures are close to previous designs in terms of gate count, constant input and garbage output criteria, they are superior in terms of quantum cost.

Keywords Nanotechnology · Reversible logic · Parity-preserving · Flip-flop · Master–slave

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1 Introduction

Landauer proved that the thermal energy generated by the loss of one bit of information during processing is equal to *kTLn2* Joules of heat energy, where k is the Boltzmann's constant and T is the absolute temperature of the environment [1]. Bennett showed that in order to avoid energy waste in computational circuits, the processes should be reversible; that is, if reversible logic gates are used, there is no power consumption, and no energy is lost [2]. A block is reversible if the number of inputs with the number of outputs is equal, and there is a one-to-one correspondence between them [3]. In other words, the input vector can be retrieved through the output vector. In reversible logic, feedback loop and fan-out (fan-out = 1) are not allowed [3]. Of course, Toffoli showed that feedback is possible in reversible circuits [4]. Accordingly, a sequential circuit is reversible if its combinational part is reversible. Fredkin used this concept to propose the first reversible sequential circuit design, which had a feedback loop from the output. Reversible logic is widely applied in a wide variety of research fields such as low-power CMOS [5], optical technology [6], quantum computing [7], DNA computing [8] and nanotechnology [9]. In order to properly synthesize the reversible circuits, it is necessary that criteria such as, gate count (GC), number of constant inputs (CI), garbage outputs (GO), and quantum cost (QC) are optimized, which are defined as follows [10–19]:

Gate count (GC) This criterion refers to the number of gates used in reversible circuit design.

Constant inputs (CI) This criterion refers to the number of inputs that are set to a constant value (0 or 1) for the synthesis of the logical function.

Garbage outputs (GO) This indicates the number of unwanted outputs which are added to make a function reversible.

Quantum cost (QC) This refers to the cost of reversible circuits based on the number of elementary quantum gates. The QC of reversible 1×1 gate (such as the NOT gate) and 2×2 gates (such as the controlled-V, controlled-V^+, CNOT and integrated 2-qubit gates) is considered to be equal to one.

Logical calculation (LC) A number of gates such as EXOR, AND and NOT are used to construct a logical function.

One of the most issues in the reversible circuits is the fault-detection problem. The parity check is considered as one of the straightforward and low-cost approaches to identify faults in the communication and digital systems. Hence, the parity-preserving can be used well in the reversible circuits with an effective cost. A reversible block is called parity-preserving if the EXOR of the inputs is equal to EXOR of the outputs [20].

Fig. 1 Quantum representation of NOT gate

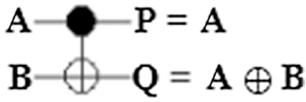


Fig. 2 Quantum representation of CNOT gate

So far, several reversible computational circuits with parity-preserving capability are introduced, such as adder [21], multiplier [22, 23], divider [24], ALU [25] and flip-flops [26].

Among these, flip-flops are of particular importance since they are frequently used as the building blocks in the sequential circuits.

The main scientific contributions of this paper are summed up as follows:

- Proposing two new parity-preserving reversible blocks with the low quantum cost.
- Quantum synthesis of the proposed blocks is performed using the Miller et al. method.
- Introducing effective designs of D, T and J-K flip-flops and their master–slave versions using the proposed parity-preserving reversible blocks.
- The comparison results indicate that the proposed circuits are better than previous related works.

The rest of the paper is as follows: In Sect. 2, the basis of the reversible logic and Miller et al. synthesis algorithm are described. In Sect. 3, the related works are reviewed. In Sect. 4, the proposed new parity-preserving reversible blocks are introduced. In Sect. 5, the simulation results and comparisons are presented. Finally, Sect. 6 concludes the paper.

2 An overview of reversible logic

In this section, we introduce some basic concepts in reversible logic, including preliminaries, some parity-preserving reversible gates and Miller et al. synthesis algorithm.

A gate/block is called reversible if there is a one-to-one correspondence between the inputs and the outputs. The function F, with the input vector $I_v=(I_1, I_2, \ldots, I_n)$ and the output vector $O_v=(O_1, O_2, \ldots, O_n)$, is reversible if and only if there is a one-to-one correspondence between the input and output vectors [27].

A gate/block is parity-preserving if the parity of the inputs is equal to the parity of the outputs. Therefore, if a fault takes place on one of the outputs, it can be detected. Furthermore, a reversible circuit is fault-tolerant if it is only made from the parity-preserving reversible gates/blocks [20].

Fig. 3 Quantum realization of **a** controlled-V gate and **b** controlled-V^+ gate

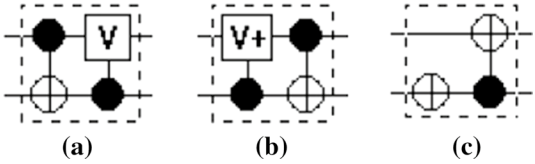


Fig. 4 Quantum realization of three integrated qubit gates: **a** pattern 1, **b** pattern 2 and **c** pattern 3

2.1 Basic reversible gates

NOT gate

A NOT gate is a 1×1 quantum gate with QC equal to 1, as shown in Fig. 1 [28].

Controlled-NOT gate (CNOT)

The CNOT gate, which is also known as the Feynman gate (FG), is a 2×2 reversible gate that has the inputs control (A) and target (B) and the produces the outputs $P=A$ and $Q=A\oplus B$. The CNOT quantum representation is shown in Fig. 2. As can be seen, if the control input is equal to 1 ($A=1$), the output Q will be the inverse of the target input ($\bar{B}$); otherwise, the target input (B) is transferred unchanged to the output Q [29].

Controlled-V and controlled-V^+ gates

Controlled-V and controlled-V^+ gates are known as primary 2×2 quantum gates and are shown in Fig. 3a and b, respectively [10, 28].

V and V^+ matrices are provided in Eqs. (1) and (2), respectively [10, 28, 30–32]:

$$V=\frac{1+i}{2}\begin{pmatrix}1 & -i\\ -i & 1\end{pmatrix} \tag{1}$$

$$V^+=\frac{1}{i+1}\begin{pmatrix}1 & -1/i\\ i & 1\end{pmatrix} \tag{2}$$

Also, V and V^+ matrices have the following properties [10, 28]:

$$V\times V=\text{NOT} \tag{3}$$

$$V^+\times V=V\times V^+=I \tag{4}$$

$$V^+\times V^+=\text{NOT} \tag{5}$$

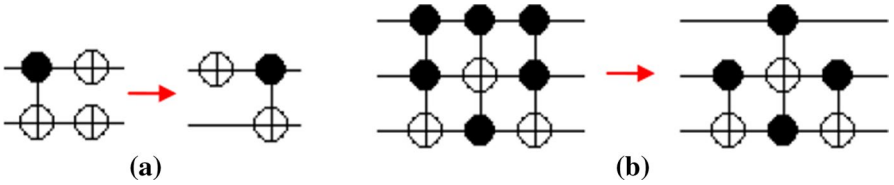


Fig. 5 Templates with 2 or 3 inputs

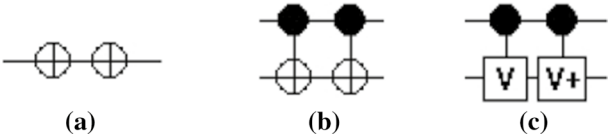


Fig. 6 Simplification rules for minimizing the quantum cost of the reversible circuits

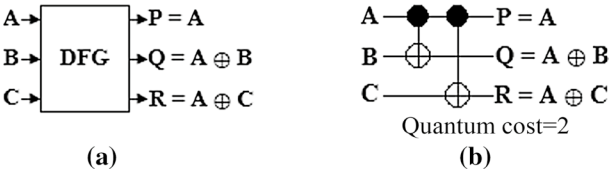


Fig. 7 Reversible DFG gate: **a** circuit view and **b** quantum realization

As seen in Fig. 3, if the control input A is equal to 1 ($A = 1$), controlled-V and controlled-V^+ gates result in $V(B)$ and $V^+(B)$ outputs, respectively. Otherwise, target input B will be transferred unchanged to the output. Their QC is 1.

The quantum realization of the three integrated 2-qubit gates is shown in Fig. 4. It should be mentioned that each dotted rectangle in Fig. 4 is equivalent to a 2×2 gate, and its QC is 1 [11, 12, 32, 33].

A common method to simplifying of quantum circuits is template matching. Two practical templates are illustrated in Fig. 5 showing possible reductions for several cascades [34, 35].

It should be noted that the quantum cost of the circuits shown in Fig. 6 is equal to zero [35–39].

2.2 Basic parity-preserving reversible gates

So far, various parity-preserving reversible gates/blocks have been introduced [14, 26, 40–46]. In the following, we introduce the three most important gates, including double Feynman gate (DFG), Fredkin gate (FRG) and new fault tolerance gate (NFT).

Double Feynman gate (DFG) Circuit representation and quantum realization of the 3×3 parity-preserving reversible DFG gate are illustrated in Fig. 7 [20].

Table 1 Truth table of the DFG gate

A	*B*	*C*	*P*	*Q*	*R*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

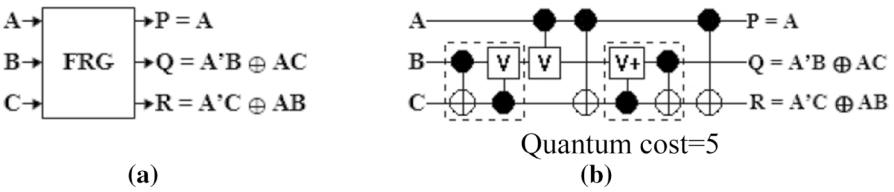


Fig. 8 Reversible FRG gate: **a** circuit view and **b** quantum realization

Table 2 Truth table of the FRG gate

A	*B*	*C*	*P*	*Q*	*R*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

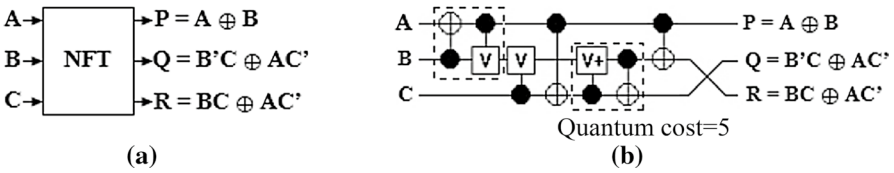


Fig. 9 Reversible NFT gate: **a** circuit view and **b** quantum realization

Table 3 Truth table of the NFT gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

Its truth table is also provided in Table 1 so that its output equations are $P=A$, $Q=A\oplus B$ and $R=A\oplus C$. Moreover, its quantum cost is 2 and the logical calculation is 2α.

Fredkin gate (FRG) Circuit representation and quantum realization of the 3×3 parity-preserving reversible FRG gate are shown in Fig. 8 [47]. Its truth table is also given in Table 2 so that its output equations are $P=A$, $Q=A'B\oplus AC$ and $R=A'C\oplus AB$. In addition, its quantum cost is 5 and logical calculation is $2\alpha+4\beta+1\delta$.

New fault tolerance gate (NFT) Circuit representation and quantum realization of the 3×3 parity-preserving reversible NFT gate are shown in Fig. 9 [48]. Its truth table is also given in Table 3 so that its output equations are $P=A\oplus B$, $Q=B'C\oplus AC'$ and $R=BC\oplus AC'$. Moreover, its quantum cost is 5 and the logical calculation is $3\alpha+3\beta+2\delta$.

2.3 Miller synthesis algorithm

Miller et al. synthesis algorithm is a transformation-based approach that is able to synthesis a reversible circuit in terms of $n\times n$ Toffoli gates. In this method, a circuit is built by a single pass through the specification with minimal look ahead and no back-tracking [34]. Basic Miller et al. synthesis algorithm is given as follows [34].

Consider, an m-input, m-output, totally specified Boolean function f (X), $X=\{x_1, x_2 \ldots x_m\}$ is reversible if it maps each input assignment to a unique output assignment. In the other words, a reversible function specified as a mapping over $\{0, 1 \ldots 2^m-1\}$.

To start, a basic naive and greedy scheme is utilized that specifies Toffoli gates only on the output side of the specification.

2.4 Basic algorithm

Step 1 If $f(0)\neq0$, invert the outputs corresponding to 1 bits in $f(0)$. Each inversion needs a 1×1 Toffoli gate ($TOF1$). The transformed function f^+ has $f^+(0)=0$.

Step 2 Assume each i in turn for $1 \le i < 2^m - 1$ letting f^+ indicate the current reversible specification. If $f^+(i) = i$, no transformation and therefore no Toffoli gate are needed for this i. Otherwise, gates are needed to transform the specification to a new specification with $f^{++}(i) = i$. The required gates have to map $f^+(i) \rightarrow i$.

Let p be the bit sequence with 1's in all positions where the binary expansion of i is 1, while the expansion of $f^+(i)$ is 0. These are the 1 bits that should be added in transforming $f^+(i) \rightarrow i$. Conversely, let q be the bit sequence with 1's in all positions where the expansion of i is 0, while the expansion of $f^+(i)$ is 1. q specifies the bits to be deleted in the transformation.

For each $p_j = 1$, utilize the Toffoli gate with control lines corresponding to all outputs in positions where the expansion of i is 1 and whose target line is the output in position j. Then, for each $q_k = 1$, apply the Toffoli gate with control lines corresponding to all outputs in positions where the expansion of $f^+(i)$ is 1 and whose target line is the output in position k.

3 Related works

In 2006, Thapliyal and Srinivas [49], using eight Fredkin gates (FRG), proposed a parity-preserving reversible T flip-flop, which has GC = 8, CI = 11, GO = 11 and QC = 40. Also, they provided a parity-preserving reversible J-K flip-flop using seven FRG gate which has GC = 7, CI = 9, GO = 10 and QC = 35. Moreover, they introduced D, T, J-K master–slave flip-flops. D master–slave flip-flop has GC = 5, CI = 6, GO = 6 and QC = 25. T master–slave flip-flop has GC = 23, CI = 32 and GO = 35, and QC = 115. J-K master–slave flip-flop has GC = 22, CI = 30, GO = 32 and QC = 110.

In 2010, Thapliyal and Ranganathan, using two reversible Fredkin gates (FRGs), proposed a parity-preserving reversible D flip-flop, which has GC = 2, CI = 2, GO = 2 and QC = 10 [50]. Also, they presented a parity-preserving reversible T flip-flop using three FRG gates, in which the GC = 3, CI = 3, GO = 3 and QC = 15. They also presented a parity-preserving reversible J-K flip-flop using four FRG gates, in which the GC = 4, CI = 4, GO = 5 and QC = 20.

In 2011, Haghparast and Navi, using one FRG gate as well as one double Feynman gate (DFG), proposed a reversible D latch, which has GC = 2, CI = 1 as well as GO = 2 and QC = 7 [51].

In 2012, Gharajeh and Haghparast first suggested a new parity-preserving reversible gate, called Unit4, and then presented a fault-tolerant reversible D flip-flop using one Unit4 gate in which GC = 1, CI = 3 as well as GO = 3 and QC = 10 [41].

In 2014, Pareek et al. first suggested a new parity-preserving reversible gate, called PAREEK gate and then presented a parity-preserving reversible D flip-flop, using PAREEK gate, with GC = 1, CI = 1 as well as GO = 2 and QC = 7 [40].

Also, in 2014, Pareek [52] presented a parity-preserving reversible D flip-flop, using PAREEK and DFG gates, with GC = 2, CI = 3, GO = 3 and QC = 9 and also, presented a parity-preserving reversible T flip-flop, using PAREEK and DFG gates, with GC = 2, CI = 2 as well as GO = 2 and QC = 9. Also, they provided a parity-preserving reversible J-K flip-flop using FRG, DFG and PAREEK gates, in

Table 4 A brief description of the parity-preserving reversible flip-flops designs

Designs	GC	CI	GO	QC	LC
D flip-flop designs with output Q					
Haghparast and Navi [51]	2	1	2	7	$4\alpha+4\beta+1\delta$
Pareek et al. [40]	1	1	2	7	$3\alpha+2\beta+1\delta$
D flip-flop designs with outputs Q and $\bar{Q}$					
Misra et al. [26]	2	3	3	8	$6\alpha+2\beta+1\delta$
Thapliyal and Ranganathan [50]	2	2	2	10	$4\alpha+8\beta+2\delta$
Gharajeh and Haghparast [41]	1	2	3	10	$8\alpha+16\beta+8\delta$
Pareek [52]	2	3	3	9	$5\alpha+3\beta+1\delta$
Goswami et al. [53]	2	3	2	19	$18\alpha+4\beta+1\delta$
T flip-flop designs with outputs Q and $\bar{Q}$					
Pareek [52]	2	2	2	9	$5\alpha+2\beta+1\delta$
Thapliyal and Ranganathan [50]	3	3	3	15	$6\alpha+12\beta+3\delta$
Misra et al. [26]	2	2	2	8	$6\alpha+2\beta+1\delta$
Thapliyal and Srinivas [49]	8	11	11	40	$16\alpha+32\beta+8\delta$
J-K flip-flop designs with outputs Q and $\bar{Q}$					
Pareek [52]	4	5	6	19	$9\alpha+10\beta+3\delta$
Thapliyal and Ranganathan [50]	4	4	5	20	$8\alpha+16\beta+4\delta$
Thapliyal and Srinivas [49]	7	9	10	35	$14\alpha+28\beta+7\delta$
Master–slave D flip-flop designs with output Q					
Pareek [52]	2	2	3	14	$6\alpha+4\beta+2\delta$
Master–slave D flip-flop designs with outputs Q and $\bar{Q}$					
Thapliyal and Srinivas [49]	5	6	6	25	$10\alpha+20\beta+5\delta$
Goswami et al. [53]	4	5	4	38	$36\alpha+8\beta+2\delta$
Master–slave T flip-flop designs with outputs Q and $\bar{Q}$					
Thapliyal and Srinivas [49]	23	32	35	115	$46\alpha+92\beta+23\delta$
Master–slave J-K flip-flop designs with outputs Q and $\bar{Q}$					
Thapliyal and Srinivas [49]	22	30	32	110	$44\alpha+88\beta+22\delta$

which GC = 4, CI = 5 as well as GO = 6 and QC = 19. They also provided a parity-preserving reversible master–slave D flip-flop using two PAREEK gates, in which GC = 2, CI = 2 as well as GO = 3 and QC = 14.

In 2017, Misra et al. first proposed a new parity-preserving reversible gate, called RCQCA gate, and then presented a parity-preserving reversible D flip-flop, using RCQCA and DFG gates, with GC = 2, CI = 3, as well as GO = 3 and QC = 8 [26]. Also, they provided a parity-preserving reversible T flip-flop using RCQCA and DFG gates, in which GC = 2, CI = 2, GO = 2 and QC = 8.

In 2018, Goswami et al. [53] first proposed two new parity-preserving reversible block, called TFR and TF2G, and then presented a parity-preserving reversible D flip-flop, using one TFR and one TF2G gates, with GC = 2, CI = 3, as well as GO = 3 and QC = 19. Also, they provided a parity-preserving reversible

Table 5 Truth table of the proposed parity-preserving reversible block, PNM1

EXOR inputs	*A*	*B*	*C*	*D*	*P*	*Q*	*R*	*S*	EXOR outputs
0	0	0	0	0	1	1	0	0	0
1	0	0	0	1	1	1	0	1	1
1	0	0	1	0	1	1	1	0	1
0	0	0	1	1	1	1	1	1	0
1	0	1	0	0	0	0	0	1	1
0	0	1	0	1	0	0	1	1	0
0	0	1	1	0	0	0	0	0	0
1	0	1	1	1	0	0	1	0	1
1	1	0	0	0	0	1	0	0	1
0	1	0	0	1	0	1	0	1	0
0	1	0	1	0	0	1	1	0	0
1	1	0	1	1	0	1	1	1	1
0	1	1	0	0	1	0	0	1	0
1	1	1	0	1	1	0	1	1	1
1	1	1	1	0	1	0	0	0	1
0	1	1	1	1	1	0	1	0	0

master–slave D flip-flop using two TFR and two TF2G gates, in which GC = 4, CI = 5, GO = 4 and QC = 38.

Moreover, in Table 4, a summary of the previous parity-preserving reversible flip-flops designs is provided.

4 Proposed parity-preserving reversible designs

In this section, we first propose two effective parity-preserving reversible blocks and then, using these blocks, various new parity-preserving reversible flip-flops are introduced.

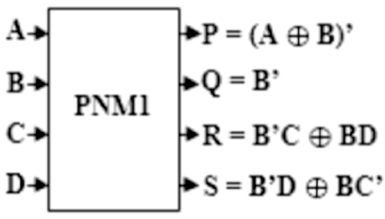


Fig. 10 Circuit representation of the proposed PNM1 block

Table 6 Steps to apply the Miller et al. synthesis on the proposed PNM1 block

Inputs				Outputs				Step 1				Step 2				Step 3				Step 4				Step 5				Step 6			
								Invert P and Q				If ($Q=1$), then invert P				If ($Q=1$), then invert S				If ($Q=1$ and $R=1$), then invert S				If ($Q=1$ and $S=1$), then invert R				If ($Q=1$ and $R=1$), then invert S			
A	B	C	D	P	Q	R	S	P	Q	R	S	P	Q	R	S	P	Q	R	S	P	Q	R	S	P	Q	R	S	P	Q	R	S
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
0	0	1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	0	0	0	0	1	1	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	0	0	1	1	1	0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1	0	1	0	1	0	1	0	1	1	1	0	1	1	0
0	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	0	1	1	1	0	1	1	0	0	1	1	0	0	1	1	1
1	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
1	0	0	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
1	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	0	1	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1
1	1	0	0	1	0	0	1	0	1	0	1	1	1	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
1	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	0	1
1	1	1	0	1	0	0	0	0	1	0	0	1	1	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	0	1	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1

4.1 Proposed parity-preserving reversible blocks

4.1.1 Proposed block, PNM1

The truth table of the proposed 4×4 parity-preserving reversible block is shown in Table 5. Each input vector is mapped individually to an output vector. The proposed reversible structure is called the PNM1 block.

The output equations of the PNM1 block can be determined as follows:

$$P(A, B, C, D) = (A \oplus B)' \quad (1)$$

$$Q(A, B, C, D) = B' \quad (2)$$

$$R(A, B, C, D) = B'C \oplus BD \quad (3)$$

$$S(A, B, C, D) = B'D \oplus BC' \quad (4)$$

The circuit representation of the PNM1 block is shown in Fig. 10.

In order to calculate the quantum cost of the proposed reversible block, it is necessary first to be implemented using the NCT library (NOT-CNOT and Toffoli). For this purpose, the synthesis approach provided by Miller et al. is used [34]. The Miller et al. synthesis algorithm is a greedy method that determined the Toffoli gates only on the output side of the specification. The steps of the Miller algorithm in order to obtain the inputs via the outputs are shown in Table 6.

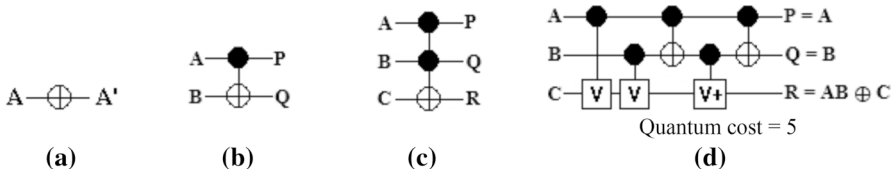


Fig. 11 Toffoli gates: **a** TOF1(*A*), **b** TOF2(*A*, *B*), **c** TOF3(*A*, *B*, *C*) and **d** quantum realization of TOF3(*A*, *B*, *C*)

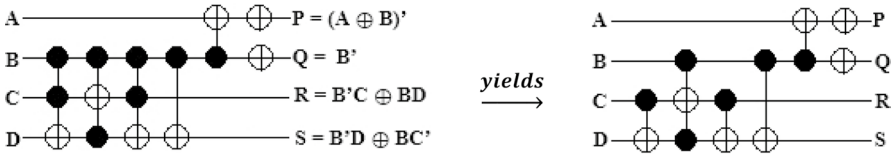


Fig. 12 NCT-based circuit of the proposed PNM1 block

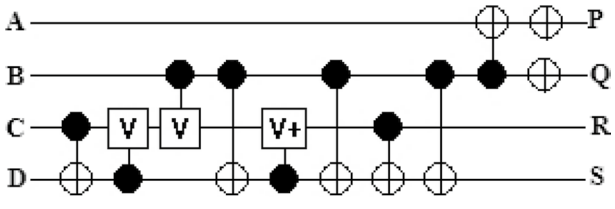


Fig. 13 NCV-based circuit of the proposed PNM1 block

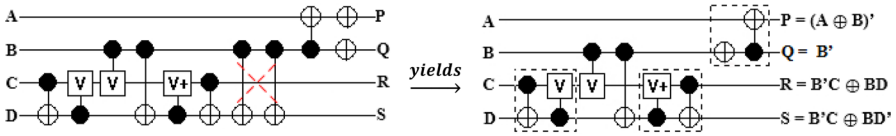


Fig. 14 The optimized NCV of the proposed PNM1 block

Table 7 Truth table of the proposed parity-preserving reversible block, PNM2

EXOR inputs	*A*	*B*	*C*	*D*	*P*	*Q*	*R*	*S*	EXOR outputs
0	0	0	0	0	0	1	1	0	0
1	0	0	0	1	0	1	1	1	1
1	0	0	1	0	0	1	0	0	1
0	0	0	1	1	0	1	0	1	0
1	0	1	0	0	0	0	1	0	1
0	0	1	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0	1	0
1	0	1	1	1	1	0	0	0	1
1	1	0	0	0	1	0	1	1	1
0	1	0	0	1	1	0	1	0	0
0	1	0	1	0	0	0	0	0	0
1	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	1	0
1	1	1	0	1	1	1	1	0	1
1	1	1	1	0	1	1	0	1	1
0	1	1	1	1	1	1	0	0	0

An $n \times n$ Toffoli gate (TOFn (x_1, x_2, …, x_n)) consists of $(n-1)$ control lines that transit through the gate unchanged and a target line on which the value is inverted if all the control lines are equal to value '1.' TOF1 (A) is the special case that there are no control lines; therefore, x_1 always invert. It is called NOT gate. TOF2 (A, B) is called Feynman or controlled-NOT gate (CNOT). TOF3 (A, B, C) is often termed to simply as a Toffoli gate. These gates are illustrated in Fig. 11.

As can be seen from Table 6,

- Step 1 identifies TOF1 (P, Q) giving Step 2
- Step 2 identifies TOF2 (Q, P) giving Step 3
- Step 3 identifies TOF2 (Q, S) giving Step 4
- Step 4 identifies TOF3 (Q, R, S) giving Step 5
- Step 5 identifies TOF3 (Q, S, R) giving Step 6
- Step 6 identifies TOF3 (Q, R, S).

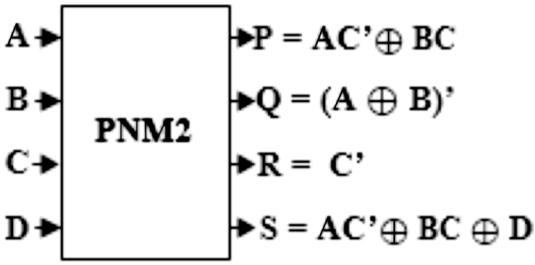


Fig. 15 Circuit representation of the proposed PNM2 block

Table 8 Steps to apply the Miller et al. synthesis on the proposed PNM2 block

Inputs				Outputs				Step 1				Step 2				Step 3				Step 4			
								Invert Q and R				If ($P=1$), then invert				If ($Q=1$ and $R=1$), then invert P				If ($P=1$), then invert Q			
A	B	C	D	P	Q	R	S	P	Q	R	S	P	Q	R	S	P	Q	R	S	P	Q	R	S
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
0	0	1	1	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	1	0	1	0	0	1	1	1	1	1	1	1	1	0	0	1	1	0	0	1	1	0
0	1	1	1	1	0	0	0	1	1	1	0	1	1	1	1	0	1	1	1	0	1	1	1
1	0	0	0	1	0	1	1	1	1	0	1	1	1	0	0	1	1	0	0	1	0	0	0
1	0	0	1	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	0	1
1	0	1	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	1	0	1	0	1	0
1	0	1	1	0	0	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1
1	1	0	0	1	1	1	1	1	0	0	1	1	0	0	0	1	0	0	0	1	1	0	0
1	1	0	1	1	1	1	0	1	0	0	0	1	0	0	1	1	0	0	1	1	1	0	1
1	1	1	0	1	1	0	1	1	0	1	1	1	0	1	0	1	0	1	0	1	1	1	0
1	1	1	1	1	1	0	0	1	0	1	0	1	0	1	1	1	0	1	1	1	1	1	1

It should be noted that the TOF gates are determined from the output side to the input side. The Toffoli-based circuit of the proposed PNM1 block is illustrated in Fig. 12.

Given that the quantum cost of the primitive gates 1×1 and 2×2 is one, then the initial quantum cost of the proposed PNM1 block is 11.

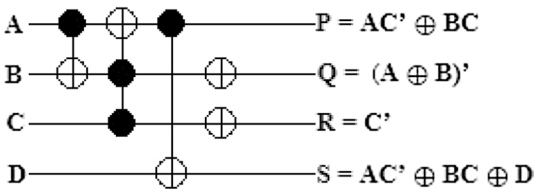


Fig. 16 NCV-based circuit of the proposed PNM2 block

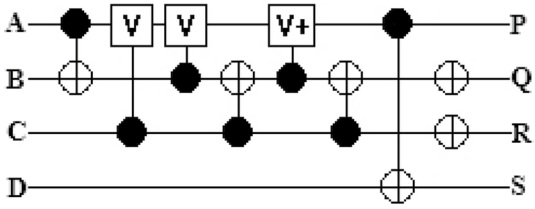


Fig. 17 NCV-based circuit of the proposed PNM2 block

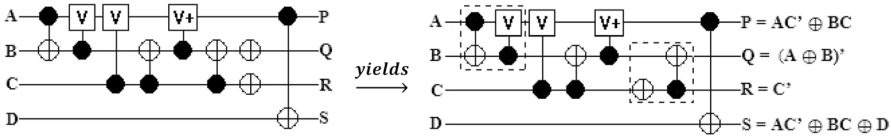


Fig. 18 The optimized NCV of the proposed PNM2 block

Moreover, according to Fig. 12, the NCV display of the proposed PNM1 block is shown in Fig. 13.

After simplifying the circuit shown in Fig. 13, according to the simplification rules in [33, 35–37], the optimized NCV display of the proposed PNM1 circuit is illustrated in Fig. 14.

Therefore, the total quantum cost of the proposed PNM1 block is 5. In addition, its logical calculation is $3\alpha+3\beta+3\delta$.

4.1.2 Proposed block, PNM2

The truth table of the proposed 4×4 parity-preserving reversible block is shown in Table 7. Each input vector is mapped individually to an output vector. The proposed reversible structure is called the PNM2 block.

The output equations of the PNM2 block can be determined as follows:

$$P(A,B,C,D) = AC' \oplus BC \quad (1)$$

$$Q(A,B,C,D) = (A \oplus B)' \quad (2)$$

$$R(A,B,C,D) = C' \quad (3)$$

$$S(A,B,C,D) = AC' \oplus BC \oplus D \quad (4)$$

The circuit representation of the PNM2 block is shown in Fig. 15.

As can be seen from Table 8,

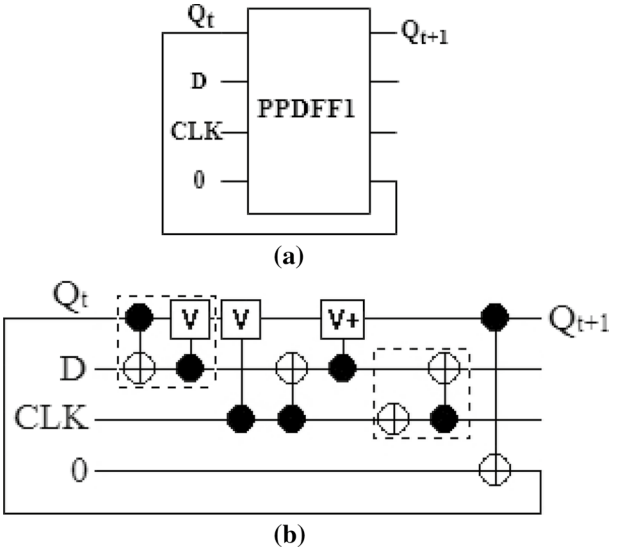


Fig. 19 Proposed parity-preserving reversible D flip-flop: **a** circuit view and **b** quantum realization

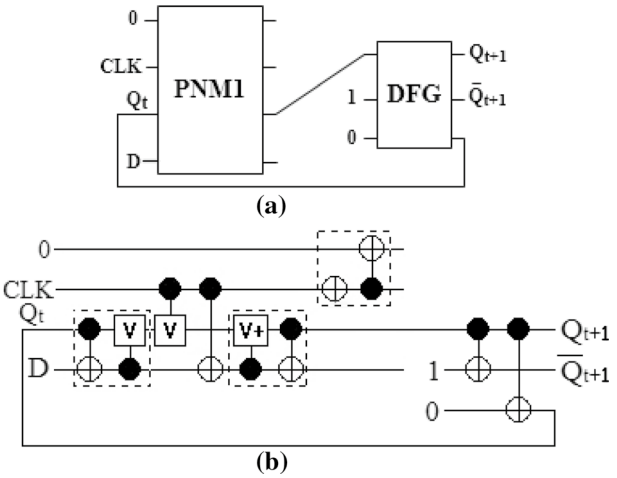


Fig. 20 Proposed parity-preserving reversible D flip-flop: **a** circuit view and **b** quantum realization

- Step 1 identifies TOF1 (Q, R) giving Step 2
- Step 2 identifies TOF2 (P, S) giving Step 3
- Step 3 identifies TOF3 (Q, R, P) giving Step 4
- Step 4 identifies TOF2 (P, Q).

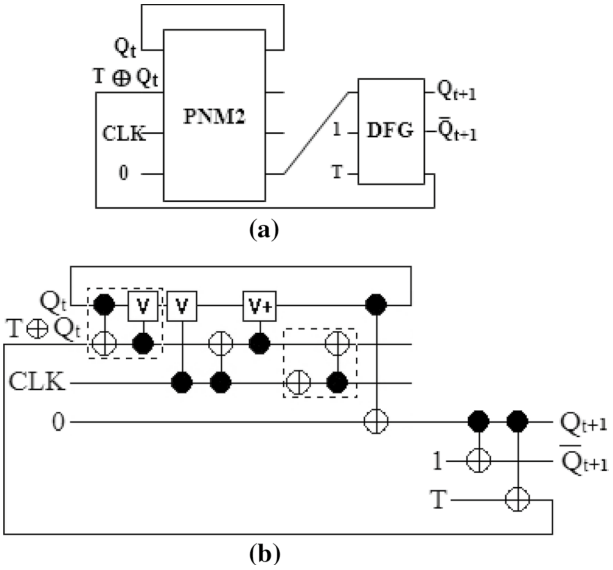


Fig. 21 The first proposed parity-preserving reversible T flip-flop: **a** circuit view and **b** quantum realization

It should be noted that the TOF gates are determined from the output side to the input side, respectively. The Toffoli-based circuit of the proposed PNM2 block is illustrated in Fig. 16.

Given that the quantum cost of the primitive gates 1×1 and 2×2 is one, then the initial quantum cost of the proposed PNM2 block is 9.

Moreover, according to Fig. 16, the NCV display of the proposed PNM1 block is shown in Fig. 17.

After simplifying the circuit shown in Fig. 17 according to the simplification rules in [33, 35–37], the optimized NCV display of the proposed PNM2 circuit is illustrated in Fig. 18.

Therefore, the total quantum cost of the proposed PNM2 block is 6. In addition, its logical calculation is $4\alpha + 2\beta + 2\delta$.

4.2 Proposed parity-preserving reversible flip-flops

In this section, using the proposed parity-preserving reversible blocks PNM1, PNM2 blocks and DFG gate various parity-preserving reversible flip-flops D, T and J-K are introduced.

The output equation of a D flip-flop with inputs D and CLK is expressed as $Q_{t+1} = Q_t.\overline{\text{CLK}} + \text{CLK.D}$. In Fig. 19, the first proposed parity-preserving reversible D flip-flop (PPDFF1) is illustrated using the PNM2 block.

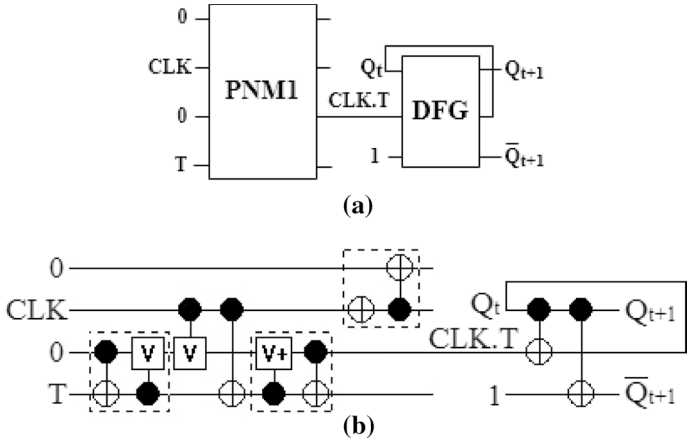


Fig. 22 The second proposed parity-preserving reversible T flip-flop: **a** circuit view and **b** quantum realization

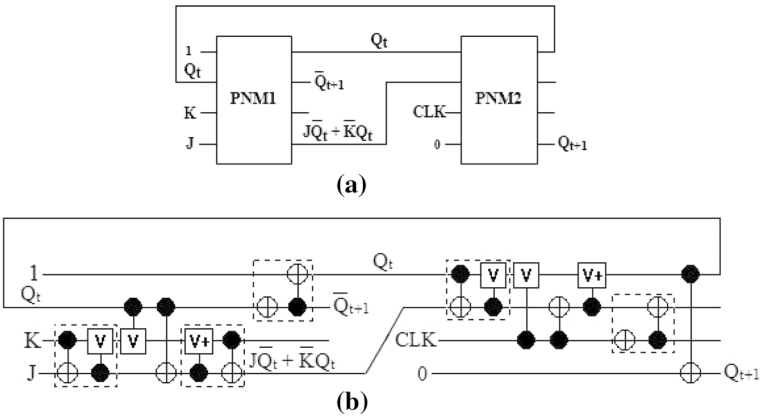


Fig. 23 The proposed parity-preserving reversible J-K flip-flop: **a** circuit view and **b** quantum realization

As seen in Fig. 19, the first proposed parity-preserving reversible D flip-flop has GC = 1, CI = 1 and GO = 2. Given that one parity-preserving reversible PNM2 block has been used in its design, so the quantum cost is calculated as follows:

$$QC_{PPDFF1} = 1QC_{PNM2} = (1 \times 6) = 6$$

The second parity-preserving reversible D flip-flop (PPDFF2) is shown in Fig. 20 using the proposed PNM1 block and DFG gate.

As seen in Fig. 20, the second proposed parity-preserving reversible D flip-flop has GC = 2, CI = 3 and GO = 3. Given that one parity-preserving reversible PNM1 block and one DFG gate have been used in its design, so the quantum cost is calculated as follows:

$$QC_{PPDFF2} = 1QC_{PNM1} + 1QC_{DFG} = (1 \times 5) + (1 \times 2) = 7$$

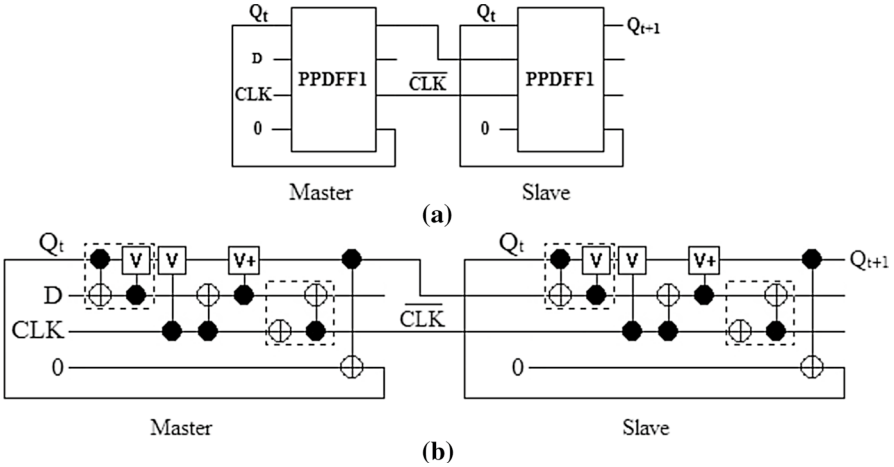


Fig. 24 The first proposed parity-preserving reversible master–slave D flip-flop: **a** circuit view and **b** quantum realization

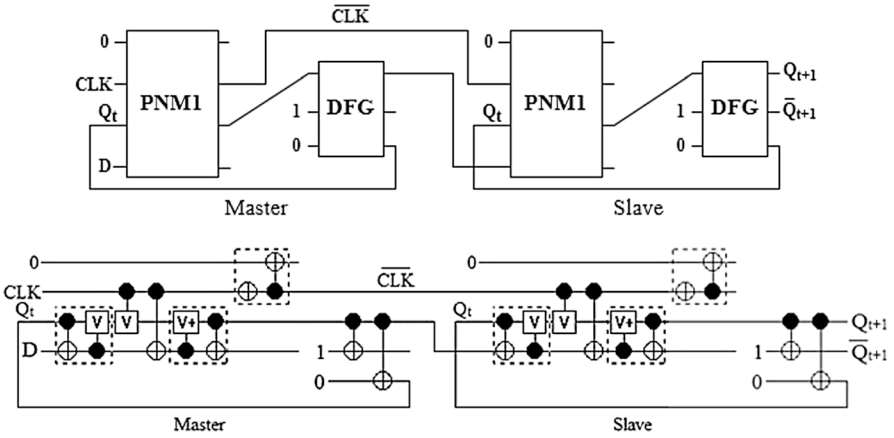


Fig. 25 The second proposed parity-preserving reversible master–slave D flip-flop flop: **a** circuit view and **b** quantum realization

The output equation of the T flip-flop with inputs T and CLK can be written as $Q_{t+1} = \mathrm{T}Q_t.\mathrm{CLK}Q_t.\overline{\mathrm{CLK}}$. Moreover, it can be easily demonstrated that the above equation is equal to $Q_{t+1} = (\mathrm{T.CLK})Q_t$.

In Fig. 21, the first proposed parity-preserving reversible T flip-flop (PPTFF1) is illustrated using the PNM2 block and DFG gate.

As seen in Fig. 21, the first proposed parity-preserving reversible T flip-flop has GC = 2, CI = 2 and GO = 2. Given that one parity-preserving reversible PNM2 block and one DFG gate have been used in its design, so the quantum cost is calculated as follows:

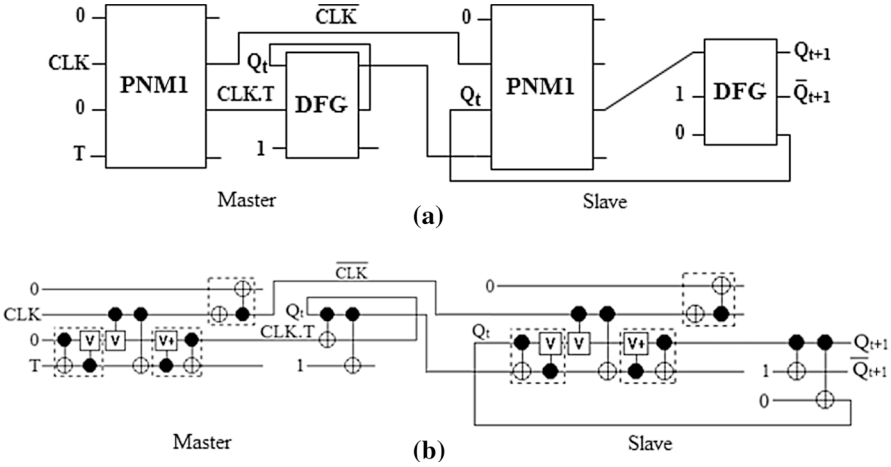


Fig. 26 The proposed parity-preserving reversible master–slave T flip-flop: **a** circuit view and **b** quantum realization

$$\mathrm{QC}_{\mathrm{PPTFF1}} = 1\mathrm{QC}_{\mathrm{PNM2}} + 1\mathrm{QC}_{\mathrm{DFG}} = (1 \times 6) + (1 \times 2) = 8$$

In Fig. 22, the second proposed parity-preserving reversible T flip-flop (PPTFF2) is illustrated using the PNM1 block and DFG gate.

As seen in Fig. 22, the second proposed parity-preserving reversible T flip-flop has GC = 2, CI = 3 and GO = 3. Given that one parity-preserving reversible PNM1 block and one DFG gate have been used in its design, so the quantum cost is calculated as follows:

$$\mathrm{QC}_{\mathrm{PPTFF2}} = 1\mathrm{QC}_{\mathrm{PNM1}} + 1\mathrm{QC}_{\mathrm{DFG}} = (1 \times 5) + (1 \times 2) = 7$$

The characteristic equation of J-K flip-flop is $Q_{t+1} = \overline{\mathrm{CLK}} Q_t + \mathrm{CLK}\left(J\bar{Q}t + \bar{K}Qt\right)$. The parity-preserving reversible J-K flip-flop is shown in Fig. 23 using the proposed reversible PNM1 and PNM2 blocks.

As seen in Fig. 23, the second proposed parity-preserving reversible J-K flip-flop has GC = 2, CI = 2 and GO = 3. Given that one PNM1 block and one PNM2 block have been used in its design, so the quantum cost is calculated as follows:

$$\mathrm{QC}_{\mathrm{PPJ\text{-}KFF}} = 1\mathrm{QC}_{\mathrm{PNM1}} + 1\mathrm{QC}_{\mathrm{PNM2}} = (1 \times 5) + (1 \times 6) = 11$$

In Fig. 24, the first proposed parity-preserving reversible master–slave D flip-flop is illustrated using the two parity-preserving reversible D Flip-flops (PPDFF1).

As seen in Fig. 24, the first proposed parity-preserving reversible master–slave D flip-flop has GC = 2, CI = 2 and GO = 3. Given that two parity-preserving reversible D flip-flops (PPDFF1) has been used in its design, so the quantum cost is calculated as follows:

$$\text{Quantum Cost} = 2\mathrm{QC}_{\mathrm{PPDFF1}} = (2 \times 6) = 12$$

In Fig. 25, the second proposed parity-preserving reversible master–slave D flip-flop is illustrated using the two parity-preserving reversible D flip-flops (PPDFF2).

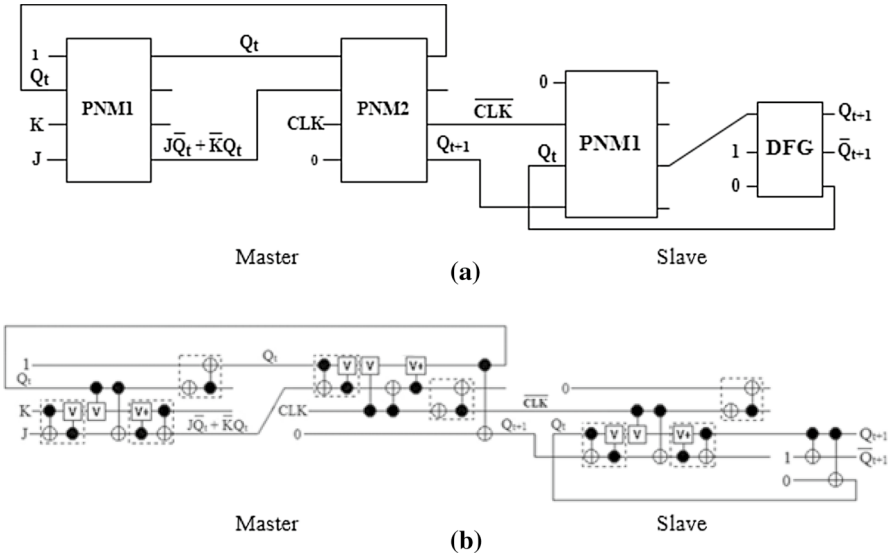


Fig. 27 The proposed parity-preserving reversible master–slave J-K flip-flop: **a** circuit view and **b** quantum realization

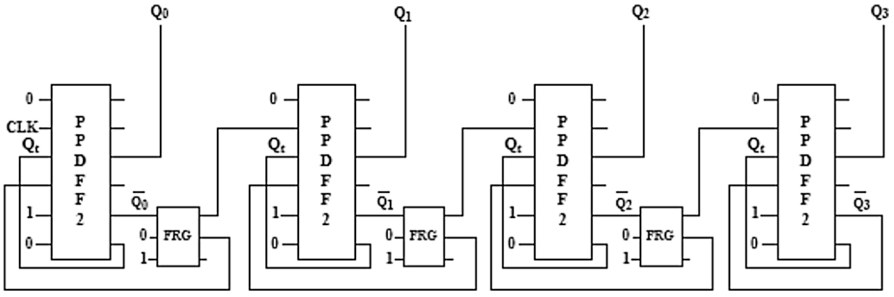
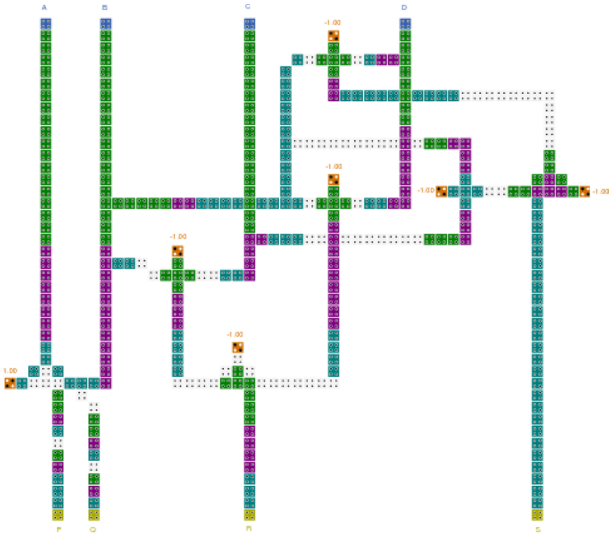


Fig. 28 The proposed parity-preserving reversible 4-bit asynchronous up-counter

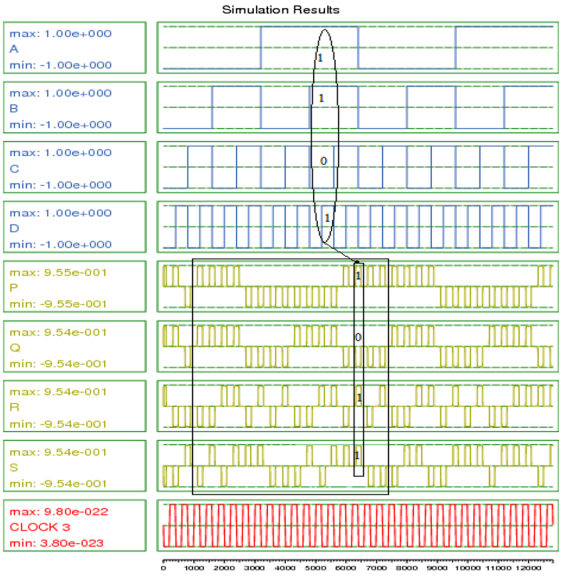
As seen in Fig. 25, the second proposed parity-preserving reversible master–slave D flip-flop has GC = 4, CI = 6 and GO = 6. Given that two parity-preserving reversible D flip-flops (PPDFF2) have been used in its design, so the quantum cost is calculated as follows:

$$\text{Quantum Cost} = 2\text{QC}_{\text{PPDFF2}} = (2 \times 7) = 14$$

In Fig. 26, the proposed parity-preserving reversible master–slave T flip-flop is illustrated using the one parity-preserving reversible T flip-flop (PPTFF2) and one parity-preserving reversible D flip-flop (PPDFF2).



(a)

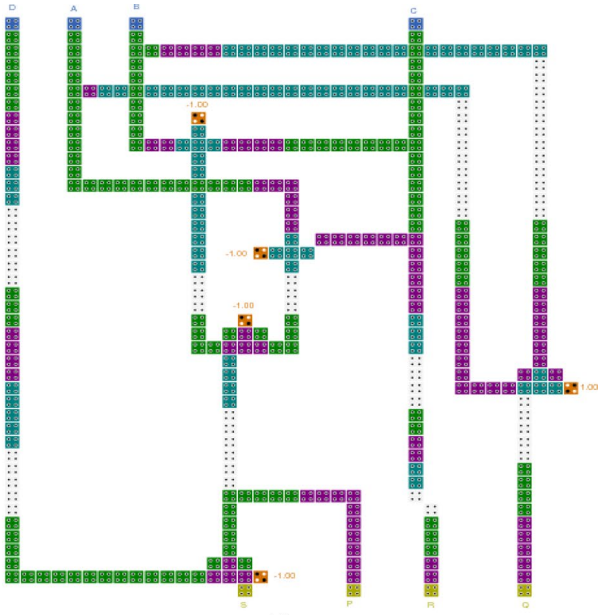


(b)

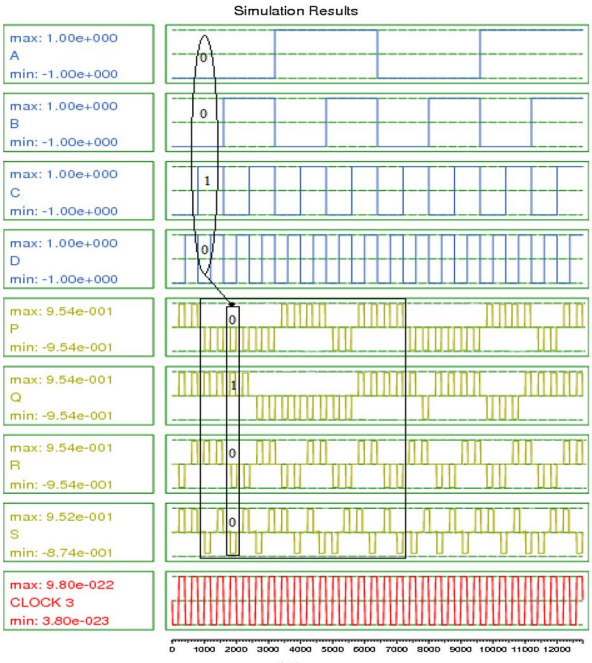
Fig. 29 The QCA implementation of the proposed reversible blocks: **a** QCA layout of the PNM1 block, **b** simulation results of the PNM1 block, **c** QCA layout of the PNM2 block and **d** simulation results of the PNM2 block

As seen in Fig. 26, the proposed parity-preserving reversible master–slave T flip-flop has GC = 4, CI = 6 and GO = 6. Given that one parity-preserving reversible T flip-flop (PPTFF2) and one parity-preserving reversible D flip-flop (PPDFF2) have been used in its design, so the quantum cost is calculated as follows:

$$\text{Quantum Cost} = 1\text{QC}_{\text{PPTFF2}} + 1\text{QC}_{\text{PPDFFF2}} = (1 \times 7) + (1 \times 7) = 14$$



(c)



(d)

Fig. 29 (continued)

Table 9 The energy consumption analysis of the QCA reversible gates

Circuits	Avg. leakage energy diss (meV)			Avg. switching energy diss (meV)			Total energy diss (meV)		
	0.5 E_K	1 E_K	1.5 E_K	0.5 E_K	1 E_K	1.5 E_K	0.5 E_K	1 E_K	1.5 E_K
Proposed QCA reversible PNM1 block	100.25	301.57	599.35	611.71	519.69	421.15	711.96	821.26	1020.5
Proposed QCA reversible PNM2 block	105.46	333.26	606.10	624.61	538.28	453.59	730.07	871.54	1059.38

In Fig. 27, the proposed parity-preserving reversible master–slave J-K flip-flop is illustrated using the one parity-preserving J-K flip-flop (PPJ-KFF) and one parity-preserving reversible D flip-flop (PPDFF2).

As seen in Fig. 27, the proposed parity-preserving reversible master–slave J-K flip-flop has GC = 4, CI = 5, and GO = 6. Given that one parity-preserving J-K flip-flop (PPJ-KFF) and one parity-preserving reversible D flip-flop (PPDFF2) have been used in its design, so the quantum cost is calculated as follows:

$$\text{Quantum Cost} = 1\text{QC}_{\text{PPJ-KFF}} + 1\text{QC}_{\text{PPDFF2}} = (1 \times 11) + (1 \times 7) = 18$$

In Fig. 28, the proposed parity-preserving reversible 4-bit asynchronous up-counter (PPUPC) is illustrated using the four proposed parity-preserving reversible D flip-flops (PPDFF2) and three FRG gates.

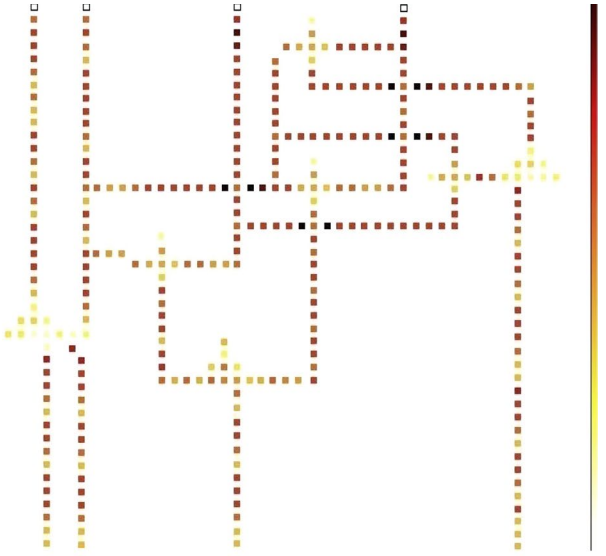
As seen in Fig. 28, the proposed parity-preserving reversible 4-bit asynchronous up-counter has GC = 11, CI = 18 and GO = 15. Given that four parity-preserving reversible D flip-flops (PPDFF1) flip-flops and three FRG gates have been used in its design, so the quantum cost is calculated as follows:

$$\text{Quantum Cost} = 4\text{QC}_{\text{PPDFF2}} + 3\text{QC}_{\text{FRG}} = (4 \times 7) + (3 \times 5) = 43$$

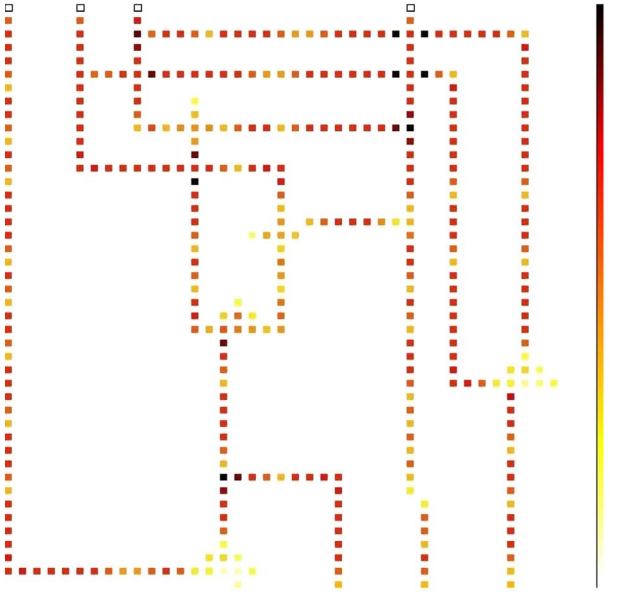
5 Simulation results and comparisons

In this section, we implement the proposed reversible blocks in QCA technology by QCADesigner 2.0.3 software [54]. As observed, the proposed reversible blocks consist of 2-input AND, 2-input XOR and 2-input XNOR gates. To achieve effective quantum-dot cellular automata [55–59] implementation of the proposed blocks, we have used 2-input XOR presented in [60]. The QCA layouts, along with the simulation results of the proposed reversible blocks, are illustrated in Fig. 29.

As seen in Fig. 29, the proposed QCA layouts are coplanar and consist of simple cells so that crossing of the wires is carried out using the technique introduced



(a)



(b)

Fig. 30 Energy dissipation map at 2 K and tunneling energy of 0.5 EK for **a** the proposed QCA reversible PNM1 block and **b** the proposed QCA reversible PNM2 block

Table 10 Comparative characteristics of the parity-preserving reversible D flip-flop designs **a** with output Q and **b** outputs Q and $\bar{Q}$

Designs	GC	CI	GO	QC	LC	Ratio
(a)						
Haghparast and Navi [51]	2	1	2	7	$4\alpha+4\beta+1\delta$	1.16
Pareek et al. [40]	1	1	2	7	$3\alpha+2\beta+1\delta$	1.16
Proposed PPDFF1	1	1	2	6	$4\alpha+2\beta+2\delta$	1
(b)						
Misra et al. [26]	2	3	3	8	$6\alpha+2\beta+1\delta$	1.14
Thapliyal and Ranganathan [50]	2	2	2	10	$4\alpha+8\beta+2\delta$	1.42
Gharajeh and Haghparast [41]	1	2	3	10	$8\alpha+16\beta+8\delta$	1.42
Pareek [52]	2	3	3	9	$5\alpha+3\beta+1\delta$	1.28
Goswami et al. [53]	2	3	2	19	$18\alpha+4\beta+1\delta$	2.71
Proposed PPDFF2	2	3	3	7	$5\alpha+3\beta+3\delta$	1

Table 11 Comparative characteristics of the parity-preserving reversible T flip-flop designs with outputs Q and $\bar{Q}$

Designs	GC	CI	GO	QC	LC	Ratio
Pareek [52]	2	2	2	9	$5\alpha+2\beta+1\delta$	1.28
Thapliyal and Ranganathan [50]	3	3	3	15	$6\alpha+12\beta+3\delta$	2.14
Misra et al. [26]	2	2	2	8	$6\alpha+2\beta+1\delta$	1.14
Thapliyal and Srinivas [49]	8	11	11	40	$16\alpha+32\beta+8\delta$	5.71
Proposed PPTFF1	2	2	2	8	$6\alpha+2\beta+2\delta$	1.14
Proposed PPTFF2	2	3	3	7	$5\alpha+3\beta+3\delta$	1

Table 12 Comparative characteristics of different parity-preserving reversible J-K flip-flop designs with outputs Q and $\bar{Q}$

Designs	GC	CI	GO	QC	LC	Ratio
Pareek [52]	4	5	6	19	$9\alpha+10\beta+3\delta$	1.72
Thapliyal and Ranganathan [50]	4	4	5	20	$8\alpha+16\beta+4\delta$	1.81
Thapliyal and Srinivas [49]	7	9	10	35	$14\alpha+28\beta+7\delta$	3.18
Proposed PPJ-KFF1	2	2	3	11	$7\alpha+5\beta+5\delta$	1

by Abedi et al. [61]. The QCA layout of the PNM1 block has 345 cells with occupied area 0.82 μm^2 and a delay equal to 2.75 clock cycles. Also, the QCA layout of the PNM2 block has 353 cells with occupied area 0.63 μm^2 and a delay equal to 2.5 clock cycles.

In order to compute the energy consumption of the QCA reversible blocks, we have used the QCAPRO tool [62]. The results of the energy consumption analysis of the proposed structures at three different levels of energy (0.5 E_K, 1 E_K and 1.5 E_K) are provided in Table 9.

Table 13 Comparative characteristics of different parity-preserving reversible master–slave D flip-flop designs **a** with output Q and **b** outputs Q and $\bar{Q}$

Designs	GC	CI	GO	QC	LC	Ratio
(a)						
Pareek [52]	2	2	3	14	$6\alpha+4\beta+2\delta$	1.16
Proposed#1	2	2	3	12	$8\alpha+4\beta+4\delta$	1
(b)						
Thapliyal and Srinivas [49]	5	6	6	25	$10\alpha+20\beta+5\delta$	1.78
Goswami et al. [53]	4	5	4	38	$36\alpha+8\beta+2\delta$	2.71
Proposed#2	4	6	6	14	$10\alpha+6\beta+6\delta$	1

Table 14 Comparative characteristics of two parity-preserving reversible master–slave T flip-flop designs with outputs Q and $\bar{Q}$

Designs	GC	CI	GO	QC	LC	Ratio
Thapliyal and Srinivas [49]	23	32	35	115	$46\alpha+92\beta+23\delta$	8.21
Proposed	4	6	6	14	$10\alpha+6\beta+6\delta$	1

Table 15 Comparative characteristics of two parity-preserving reversible master–slave J-K flip-flop designs with outputs Q and $\bar{Q}$

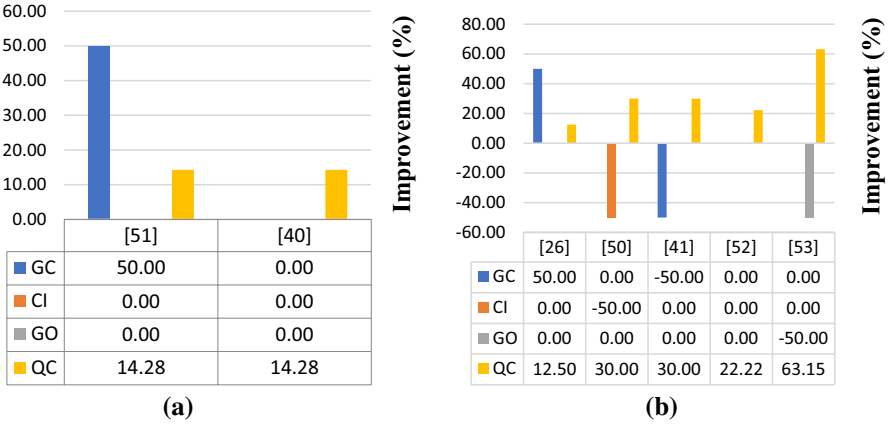
Designs	GC	CI	GO	QC	LC	Ratio
Thapliyal and Srinivas [49]	22	30	32	110	$44\alpha+88\beta+22\delta$	6.11
Proposed	4	5	6	18	$12\alpha+8\beta+8\delta$	1

Table 16 Characteristics of the parity-preserving reversible 4-bit asynchronous up-counter design

Design	GC	CI	GO	QC
Proposed	11	18	15	43

Besides, energy dissipation maps of the proposed designs with tunneling energy of 0.5 E_K are illustrated in Fig. 30. The cells with higher power dissipation are depicted with darker colors in the thermal hot spot maps.

In the following, the performance analyses of the proposed parity-preserving reversible designs concerning the existing designs are provided. Tables 10, 11, 12, 13, 14, 15 and 16 give the characteristics of the proposed flip-flops circuits along with the previous designs in terms of GC, CI, GO, QC, LC and ratio



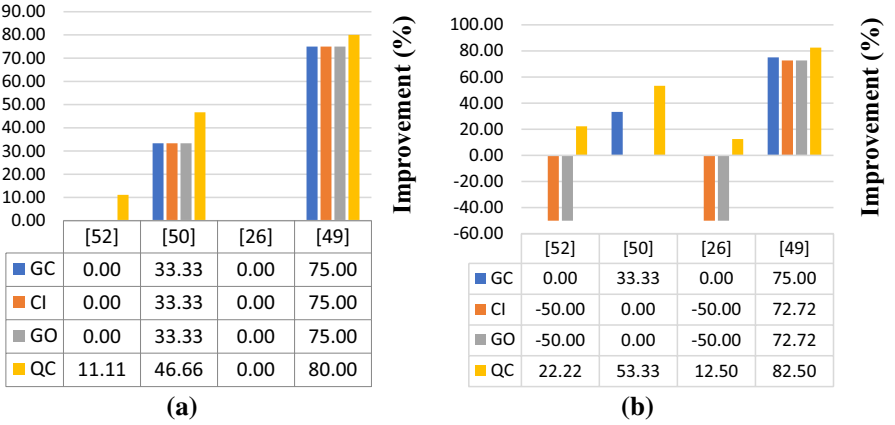
	[51]	[40]
GC	50.00	0.00
CI	0.00	0.00
GO	0.00	0.00
QC	14.28	14.28

(a)

	[26]	[50]	[41]	[52]	[53]
GC	50.00	0.00	-50.00	0.00	0.00
CI	0.00	-50.00	0.00	0.00	0.00
GO	0.00	0.00	0.00	0.00	-50.00
QC	12.50	30.00	30.00	22.22	63.15

(b)

Fig. 31 Improvement of the proposed parity-preserving reversible D flip-flop compared to other designs **a** with output Q and **b** with outputs Q and $\bar{Q}$



	[52]	[50]	[26]	[49]
GC	0.00	33.33	0.00	75.00
CI	0.00	33.33	0.00	75.00
GO	0.00	33.33	0.00	75.00
QC	11.11	46.66	0.00	80.00

(a)

	[52]	[50]	[26]	[49]
GC	0.00	33.33	0.00	75.00
CI	-50.00	0.00	-50.00	72.72
GO	-50.00	0.00	-50.00	72.72
QC	22.22	53.33	12.50	82.50

(b)

Fig. 32 Improvement of the proposed parity-preserving reversible T flip-flop compared to other designs **a** PPTFF1 and **b** PPTFF2

criteria. The ratio criterion denoted the ratio of quantum cost of each existing design in comparison with the quantum cost of the proposed design.

As shown in Table 10a, the quantum cost of the proposed PPDFF1, compared with the best previous design in [51] and [40], shows an improvement of 14.28%. Also, its GC, CI and GO criteria are equal or better to all of the previous designs. Also, as shown in Table 10b, the quantum cost of the proposed PPDFF2, compared with the best previous design in [26], shows an improvement of 12.50%. Besides, its GC, CI and GO criteria are very close to than all of previous designs.

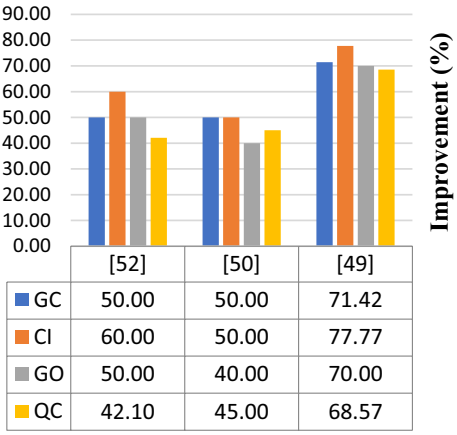


Fig. 33 Improvement of the proposed parity-preserving reversible J-K flip-flop compared to other designs

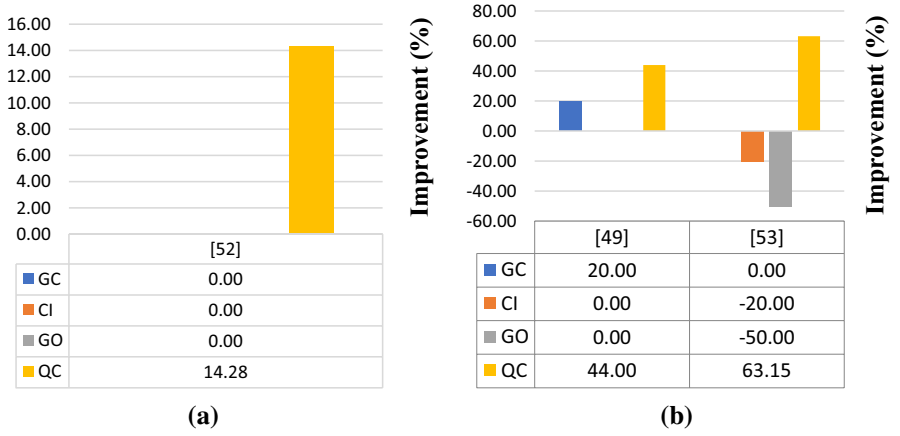


Fig. 34 Improvement of the proposed parity-preserving reversible master-salve D flip-flop compared to other designs **a** with output Q and **b** outputs Q and $\bar{Q}$

Moreover, the improvement percentage of the proposed parity-preserving reversible PPDFF1 and PPDFF2 is shown in Fig. 31.

As shown in Table 11, the quantum cost of the proposed PPTFF2, compared with the best previous design in [26], shows an improvement of 12.50%. In addition, its GC, CI and GO criteria are smaller or equal to all of previous designs. In addition, the improvement percentage of the proposed parity-preserving reversible PPTFF1 and PPTFF2 is shown in Fig. 32.

As shown in Table 12, the quantum cost of the proposed PPJ-KFF1, compared with the best previous design in [52], shows an improvement of 42.10%. Also, its GC, CI and GO criteria are so better than all of the previous designs.

Besides, the improvement percentage of the proposed parity-preserving reversible PPJ-KFF1 is shown in Fig. 33.

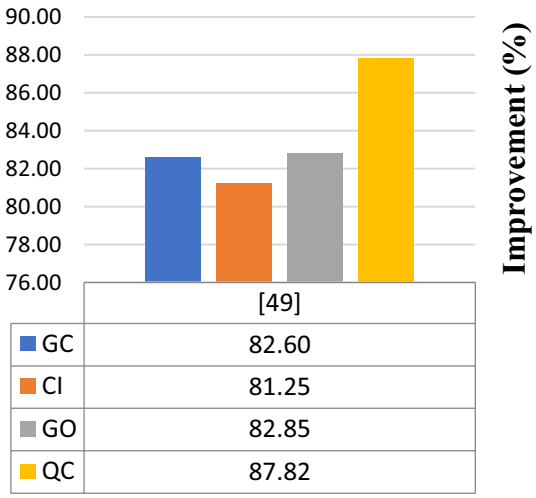


Fig. 35 Improvement of the proposed parity-preserving reversible master–slave T flip-flop compared to the other designs

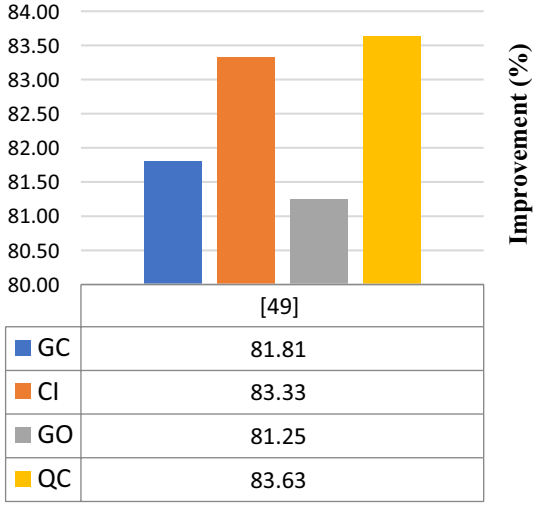


Fig. 36 Improvement of the proposed parity-preserving reversible J-K flip-flop compared to other designs

As shown in Table 13a, the quantum cost of the parity-preserving master–slave Proposed#1, compared with the best previous design in [52], shows an improvement of 14.28%. In addition, its GC, CI and GO criteria are equal to all of the previous designs. Also, as shown in Table 13b, the quantum cost of the parity-preserving master–slave Proposed#2, compared with the best previous design in [49] shows an improvement of 44%. Besides, its GC, CI and GO criteria are very close to all of the previous designs.

In addition, the improvement percentage of the proposed parity-preserving reversible master–slave D flip-flop is shown in Fig. 34.

Also, as shown in Table 14, the quantum cost of the proposed parity-preserving master–slave T flip-flop, compared with the best previous design in [49], shows

an improvement of 87.82%. In addition, its GC, CI and GO criteria are smaller than all of the previous designs. Besides, the improvement percentage of the proposed parity-preserving reversible master–slave T flip-flop is shown in Fig. 35.

Also, as shown in Table 15, the quantum cost of the proposed parity-preserving master–slave J-K flip-flop, compared with the best previous design in [49], shows an improvement of 83.63%. In addition, its GC, CI and GO criteria are smaller than all of the previous designs. Besides, the improvement percentage of the proposed parity-preserving reversible master–slave J-K is shown in Fig. 36.

6 Conclusion

In this paper, initially two novel parity-preserving reversible blocks were introduced. Then, effective designs of parity-preserving reversible D, T and J-K flip-flops, as well as their master–slave, were proposed using the proposed blocks and DFG gates. Finally, a parity-preserving reversible 4-bit asynchronous up-counter was designed using the proposed parity-preserving reversible D flip-flops and three FRG gates. The proposed circuits are compared with the existing counterparts in terms of constant inputs, garbage outputs and quantum cost. The comparison results show that the proposed designs are superior to the quantum cost and some of the other criteria, such as constant input and garbage outputs. Utilizing the proposed flip-flops designs in the parity-preserving reversible sequential circuits such as registers, BCD counters and RAM minimizes the quantum cost criteria. All the scales are in the nanometric area.

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