The Journal of Supercomputing (2018) 74:4696–4716
https://doi.org/10.1007/s11227-018-2464-9

A novel fault-tolerant multiplexer in quantum-dot cellular automata technology

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Published online: 25 June 2018

Abstract

Quantum-dot cellular automaton (QCA) has emerged as one of the best alternatives to CMOS technology in nanoscale. In spite of the potential advantages of QCA technology over CMOS, QCA circuits often suffer from various types of manufacturing defects and are therefore prone to fault. Hence, the design of fault-tolerant circuits in QCA technology is considered a necessity. The implementation of multiplexer circuits in QCA technology has been of great interest to researchers due to its widespread use in memory circuits and ALUs. In most of the multiplexer circuits presented in QCA, the problem of fault-tolerant is ignored. In this paper, a novel fault-tolerant three-input majority gate is initially proposed. The proposed structure has been investigated against all kinds of cell omission, extra cell deposition, and cell displacement defects. The simulation results are verified by QCA Designer 2.0.3, and it showed that it is 100, 84.98, and 100% tolerant to single-cell omission, double-cell omission, and extra cell deposition, respectively. In addition, the proposed structure shows that it is robust against cell displacement defects. Moreover, physical investigations are provided in order to confirm the function of the proposed fault-tolerant structure. Finally, using the proposed structure, a novel single-layer 2:1 multiplexer is presented. The results of comparisons indicate that the proposed designs are more reliable than the existing designs. Furthermore, QCAPro power estimator tool is employed to estimate the energy dissipation of the proposed structure.

Keywords Circuit design · Nanotechnology · Quantum-dot cellular automata (QCA) · Majority gate · Fault-tolerant · Multiplexer

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1 Introduction

Within a short time, it is expected that CMOS technology will reach the end of its way due to limitations such as physical scalability, short channel effects, and high cost of lithography as well as heating and cooling challenges [1–3]. Therefore, emerging technologies such as single-electron transistor (SET), resonant tuning diode (RTD), carbon nanotube field effect transistor (CNTFET), and QCA have been able to overcome these problems. Based on the International Technology Roadmap for Semiconductor (ITRS), which offers a summary of future technologies, QCA has been introduced as one of the effective strategies. This technology is one of the options for designing high-density logic circuits due to its unique features such as high speed, small size, and low power consumption. The simplest element in QCA technology is a square structure in nanoscale that includes four quantum dots and two electrons. The electrons are able to tunnel between quantum dots if potential barrier that discriminates quantum dots is low [3–5]. According to Coulomb repulsion, electrons located two opposite corners of the QCA cell [3–5].

Although extensive research has so far been carried out to design and simulate various digital circuits such as basic logic gates, adders [6–13], multipliers [14–18], dividers [16, 19–21], and memory circuits [22–26] in QCA technology, due to the novelty of this technology, there are still many serious barriers that have not been sufficiently studied. One of the major barriers is the lack of mature QCA technology in the commercial production of circuits, which suffer from a high rate of defects [27]. The available defects in the manufacturing process may occur in the chemical synthesis and the deposition phases [27]. Cell misplacement defects occur during the deposition phase, which is among the most common defects [27]. The cell misplacement defects include cell omission, deposition of extra cells, and cell displacement [27, 28]. Occurrence of such defects in QCA logic devices causes a dramatic reduction in efficiency [28]. Therefore, the design of fault-tolerant logic circuits in QCA technology is absolutely necessary, and that is why in the last decade, QCA researchers have focused on designing fault-tolerant circuits. Since the inverter and majority gates are two basic gates designed for QCA circuits, their durable configurations can lead to the design of robust logic circuits for QCA technology. So far, several fault-tolerant circuits have been proposed. Lent et al. [3] have provided the conventional three-input majority gate that is only 20% fault-tolerant for a single-cell omission defect. In 2007, Huang et al. introduced a new fault-tolerant three-input majority gate called the orthogonal tile, which has 13 cells and occupies 0.01 μm^2. It has 66.7 and 36.1% fault-tolerant against single- and double-cell omission defects, respectively [29]. In 2014, Sen et al. [30] presented a fault-tolerant three-input majority gate that achieved 95.65 and 78% fault-tolerant against single- and double-cell omission defects. It also consists of 27 cells and occupies 0.02 μm^2. In 2016, Sen et al. suggested another three-input majority gate that is 75 and 42% robust against single- and double-cell omission defects. It has 12 cells with an area of 0.01 μm^2 [31]. In addition, in 2016, Sen et al. [32] provided a novel fault-tolerant three-input majority gate that is 97.44 and 82.86% fault-tolerant against the single- and double-cell omission defects. They used cellular rotation in their design. This structure has 43 cells, and its occupied area is equal to 0.04 μm^2. In 2016, Kumar et al. suggested a fault-tolerant three-input majority

gate, which used two clocks. This has 87.5 and 60% fault-tolerant against single- and double-cell omission defects [9]. It includes 20 cells that occupy 0.01 μm^2. In 2016, Du et al. [33] introduced a fault-tolerant three-input majority gate that used 5×3 tiles and has 60 and 31% fault-tolerant against single- and double-cell omission defects. This structure has 20 cells with an area of 0.01 μm^2. In 2018, Sun et al. [34] proposed new three-input majority gate with 25 cells which covers an area of 0.01 μm^2. This structure is 80.95 and 39.8% fault-tolerant to single- and double-cell omission defects. In 2018, Wang et al. [35] introduced a new three-input majority gate with 36 cells, which occupies an area of 0.03 μm^2. This structure is 93.8% and 66.7 fault-tolerant against single- and double-cell omission defects. In 2018, Farazkish [36] suggested another fault-tolerant three-input majority gate with 13 cells, which covers an area of 0.01 μm^2. This structure is 66.6 and 22.2% fault-tolerant to single- and double-cell omission defects.

The major contribution of this research can be summarized as followed:

This paper proposes a novel fault-tolerant three-input majority gate with 27 cells, which covers an area of 0.02 μm^2.

- The proposed structure is 100, 84.98, and 100% fault-tolerant against single-cell omission, double-cell omission, and extra cell deposition defects.
- A novel single-layer fault-tolerant 2:1 multiplexer using the proposed structure is introduced.
- Physical investigations are used to confirm the proposed structure.
- The simulations were performed using the QCADesigner 2.0.03 and QCAPro tools to measure performance and energy consumption.

The rest of the paper is organized as follows: In Sect. 2, an overview of QCA technology is given in terms of cells, basic gates, wire crossing, clocking, and characteristic defects of QCA. In Sect. 3, the proposed fault-tolerant majority gate is introduced. The proposed fault-tolerant QCA multiplexer is described in Sect. 4. The simulation results of the proposed circuits are provided in Sect. 5. Finally, the paper ends with conclusion section.

2 Preliminaries

2.1 QCA review

The emerging technology of QCA is suitable for designing circuits at the nanoscale [5]. The basic computing element in QCA technology is a quantum cell. Each quantum cell consists of four quantum dots, which are located in the four corners of a square. Each cell contains two electrons, which can tunnel among these dots. As it is seen in Fig. 1, regarding Coulomb's repulsion force, two stable arrangements of $P = +1$ and $P = -1$ are formed, which encode 1 and 0 in binary logic, respectively [3, 5, 37].

Wires in QCA technology are created using a sequence of QCA cells, which are able to propagate inputted signal to output. Figure 2 shows 90° and 45° wires in QCA technology. As you can see, in the 90° wire, the inputted signal is transferred to the

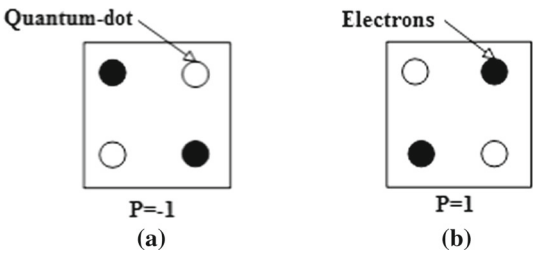


Fig. 1 QCA cell **a** zero binary value and **b** one binary value

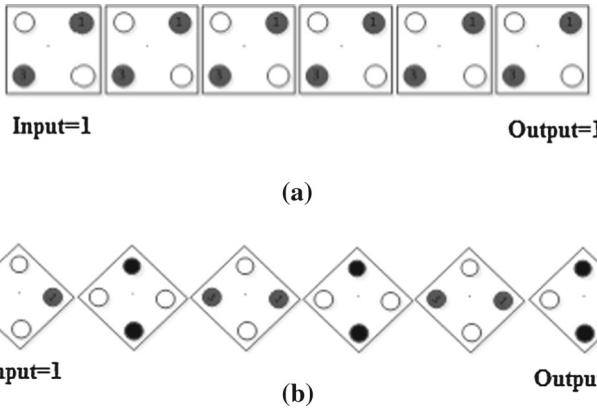


Fig. 2 QCA wires **a** 90° wire and **b** 45° wire (inverter chain)

output without change, while in the 45° wire, the inputted signal or its complement can be generated at the output.

Three-input majority gate (MV3) and inverter gate (NOT) are considered as two building blocks of the QCA circuit [5]. The MV3 gate output with inputs A, B, and C is defined using Eq. (1):

$$\mathrm{MV3}\,(A,\ B,\ C) = AB + AC + BC \tag{1}$$

Moreover, Fig. 3 shows the circuit and cellular representation of MV3 (A, B, C) gate.

It should be noted that by simply keeping one of the inputs of MV3 gate constant at '0' or '1,' we can obtain two-input AND or two-input OR gates, respectively.

Another basic gate is inverter gate. Circuit representation and two different layouts of QCA NOT gate are depicted in Fig. 4.

QCA circuits such as CMOS circuits require clock pulses in order to function correctly. The clock pulse in QCA technology follows two main goals: providing energy to circuit devices and controlling data propagation in the cells. Clock pulses facilitate the movement of electrons inside cells and thus allow the electrons to change their configuration in a predefined manner and change the barriers of tunneling between quantum dots [5]. Usually, a clocking design consists of four phases—switch, hold, release, and relaxation, as shown in Fig. 5.

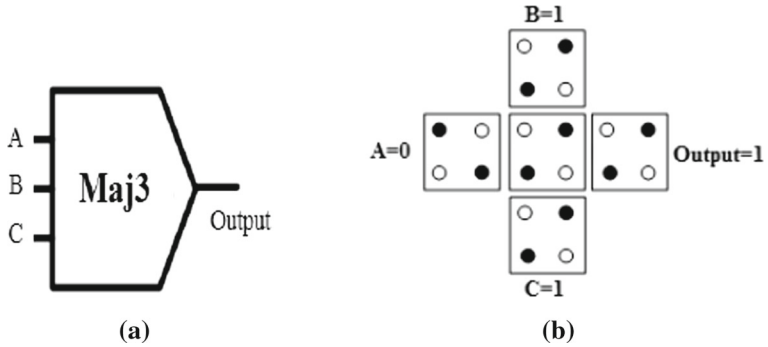


Fig. 3 The MV3 (*A*, *B*, *C*) **a** circuit representation and **b** cellular representation

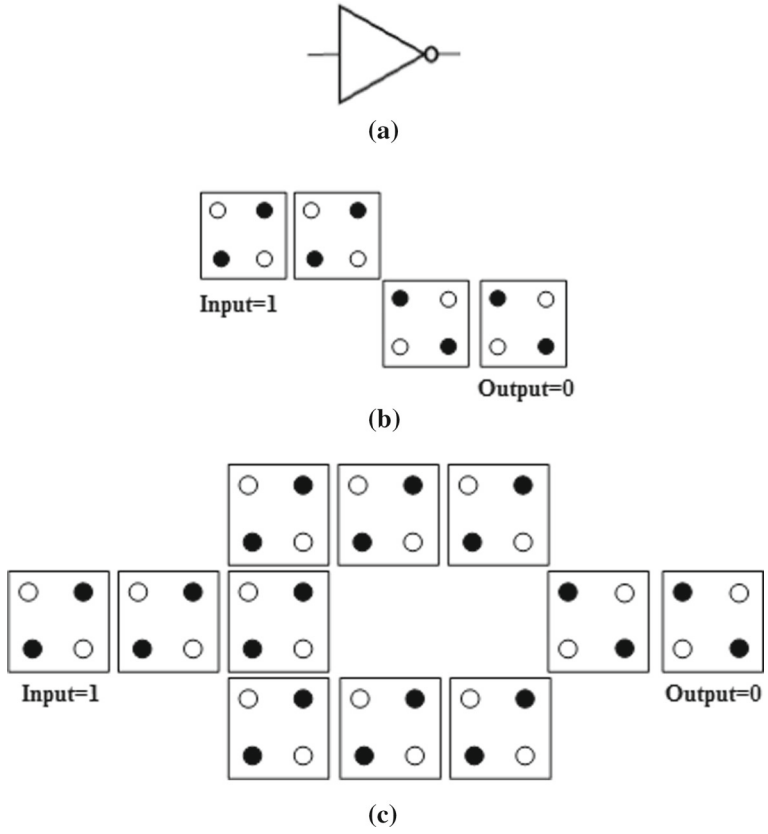


Fig. 4 Inverter gate **a** circuit representation, **b** common cellular representation, and **c** robust cellular representation

The process of cell polarization starts at the switch phase (ascending edge) and continues until the cell is completely polarized. When the clock pulse reaches the high level (hold phase), the cell retains its polarization. A decrease in polarization of

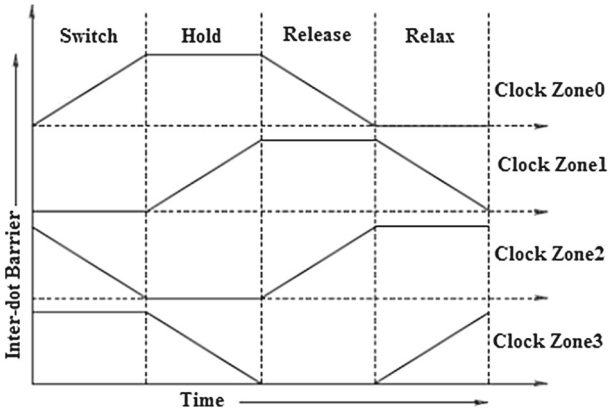


Fig. 5 Clock pulse in QCA technology

the cell occurs when the clock passes through the release phase (descending edge). Finally, at the relax phase, the cell is unpolarized [38].

2.2 Kink energy

The electrostatic energy between two electrons i and j is calculated using Eq. 2 as follows:

$$E_{ij} = K\frac{q_i q_j}{r_{ij}}(\mathrm{J}), \tag{2}$$

where E_{ij} is kink energy, K is a constant value, q_i and q_j are electrical charges, and r_{ij} is the distance between two electrical charges of i and j. By substituting values of $K = 9 \times 10^9$ and $q = 1.6 \times 10^{-38}$, kink energy between two electrons is obtained equal to $E_{ij} = 23.04 \times 10^{-29}$(J) [39–41]. The final electrostatic energy applied to q_i electron is calculated by Eq. 3:

$$U_{T_i} = \sum_{j=1}^{N} E_{ij}, \tag{3}$$

where N is the number of electrical charges.

2.3 Defects in QCA

Generally, the defects in QCA technology occur in the deposition process. These defects are basically divided into four categories as follows [42]:

1. *Cell omission* This type of defect occurs due to omission of one cell (Fig. 6a).
2. *Cell displacement* This type of defect occurs due to displacement of cells from their original position (Fig. 6b).

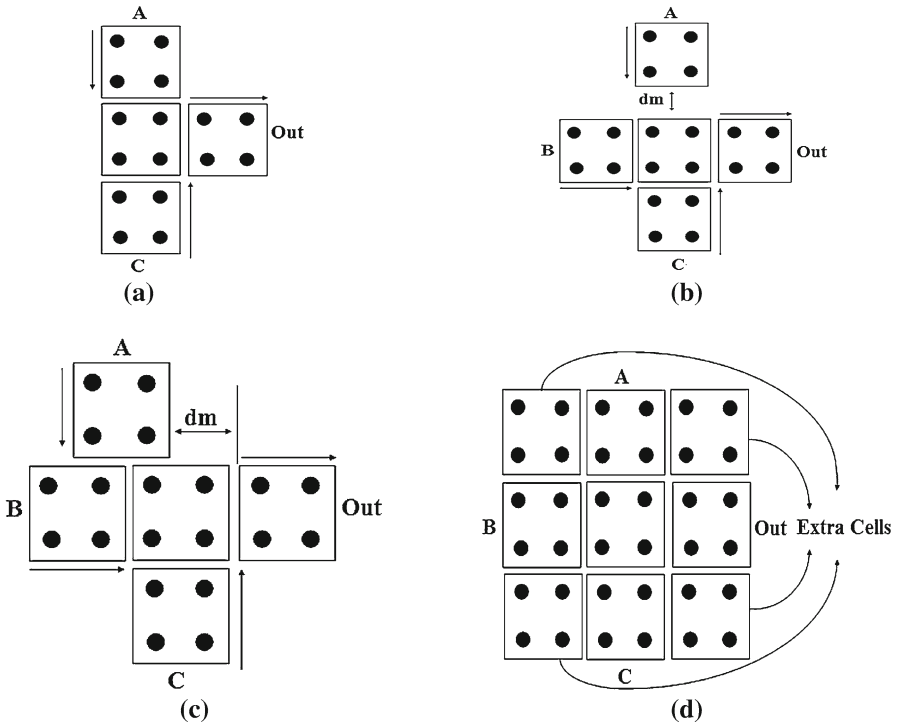


Fig. 6 Various types of defects in QCA technology **a** cell omission defects, **b** cell displacement defects, **c** cell misalignment defects, and **d** extra cell deposition

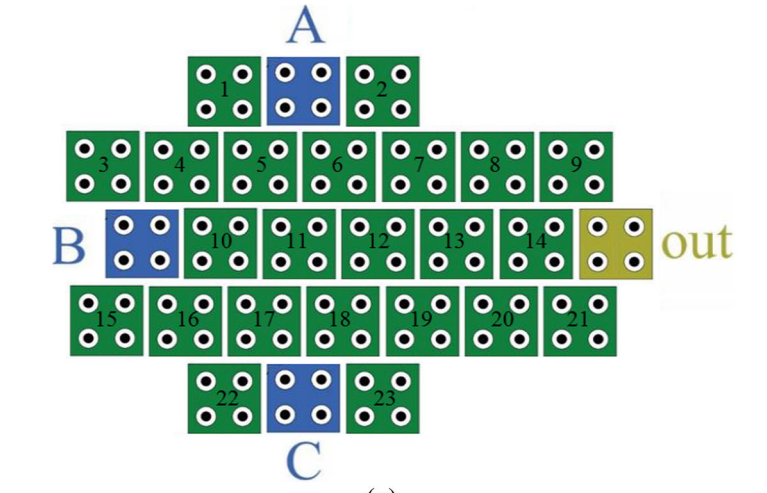
3. *Cell misalignment* This type of defect occurs due to misalignment of cells (Fig. 6c).
4. *Extra cell deposition* It occurs due to deposition of cells in the bed (Fig. 6d).

3 Proposed fault-tolerant majority gate

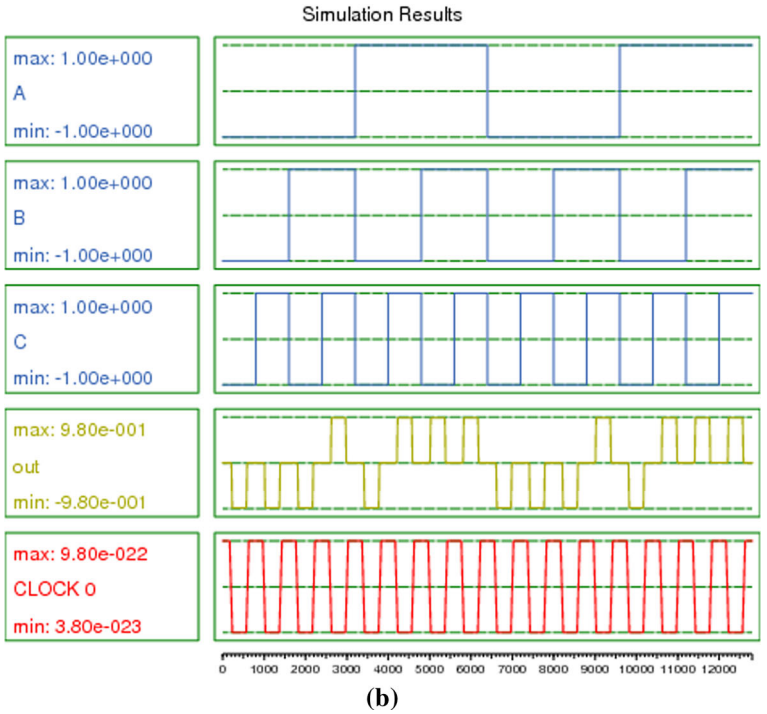
As mentioned above, the majority gate is applied as one of the most important building blocks of QCA circuits. Using common majority gate in the design of circuits reduces the fault-tolerant potential. As outlined in the introduction section, several fault-tolerant majority gates have been proposed so that their application in the design of circuits can increase the tolerability of the defects. In the following section, a novel fault-tolerant three-input majority gate has been presented and its function is investigated through some physical proofs and computer simulations.

The proposed gate consists of normal cells, not rotated cells. Cellular representation of the proposed gate is depicted in Fig. 7. As it can be seen, the cells of the sequential rows in the proposed design have 10 nm displacements with respect to each other.

As it can be seen in Fig. 7, the proposed fault-tolerant structure has 27 cells and is able to produce the output in one-clock phase.



(a)



(b)

Fig. 7 The proposed fault-tolerant majority gate **a** cellular view and **b** simulation results

3.1 Physical verification

In this section, we will show the correctness of the output of the proposed fault-tolerant structure with a single-cell omission defect through physical proofs. Since

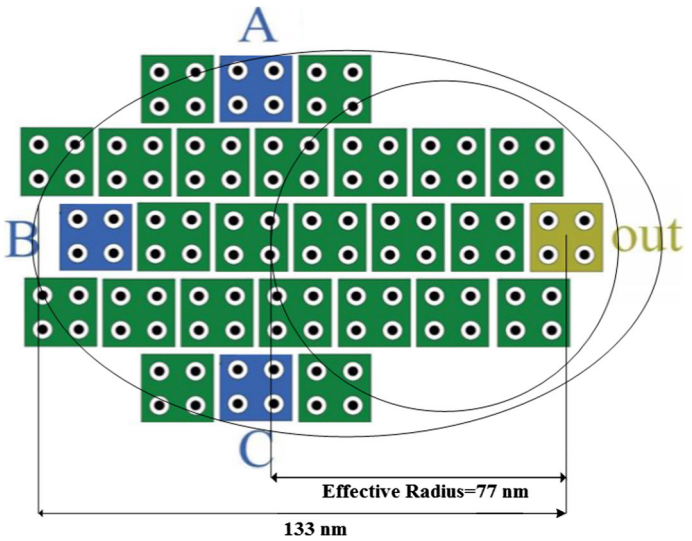


Fig. 8 Effective radius in the proposed structure

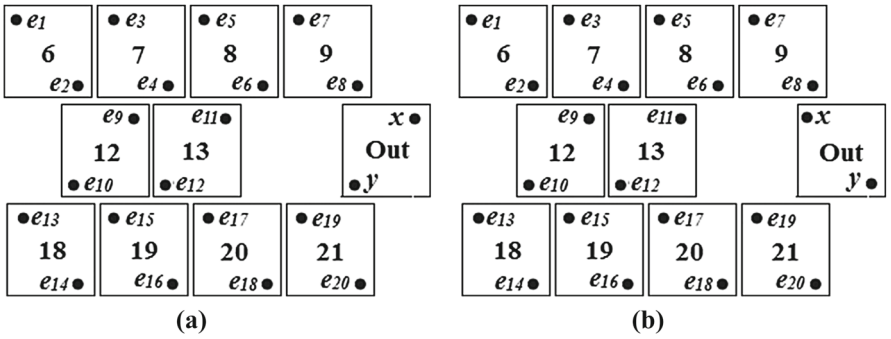


Fig. 9 The output cell polarity in two various states **a** +1 polarization and **b** − 1 polarization

the proposed structure has 27 cells, we should test all the single-cell omission defects that may happen in cells to verify the correctness of this structure. Due to the large computations, only one possible defect had been verified and other single-cell omission defects can be proven similarly. For this analysis, it was necessary to first calculate the kink energies of other cells in the effective radius on the output cell for the single-cell omission defect using the equations in Sect. 2.2. As it can be seen in Fig. 8, the effective radius was supposed 77 nm. Furthermore, it is assumed that input vector is $(A, B, C) =$ (1, 0, and 1) and single-cell omission defect occurs in the cell 14. Therefore, we have to determine the kink energy between electrons e_1 to e_{20} for two states (a) and (b) with the x and y electrons of the output cell shown in Fig. 9. Since cells 1, 2, 3, 4, 5, 10, 11, 15, 16, 17, 22, and 23 are far from the output cell, their kink energy can be ignored.

Table 1 Physical verification for the output cell in Fig. 9a

Applied kink energy to electron x	Applied kink energy to electron y
$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{90.24\times10^{-9}} \approx 0.26\times10^{-20}$(J)	$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{79.65\times10^{-9}} \approx 0.29\times10^{-20}$(J)
$U_2 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{70.03\times10^{-9}} \approx 0.33\times10^{-20}$(J)	$U_2 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{55.71\times10^{-9}} \approx 0.41\times10^{-20}$(J)
$U_3 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{70.88\times10^{-9}} \approx 0.33\times10^{-20}(J)$	$U_3 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{62.8\times10^{-9}} \approx 0.37\times10^{-20}(J)$
$U_4 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{50.04\times10^{-9}} \approx 0.46\times10^{-20}$(J)	$U_4 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{37.74\times10^{-9}} \approx 0.6\times10^{-20}$(J)
$U_5 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{52\times10^{-9}} \approx 0.44\times10^{-20}$(J)	$U_5 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{48.41\times10^{-9}} \approx 0.48\times10^{-20}$(J)
$U_6 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{30.07\times10^{-9}} \approx 0.77\times10^{-20}$(J)	$U_6 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{23.32\times10^{-9}} \approx 0.99\times10^{-20}$(J)
$U_7 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{34.41\times10^{-9}} \approx 0.67\times10^{-20}$(J)	$U_7 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{39.29\times10^{-9}} \approx 0.59\times10^{-20}$(J)
$U_8 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{10.2\times10^{-9}} \approx 2.26\times10^{-20}$(J)	$U_8 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{21.54\times10^{-9}} \approx 1.07\times10^{-20}$(J)
$U_9 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{60\times10^{-9}} \approx 0.38\times10^{-20}$(J)	$U_9 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{45.69\times10^{-9}} \approx 0.5\times10^{-20}$(J)
$U_{10} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{80.05\times10^{-9}} \approx 0.29\times10^{-20}$(J)	$U_{10} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{60\times10^{-9}} \approx 0.38\times10^{-20}$(J)
$U_{11} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{40\times10^{-9}} \approx 0.58\times10^{-20}$(J)	$U_{11} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{28.43\times10^{-9}} \approx 0.81\times10^{-20}$(J)
$U_{12} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{60.73\times10^{-9}} \approx 0.38\times10^{-20}$(J)	$U_{12} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{40\times10^{-9}} \approx 0.58\times10^{-20}$(J)
$U_{13} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{90.24\times10^{-9}} \approx 0.26\times10^{-20}$(J)	$U_{13} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{70.03\times10^{-9}} \approx 0.33\times10^{-20}$(J)
$U_{14} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{79.65\times10^{-9}} \approx 0.29\times10^{-20}$(J)	$U_{14} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{55.71\times10^{-9}} \approx 0.41\times10^{-20}$(J)
$U_{15} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{70.88\times10^{-9}} \approx 0.33\times10^{-20}$(J)	$U_{15} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{50.04\times10^{-9}} \approx 0.46\times10^{-20}$(J)
$U_{16} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{62.8\times10^{-9}} \approx 0.37\times10^{-20}$(J)	$U_{16} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{37.74\times10^{-9}} \approx 0.6\times10^{-20}$(J)
$U_{17} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{52\times10^{-9}} \approx 0.44\times10^{-20}$(J)	$U_{17} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{30.07\times10^{-9}} \approx 0.77\times10^{-20}$(J)
$U_{18} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{48.41\times10^{-9}} \approx 0.48\times10^{-20}$(J)	$U_{18} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{23.32\times10^{-9}} \approx 0.99\times10^{-20}$(J)
$U_{19} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{34.31\times10^{-9}} \approx 0.67\times10^{-20}$(J)	$U_{19} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{10.2\times10^{-9}} \approx 2.26\times10^{-20}$(J)
$U_{20} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{39.29\times10^{-9}} \approx 0.59\times10^{-20}$(J)	$U_{20} = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{21.54\times10^{-9}} \approx 1.07\times10^{-20}$(J)
$U_{T_{11}} = \sum_{i=1}^{20} U_i = 10.58\times10^{-20}$(J)	$U_{T_{12}} = \sum_{i=1}^{20} U_i = 13.96\times10^{-20}$(J)
$U_{T1} = \sum_{i=1}^{2} U_{T_{1i}} = 24.54\times10^{-20}$(J)	

The values of kink energy between electrons e_1 and e_{20} with x and y electrons shown in Fig. 9, for two states of (a) and (b), are given in Tables 1 and 2, respectively.

Comparison of results revealed that the output cell electrons are positioned in Fig. 9a which is more stable and has lower kink energy. Thus, the output cell polarity is equal to '1' and it had been obtained correctly.

Table 2 Physical verification for the output cell in Fig. 9b

Applied kink energy to electron x	Applied kink energy to electron y
$U_{T_{21}} = \sum_{i=1}^{12} U_i = 15.17 \times 10^{-20}$(J)	$U_{T_{22}} = \sum_{i=1}^{12} U_i = 9.75 \times 10^{-20}$(J)
$U_{T2} = \sum_{i=1}^{2} U_{T_{2i}} = 24.92 \times 10^{-20}$(J)	

Table 3 The simulation results of the proposed structure under single-cell omission defects

Removed cell	Output	Removed cell	Output
1	MV3	13	MV3
2	MV3	14	MV3
3	MV3	15	MV3
4	MV3	16	MV3
5	MV3	17	MV3
6	MV3	18	MV3
7	MV3	19	MV3
8	MV3	20	MV3
9	MV3	21	MV3
10	MV3	22	MV3
11	MV3	23	MV3
12	MV3		

MV3 = three-input majority gate

3.2 Fault-tolerant analysis

In order to show the high reliability of the proposed structure, we analyze the function of the proposed structure under single-cell omission and double-cell omission, extra cell deposition, and cell displacement defects.

Table 3 presents the simulation results for the proposed structure under single-cell omission defect.

As it is shown in Table 3, the proposed majority gate has correct output (MV3 function) for all single-cell omission defects. Therefore, this structure is 100% tolerant under single-cell omission defects.

The simulation results of the proposed structure under double-cell omission defect are provided in Table 4.

As it can be seen in Table 4, there are a total of 253 states of double-cell omission defects in the proposed structure, and among them, 215 cases are MV3 function, 21 cases are wire function, 13 cases are NOT function, and finally, four cases are undefined functions. Therefore, this structure is 84.98% fault-tolerant under double-cell omission defects.

Table 5 provides comparisons of the fault-tolerant characteristics of the different majority gate under single- and double-cell omission defects. Furthermore, Fig. 10a–d shows the area, cell counts and fault-tolerant for the proposed structure.

Table 4 The simulation results of the proposed structure under double-cell omission defects

Observation	Counts
Total defective patterns	253
Occurrence of MV3 function	215
Occurrence of MV3-like function	0
Occurrence of wire function	21
Occurrence of NOT function	13
Occurrence of undefended function	4

Table 5 Performance comparison of several majority gates under single- and double-cell omission defects

Design	Area (μm^2)	Cell counts	Delay (clock)	Fault tolerance (%)	
				Single cell	Double cell
In [29]	0.01	13	0.25	66.70	36.10
In [30]	0.02	27	0.25	95.65	78.00
In [31]	0.01	12	0.25	75.00	42.00
In [33]	0.01	19	0.25	60.00	31.00
In [9]	0.01	20	0.50	87.50	60.00
In [32]	0.04	43	0.25	97.44	82.86
In [34]	0.01	25	0.25	80.95	39.80
In [35]	0.03	36	0.25	93.80	66.70
In [36]	0.01	13	0.25	66.66	22.20
Proposed	0.02	27	0.25	100	84.98

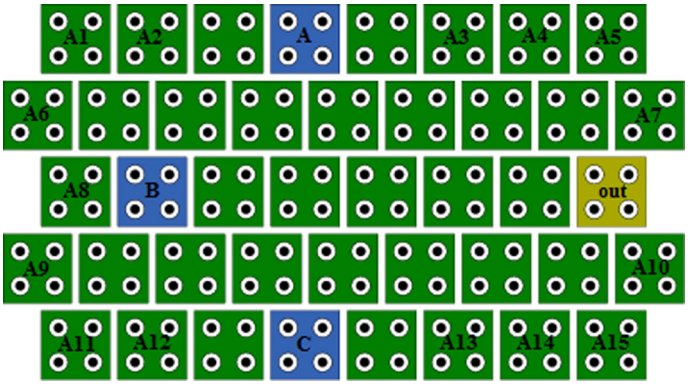


Fig. 10 Extra cells in the proposed structure

An extra cell is located in the regions around the driver cells of the proposed structure to investigate the effects of defect arising out of additional cell deposition. The possible

Table 6 The simulation results of the proposed structure under extra cell deposition defects

Extra cell	Output	Extra cell	Output
A1	MV3	A9	MV3
A2	MV3	A10	MV3
A3	MV3	A11	MV3
A4	MV3	A12	MV3
A5	MV3	A13	MV3
A6	MV3	A14	MV3
A7	MV3	A15	MV3
A8	MV3		

Table 7 Impact of cell displacement and misalignment defects

Cell name	Displacement defect		Misalignment defect	
	North	South	East	West
1	∞	–	–	∞
A	≤ 4	–	–	–
2	∞	–	∞	–
3	∞	–	–	∞
8	∞	–	–	–
9	∞	–	–	∞
B	–	–	∞	≤ 43
Out	–	–	≤ 20	–
15	–	∞	–	∞
20	–	∞	–	–
21	–	∞	∞	–
22	–	∞	–	∞
C	–	≤ 4	–	–
23	–	∞	∞	–

extra cell depositions in the proposed structure are A1 to A15 (Fig. 10). All possible additional cell depositions in the proposed structure are provided in Table 6.

According to Table 6, the proposed gate has MV3 function for all extra cell deposition defects. Therefore, this gate is 100% fault-tolerant under extra cell deposition defects.

At last, the proposed structure is analyzed under cell displacement and cell misalignment defects. The simulation results of the proposed structure under cell displacement and misalignment defects are shown in Table 7. It should be noted that the symbol '-' indicates that displacement or misalignment of the corresponding cell along that particular direction is not allowed. Note that a permissible displacement of 500 nm implies that the corresponding defect hardly has any effect on the functional behavior of the structure. It is shown by the symbol '∞.'

As it is shown in Table 7, the proposed design has proper resistance for all cell displacement and cell misalignment defects.

Table 8 Results of energy dissipation of the proposed structure

Design	Avg. leakage energy diss. (meV)			Avg. switching energy diss. (meV)			Total energy diss. (meV)		
	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$
In [33]	4	11.77	21.74	49.44	46.66	43.29	53.44	58.43	65.03
In [9]	3.89	12.36	23.45	48.73	45.36	41.32	52.62	57.72	64.77
In [30]	8.2	26.32	49.6	99.14	91.91	83.65	107.34	118.23	133.25
In [32]	26.61	69.27	114.65	57.44	45.99	37.25	84.05	115.26	151.9
In [34]	6.16	17.76	31.91	61.37	57.46	53.19	67.53	75.21	85.09
In [35]	6.7	21.47	41.07	110.75	105.31	98.61	117.45	126.78	139.68
Proposed	10.95	28.32	46.77	23.18	18.60	15.10	34.13	46.92	61.87

3.3 Energy dissipation

Energy dissipation of the proposed structure at three different levels $0.5E_K$, $1E_K$, and $1.5E_K$ with temperature of 2.0 K has been calculated using the QCAPro tool [43]. The results are given in Table 8. Moreover, energy dissipation maps are shown in Fig. 11. It should be noted that high-power cells generate a lot of heat in which hot spots appear in darker colors.

4 Proposed fault-tolerant 2:1 multiplexer

One of the logic circuits is multiplexer that is used in a wide range of digital circuits such as RAM and ALU. Multiplexer is a circuit that is capable of selecting one of the inputs and transmits it to the output. So far, several approaches of designing multiplexes have been presented in QCA technology, which differs in cell counts and delays [24, 44–48]. In this section, a single-layer 2:1 multiplexer in QCA technology had been suggested first. Then, its fault-tolerant version was given by the proposed fault-tolerant majority gate.

The proposed 2:1 QCA multiplexer has two inputs, an address line, and an output. The inputs are labeled as A and B, and the output is shown by F. Here the address line named as S. When S is 0, input A is selected, and when S is 1, input B transmits at the output. The logic equation of the 2:1 multiplexer is as follows:

$$F = A\bar{S} + BS \tag{4}$$

Layout of the proposed 2:1 QCA multiplexer is shown in Fig. 12. As it can be seen, this design includes 35 cells and produces correct output in four clock phases.

Furthermore, cellular view of the proposed fault-tolerant 2:1 multiplexer is shown in Fig. 13.

In addition, the fault-tolerant versions of the proposed 2:1 QCA multiplexer using fault-tolerant majority gates of [29, 33] are shown in Fig. 14.

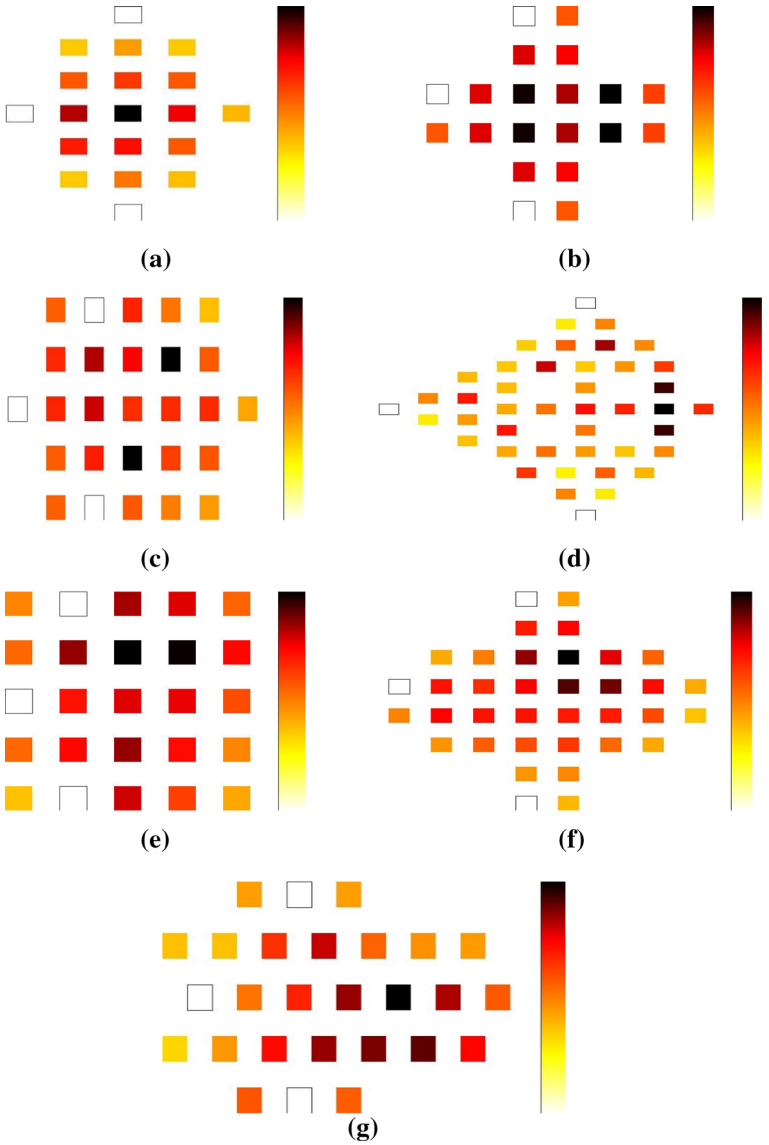


Fig. 11 Energy dissipation maps for majority gate cells (at 2.0 K with $0.5E_k$) **a** design of [33], **b** design of [9], **c** design of [30], **d** design of [32], **e** design of [34], **f** design of [35], and **g** proposed design

5 Simulation results

QCA Designer software 2.0.3 has been used to simulate proposed designs. There are two simulation engines in the QCA Designer software called 'Bistable Approximation' and 'Coherence Vector' [38]. In this paper, the 'Bistable Approximation Engine' is

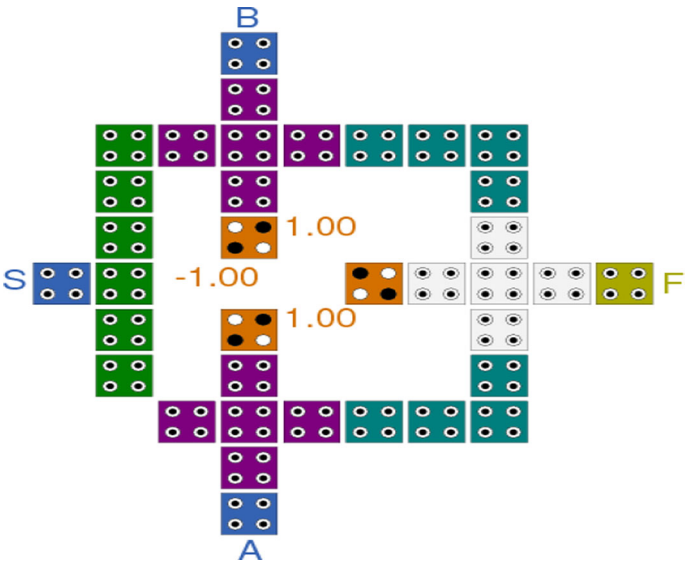


Fig. 12 The proposed single-layer 2:1 QCA multiplexer

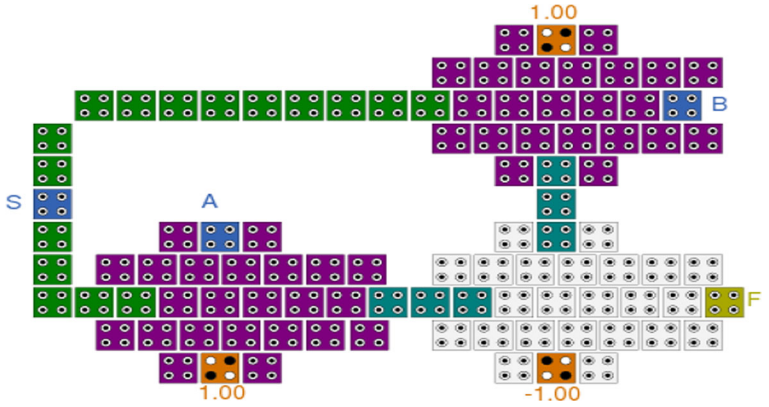


Fig. 13 Layout of the proposed fault-tolerant 2:1 multiplexer using the proposed structure

used. All parameters and simulation conditions have default values of the software, as shown in Table 9.

Results of the proposed fault-tolerant 2:1 multiplexer for all combinations of S, A, and B inputs are shown in Fig. 15. Simulation results indicate that the proposed fault-tolerant multiplexer operates well. For instance, for inputs $S = 1$, $A = 0$ and $B = 1$, the correct output is obtained. As it can be seen in Fig. 15, the output is of very high quality.

Results of comparing the proposed fault-tolerant multiplexer with other designs from single- and double-cell omission defect viewpoints are shown in Table 10.

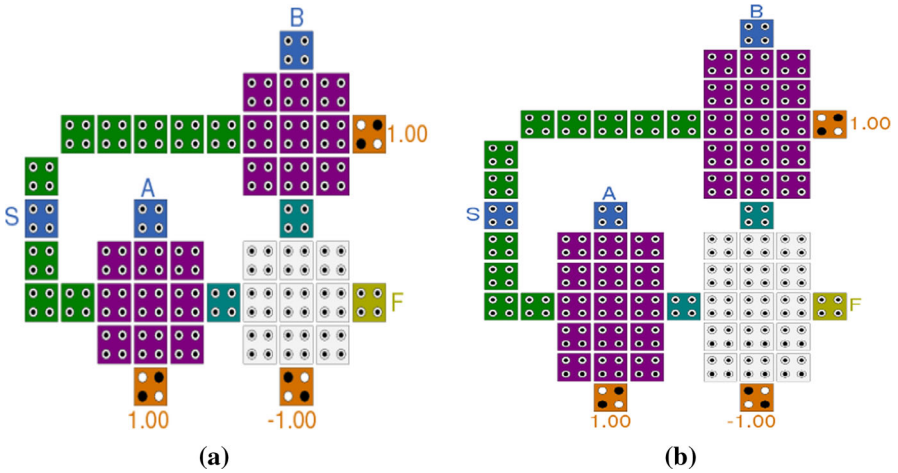


Fig. 14 Fault-tolerant 2:1 multiplexers using the majority gates presented in **a** [29], and **b** [33]

Table 9 Parameters used in the bistable approximation engine for simulations

Parameters	Values
Cell size	18 nm
Number of samples	128,000
Convergence tolerance	0.001
Radius of effect	65.000000 nm
Relative permittivity	12.900000
Clock low	3.800000e023 J
Clock high	9.800000e022 J
Clock shift	0.00000e+000
Clock amplitude factor	2.000000
Layer separation	11.500000
Maximum iterations per sample	100

As it is shown in Table 10, the proposed fault-tolerant multiplexer has the ability for 89 and 62.59% tolerance under single- and double-cell omission defects, respectively. This indicates that the proposed multiplexer has a much higher resilience than other designs.

In addition, the temperature effect on the output polarization of the multiplexer circuits has been analyzed. Figure 16 shows the variation of polarization with respect to temperature in a range of 0–28 K.

As can be seen in Fig. 16, although the output of the multiplexer circuits in Fig. 14a, b, respectively, when temperature passes from 5 and 8 K, will be broken, the output of the proposed fault-tolerant multiplexer sustains full stability for a wide range of temperature. So, it can be concluded that the proposed fault-tolerant multiplexer is more robust against temperature variations than other designs.

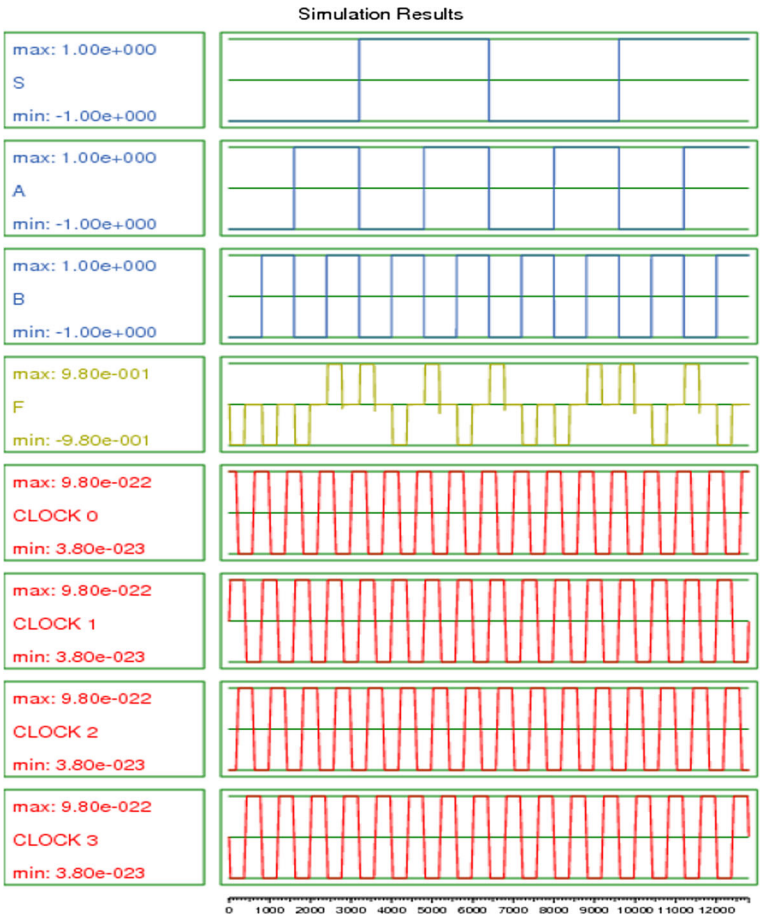


Fig. 15 Simulation results of the proposed 2:1 QCA fault-tolerant multiplexer

6 Conclusion

In this paper, we first proposed a novel fault-tolerant three-input majority gate. The proposed structure was 100, 84.98, and 100% fault-tolerant under single-cell omission, double-cell omission, and extra cell deposition defects, respectively, as well as benefits a high output power. Physical proofs confirmed the simulation results. QCA Designer 2.0.3 software was used to simulate the proposed circuits. Using this structure, we proposed a novel fault-tolerant 2:1 multiplexer. The results of the comparisons showed that the proposed fault-tolerant multiplexer has higher degree of fault tolerance than other designs. Our future works include using the proposed fault-tolerant designs for other fault-tolerant structures such as ALU and RAM.

Table 10 Comparison of the proposed fault-tolerant multiplexer with other designs in terms of single- and double-cell omission defects

Description	Fault-tolerant 2:1 multiplexer					
	Proposed deign		Figure 14a		Figure 14b	
	#Defective cells		#Defective cells		#Defective cells	
	1	2	1	2	1	2
All possible states	69	759	27	108	45	315
No. of correct outputs	60	475	9	18	29	106
No. of incorrect outputs	9	284	18	90	16	209
Fault tolerance (%)	86.96	62.59	33.33	16.67	64.45	33.66

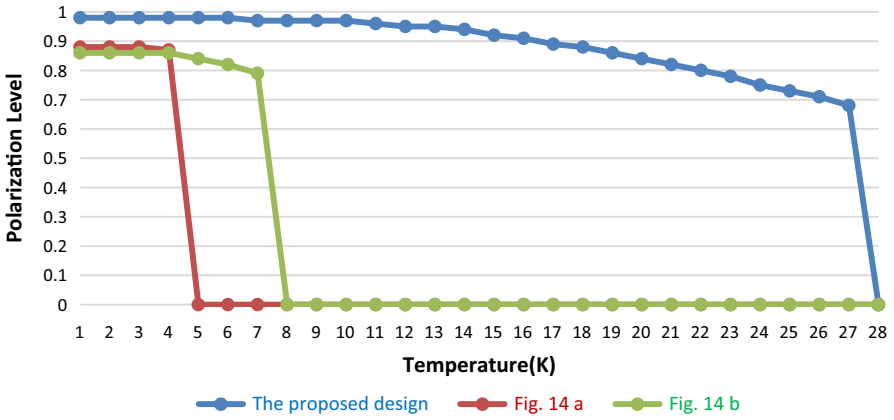


Fig. 16 Polarization versus temperature variations for the multiplexer output

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