J Supercomput (2018) 74:1994–2005
https://doi.org/10.1007/s11227-017-2206-4

A full adder structure without cross-wiring in quantum-dot cellular automata with energy dissipation analysis

Saeed Rasouli Heikalabad[1] · **Mazaher Naji Asfestani**[1] · **Mehdi Hosseinzadeh**[2,3]

Published online: 4 December 2017

Abstract Quantum-dot cellular automata (QCA) is the appearance of new technology and can be a suitable alternative to semiconductor transistor technology. In this paper, the new structure of the two-input XOR gate is presented, which is the modified version of the three-input XOR gate. This structure can be used to design various useful QCA circuits. By utilizing this gate, we design and implement a new full adder structure with 90-degree cells. This structure is designed in a single layer without cross-wiring. The operation of the proposed structure has been verified by QCADesigner version 2.0.3 and energy dissipation investigated by QCAPro tool. We also compared the effectiveness of our structure with the two previous structures.

Keywords Quantum-dot cellular automata (QCA) · Nanotechnology · XOR gate · Full adder

1 Introduction

CMOS technology based on today's traditional transistors follows Moore's law. This law was introduced by Gordon Moore in 1965 and predicts that the number of transistors placed inside a chip will double every 2 years. Therefore, minimizing transistor dimensions is needed to design high-speed, high-density, and power-down circuits [1]. Today, many integrated circuits have been made on a scale of 0.23–0.33 microns,

✉ Saeed Rasouli Heikalabad
s.rasouli@iaut.ac.ir; s.rasouli.h@gmail.com

1 Department of Computer Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran

2 Iran University of Medical Sciences, Tehran, Iran

3 Computer Science, University of Human Development, Sulaimaniyah, Iraq

but when the size of the device reaches 0.5 microns or less, physical limitations such as power dissipation and problems with lithography and design complexity arise [2]. Thus, doubling the number of transistors in a microprocessor every 2 years and doubling the clock speed every 3 years will not be possible. As a result, to improve the performance of arithmetic units, there is a need for other technologies [3–5].

As successor to CMOS, researchers have proposed a method in which computations are performed by quantum dots. This technology was first introduced in 1994 and was called quantum-dot cellular automata. In QCA, unlike today's computers that transmit information through electrical current from one point to another, the transmission of polarization status causes data transfer. In this technology, binary values are created by different specific electron arrangements at the quantum dots in a cell. Quantum cells are in the form of a square, and quantum dots are located in the corners of the square. Each cell has two extra electrons that are arranged diagonally by electrical repulsion. How polarization of quantum cells represents zero and one binary. The cell is polarized by enabling the Columbic interaction with neighboring cells [6]. In this way, it does not establish any electrical current between cells. Therefore, this technology has very low power dissipation [7–14].

The main contribution of this study is to present a new structure for single-bit full adder based on two-input XOR gate without cross-wiring.

2 Background

Quantum-dot cellular automata is a new technology suitable for nanoscale structures [10,15–17]. The basic element of QCA is a square quantum cell. Four quantum dots are located in the corner of a cell, and two electrons are located inside them [18]. Figure 1a shows the structure of a quantum cell and two stable arrangements of electrons encoded to logic "0" and logic "1."

One of the primary structures in QCA is three-input majority gate. QCA three-input majority gate performs the majority function of the three inputs A, B, and C as AB + AC + BC. Figure 1b shows the structure of this gate. Also the two-input OR and AND gates are constructed by fixing one of the majority gate inputs to the polarizations "+ 1" and "− 1," respectively. The inverter gate with two different configurations of the QCA cells is shown in Fig. 1c.

3 Clock Operation

The clocking scheme in the QCA consists of four phases. In the first phase or Switch phase, cell is in non-polarity state and the potential barrier among quantum dots is down. During this phase, the barrier goes up and the cell begins to polarize according to its own input. In the second phase or the Hold phase, the barrier is kept high. In the third phase or Release phase, the barrier is lowered and the cells will be allowed to go into internal polarity state. Finally, during the fourth phase which is called Relax phase, the potential barrier is kept low and cell remains in non-polarity state [19–21]. Four phases clock scheme is shown in Fig. 2.

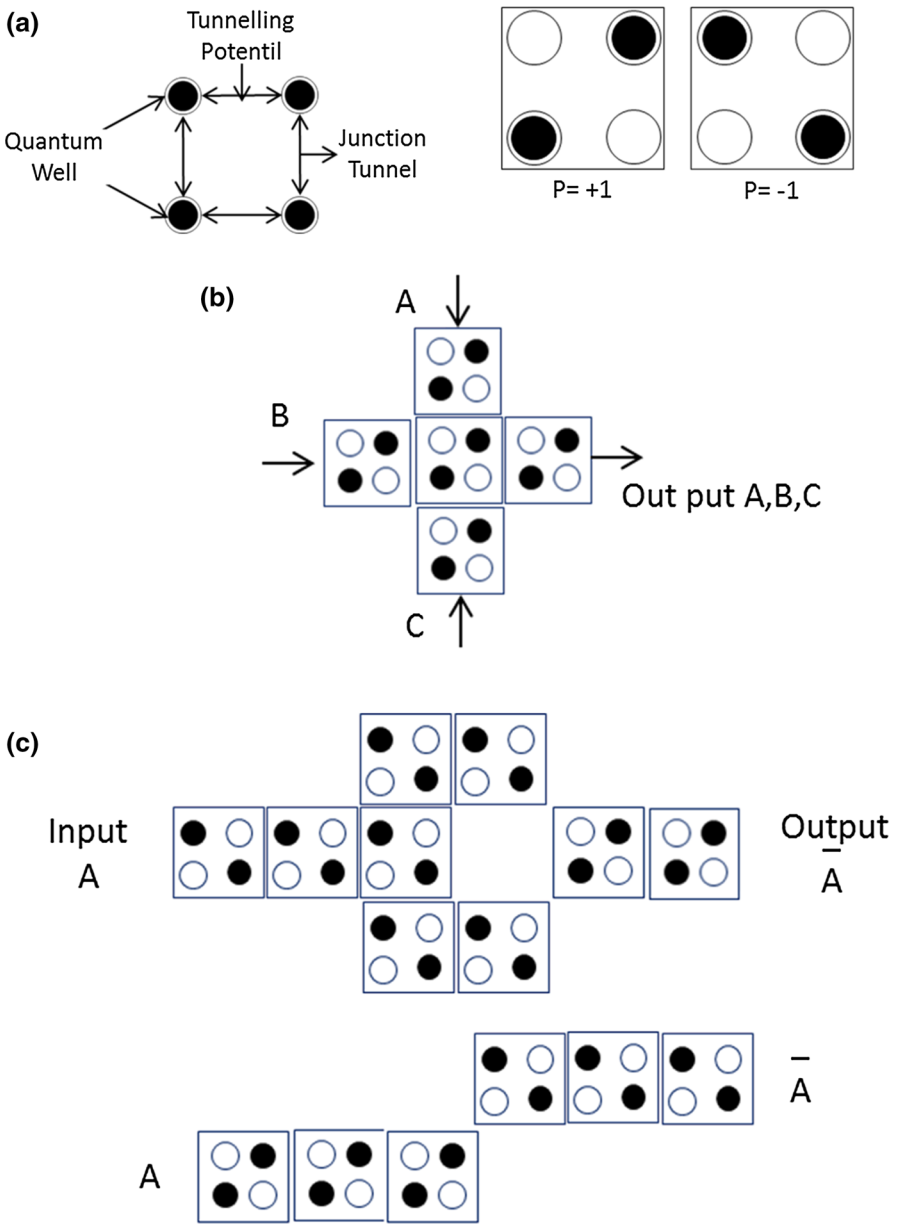

Fig. 1 QCA basic structures. **a** QCA cell. **b** Three-input majority gate. **c** Inverter gate

4 Related works

One of the most basic components in the design of the arithmetic unit is a full adder. The following two equations are mostly considered in the design of a single-bit full adder.

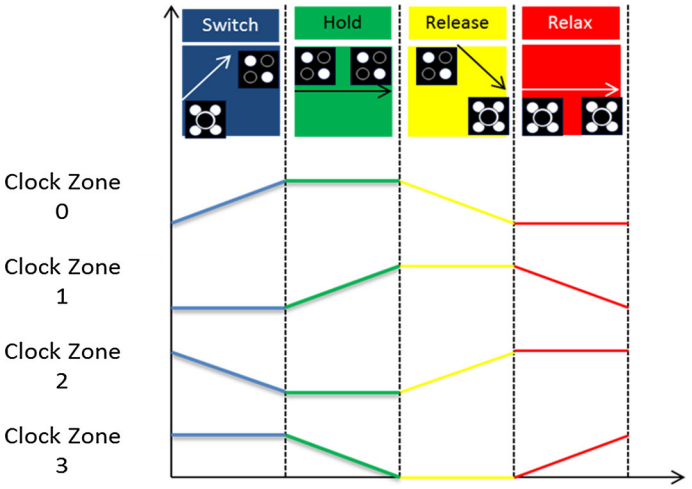

Fig. 2 QCA clocking scheme

Table 1 Truth table for a single-bit full adder

A	B	C_{in}	SUM	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$Sum = A \oplus B \oplus C_{\text{in}} \tag{1}$$

$$C_{\text{out}} = AB + C_{\text{in}}(\text{A} \oplus B) \tag{2}$$

Output *Sum* is the binary summation of three inputs A, B and C_{in}. The inputs A and B are the new two binary inputs. C_{in} is the carry out of the least significant binary bits. C_{out} represents the generated carry from the sum of the three binary inputs A, B and C_{in}. Table 1 shows the truth table of a single-bit full adder.

In recent years, research on the design of nanoscale full adder is significantly increased especially in the QCA [22–26]. In [22], a single-bit adder is presented using two majority gates. The QCA design of this structure is shown in Fig. 3a. This structure uses a five-input majority gate to produce SUM signal. In [23], a design of single-bit full adder by using three majority and two inverter gates is introduced. Figure 3b shows the QCA layout of this structure. As shown in Fig. 3, both of these structures use cross-wiring and are therefore not robust. In [27], the structure of presented full adder consists of two main components, the three-input majority gate and the three-input XOR gate.

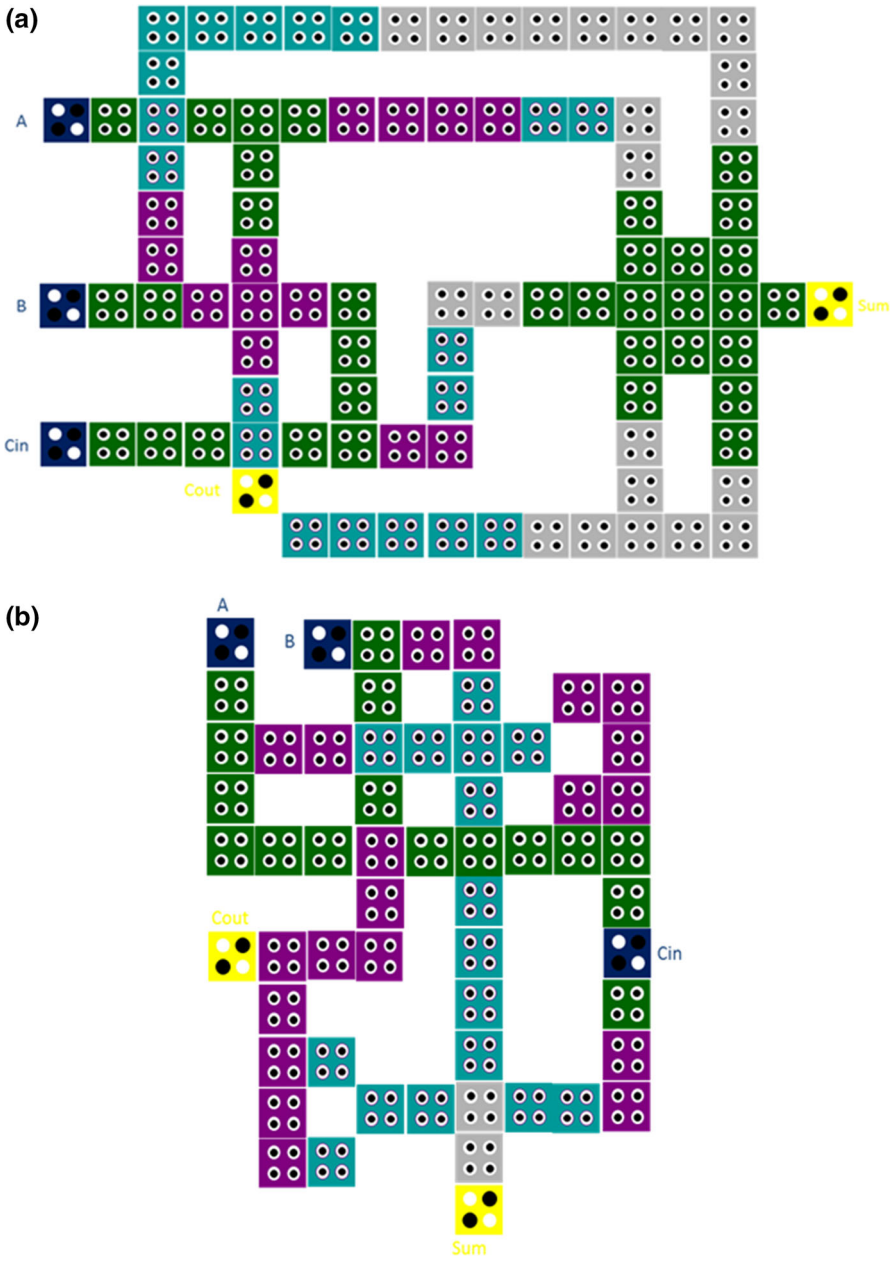

Fig. 3 Full adder structures. **a** Presented in [22]. **b** Presented in [23]

In this structure, the conventional wire crossing method is employed to transmit two input values independently. In the next section, we propose a new structure for the single-bit full adder based on the two-input XOR gate without cross-wiring.

Table 2 Truth table for two-input XOR gate

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

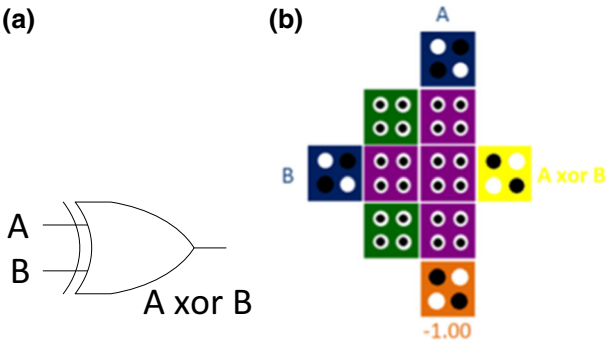

Fig. 4 Structure of two-input XOR gate extracted from design [27]. **a** Schematic. **b** QCA layout

5 Proposed Structure

This section explains the proposed structure of the single-bit full adder. For this purpose, we first introduce the structure of two-input XOR extracted from the design [27] and then describe the design of the single-bit full adder using QCA cells.

The output of the two-input XOR gate is obtained by

$$A \oplus B = \bar{A}B + A\bar{B} \tag{3}$$

where A and B are the two binary inputs. Table 2 shows the truth table for this gate. As can be seen from Table 2, the output of "1" is when the inputs are not equal.

We use a structure for the two-input XOR gate in QCA that is extracted from design [27] as Fig. 4. This structure has 10 cells. Two cells with labels A and B are input cells, and one of them is the output cell. One of the cells has fixed polarization of "-1.00," and the remaining cells are the device cells. This structure is designed in a single layer and its latency is two clock zones.

We consider the following equation for the carry out of the full adder to implement the proposed structure.

$$C_{\text{out}} = A(A \odot B) + C_{\text{in}}(A \oplus B) \tag{4}$$

This equation seems more complicated than the original equation, but its implementation in QCA is simple and requires no cross-wiring. This would reduce the size of the proposed structure.

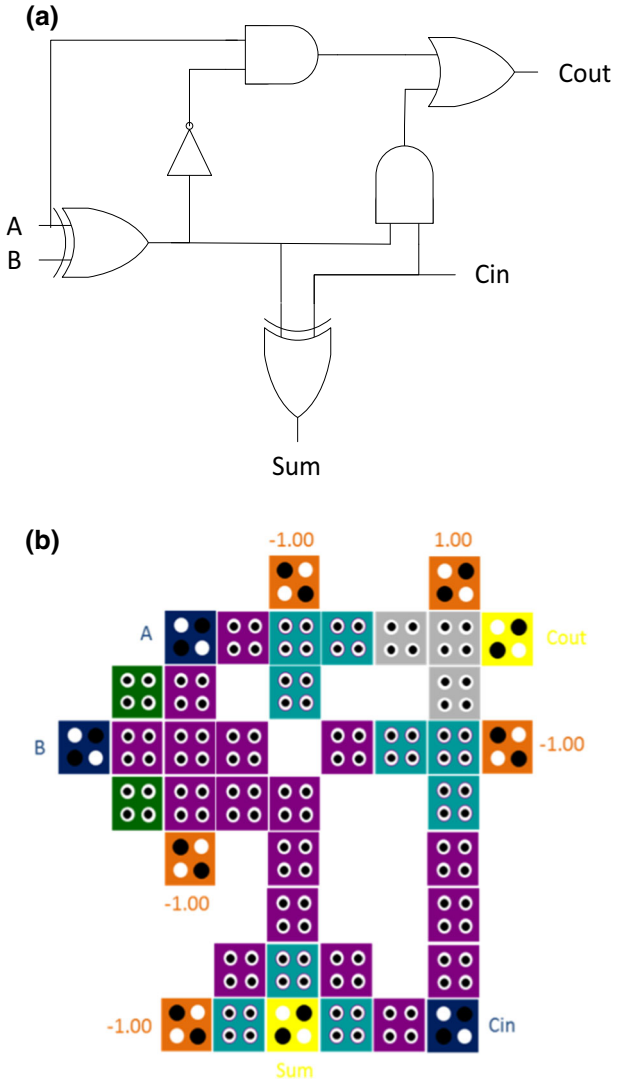

Fig. 5 Structure of proposed single-bit full adder. **a** Schematic. **b** QCA layout

The schematic and QCA implementation of proposed full adder structure are illustrated in Fig. 5a, b, respectively. This design is composed of two two-input XOR gates, two AND gates, one OR gate and one inverter gate. As shown in Fig. 5b, proposed design is implemented in a single layer. It uses only 90-degree cells and does not use the coplanar cross-wiring.

Table 3 Simulation parameters

Parameter	Value
Cell size	18 nm * 18 nm
Dot diameter	5 nm
Cell separation	2 nm
Simulation engine	Bistable approximation/ coherence vector
Radius of effect	65 nm
Number of samples	12,800
Convergence tolerance	0.001000
Temperature	1.000000
Relative permittivity	12.900000
Clock high	9.800000e−022
Clock low	3.800000e+023
Clock shift	0.000000e+000
Clock amplitude Factor	2.000000
Layer separation	11.500000
Maximum iterations per sample	100

6 Simulation results and comparison

The structures of the two-input XOR gate and single-bit full adder have been simulated with QCADesigner tool 2.0.3 [28]. Simulation parameters are initialized as shown in Table 3. GaAs-based cells are considered [29].

The simulation results of the two-input XOR gate and full adder are illustrated in Fig. 6a, b, respectively. The results confirm that the proposed structures work properly and exactly like the truth tables.

We compared the proposed full adder structure with the previous two works presented in [22,23]. Implementation results are given in Table 4. The table contains the number of cells, occupied area, latency and cross-wiring. Implementation results indicate that our design is better than previous designs in all of the parameters. Our design achieved 56 and 31% improvement in cell count compared to the structures presented in [22,23], respectively. Also, proposed structure achieved 67 and 30% improvement in occupied area compared to the structures presented in [22,23], respectively. In addition, number of clock zones has reduced by 20% compared to the structure presented in [22]. Our design does not use cross-wiring.

We use QCAPro tool [30] to evaluate power consumption of QCA circuits. This tool is used to calculate the leakage and switching energy dissipation. Analysis results of energy dissipation of full adders in three different tunneling energy levels (0.5 E_k, 1 E_k and 1.5 E_k) are shown in Table 5. It is obvious that our design has achieved 60 and 37% reduction in total power dissipation compared to the structures presented in [22,23], respectively. The power dissipation map of our structure with 0.5 E_k is shown in Fig. 7. In this map, the darker cells consume more energy.

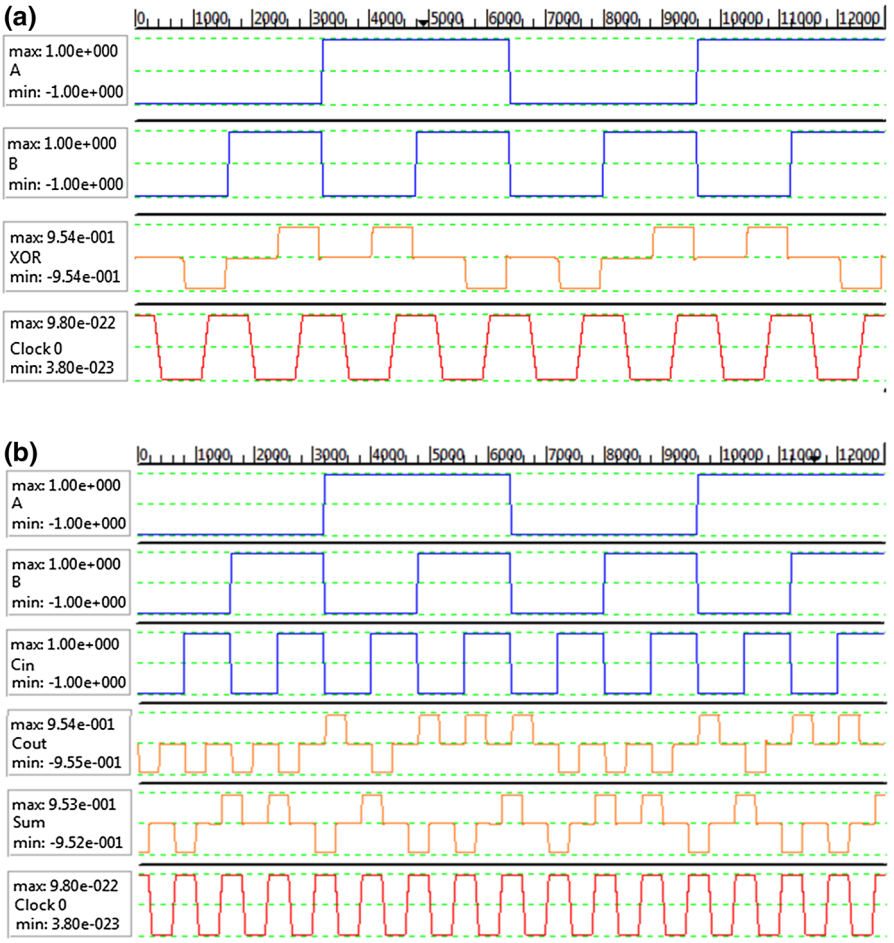

Fig. 6 Simulation results of the structures. **a** Two-input XOR gate. **b** Full adder

Table 4 Implementation results of the single-layer full adders

Structure	Cell count	Area (μm^2)	Latency (clock zone)	Cross-wiring
Presented in [22]	93	0.09	5	Yes
Presented in [23]	59	0.043	4	Yes
Our design	41	0.03	4	No

Table 5 Analysis of energy consumption of the full adders

Structure	Avg. leakage energy dissipation (eV)			Avg. switching energy dissipation (eV)			Total energy dissipation (eV)		
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
Presented in [22]	0.02652	0.08139	0.14716	0.15902	0.14040	0.12184	0.18554	0.22179	0.269
Presented in [23]	0.01598	0.05030	0.09163	0.10249	0.09007	0.07767	0.11847	0.14037	0.1693
Our design	0.01405	0.03932	0.06802	0.05061	0.04467	0.03895	0.06466	0.08399	0.10697

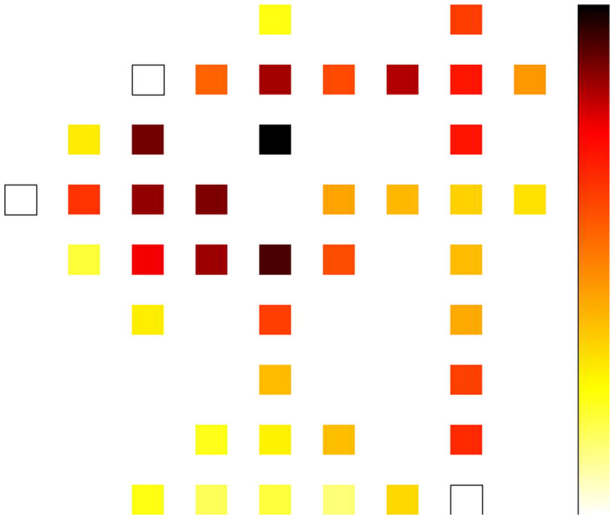

Fig. 7 Power dissipation map for the proposed full adder with 0.5 E_k

7 Conclusion

In this paper, we introduced a structure for two-input XOR gate to design a single-bit full adder in QCA. This structure is extracted from the previous design of three-input XOR gate. The structure of this gate can be constructed with only 10 QCA cells. By utilizing this gate, we designed a novel full adder structure. This structure is designed in a single layer without cross-wiring. QCADesigner is used to simulate these structures. Simulation results confirmed the operations of proposed structures. The comparison demonstrated that the proposed structure is better than previous designs. We used QCAPro to evaluate power consumption of QCA structures.

References

1. Heikalabad SR, Navin AH, Hosseinzadeh M (2015) Midpoint memory: a special memory structure for data-oriented models implementation. J Circuits Syst Comput 24:1550063
2. Yu W, Zhang B, Liu C, Zhao Y, Wu WR, Xue ZY, Chen M, Buca D, Hartmann J-M, Wang X, Zhao QT, Mantl S (2014) Impact of Si cap, strain and temperature on the hole mobility of (s)Si/sSiGe/(s)SOI quantum-well p-MOSFETs. Microelectron Eng 113:5–9. https://doi.org/10.1016/j.mee.2013.06.015
3. Liu M (2006) Robustness and power dissipation in quantum-dot cellular automata. Ph.D. thesis, Notre dame University, Indiana
4. Heikalabad SR, Navin AH, Hosseinzadeh M (2016) Content addressable memory cell in quantum-dot cellular automata. Microelectron Eng 163:140–150
5. Fey D (2012) Optical multiplexing techniques for photonic Clos networks in High Performance Computing Architectures. J Supercomput 62(2):620–632
6. Bose R, Johnson HT (2004) Coulomb interaction energy in optical and quantum computing applications of self-assembled quantum dots. Microelectron Eng 75(1):43–53. https://doi.org/10.1016/j.mee.2003.11.008
7. Niemier MT (2004) Designing digital systems in quantum cellular automata. M.S. thesis, Notre Dame University, Indiana

8. Karkaj ET, Heikalabad SR (2017) Binary to gray and gray to binary converter in quantum-dot cellular automata. Optik Int J Light Electron Opt. https://doi.org/10.1016/j.ijleo.2016.11.087
9. Karkaj ET, Heikalabad SR (2017) A testable parity conservative gate in quantum-dot cellular automata. Superlattices Microstruct. https://doi.org/10.1016/j.spmi.2016.08.054
10. Gadim MR, Navimipour NJ (2017) A new three-level fault tolerance arithmetic and logic unit based on quantum dot cellular automata. Microsyst Technol. https://doi.org/10.1007/s00542-017-3502-x
11. Jayashree HV (2016) Ancilla-input and garbage-output optimized design of a reversible quantum integer multiplier. J Supercomput 72(4):1477–1493
12. Valinataj M (2017) Novel parity-preserving reversible logic array multipliers. J Supercomput 73(11):4843–4867
13. Kotiyal S (2015) Reversible logic based multiplication computing unit using binary tree data structure. J Supercomput 71(7):2668–2693
14. Khan MHA (2017) Automatic synthesis of quaternary quantum circuits. J Supercomput 73(5):1733–1759
15. Len CS, Tougaw PD (1993) Lines of interaction quantum-dot cells: a binary wire. J Appl Phys 74:6227–6233
16. Rad SK, Heikalabad SR (2017) Reversible flip-flops in quantum-dot cellular automata. Int J Theor Phys 56(9):2990–3004. https://doi.org/10.1007/s10773-017-3575-4
17. Barughi YZ, Heikalabad SR (2017) A three-layer full adder/subtractor structure in quantum-dot cellular automata. Int J Theor Phys 56(9):2848–2858. https://doi.org/10.1007/s10773-017-3453-0
18. Lent CS, Tougaw PD, Porod W, Bernstein GH (1993) Quantum cellular automata. Nanotechnology 4(1):49–57
19. Lent C, Tougaw P (1997) A device architecture for computing with quantum dots. Proc IEEE 85(4):541–557
20. Asfestani MN, Heikalabad SR (2017) A unique structure for the multiplexer in quantum-dot cellular automata to create a revolution in design of nanostructures. Phys B Phys Condens Matter. https://doi.org/10.1016/j.physb.2017.02.028
21. Asfestani MN, Heikalabad SR (2017) A novel multiplexer-based structure for random access memory cell in quantum-dot cellular automata. Phys B Phys Condens Matter. https://doi.org/10.1016/j.physb.2017.06.059
22. Angizi S, Alkaldy E, Bagherzadeh N, Navi K (2014) Novel robust single layer wire crossing approach for exclusive or sum of products logic design with quantum-dot cellular automata. J Low Power Electron 10:259–271
23. Abedi D, Jaberipur G, Sangsefidi M (2015) Coplanar full adder in quantum-dot cellular automata via clock-zone based crossover. IEEE Trans Nanotechnol 14:497–504. https://doi.org/10.1109/TNANO.2015.2409117
24. Mohammadi M, Mohammadi M, Gorgin S (2016) An efficient design of full adder in quantum-dot cellular automata (QCA) technology. Microelectron J 50:35–43
25. Sasamal TN, Singh AK, Mohan A (2016) An optimal design of full adder based on 5-input majority gate in coplanar quantum-dot cellular automata. Optik Int J Light Electron Opt 127(20):8576–8591
26. Farazkish R, Khodaparast F (2015) Design and characterization of a new fault-tolerant full-adder for quantum-dot cellular automata. Microprocess Microsyst 39(6):426–433
27. Ahmad F, Bhat GM, Khademolhosseini H, Azimi S, Angizi S, Navi K (2016) Towards single layer quantum-dot cellular automata adders based on explicit interaction of cells. J Comput Sci 16:8–15
28. Walus K, Dysart TJ, Jullien GA, Budiman RA (2004) QCADesigner: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans Nanotechnol 3(1):2631
29. Tangmettajittakul O, Thainoi S, Changmoang P, Kanjanachuchai S, Rattanathammaphan S, Panyakeow S (2010) Extended optical properties beyond band-edge of GaAs by InAs quantum dots and quantum dot molecules. Microelectron Eng 87(5–8):1304–1307. https://doi.org/10.1016/j.mee.2009.12.063
30. Srivastava S, Asthana A, Bhanja S, Sarkar (2011) QCAPro-an error power estimation tool for QCA circuit design. In: Proceedings of the IEEE International Symposium Circuits System, pp 2377–2380